CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD

Analytical and Optimization Based Modeling Techniques to Assess the Performance of Submicron SiC MESFETs

by

Muhammad Riaz

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in the

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Department of Electrical Engineering

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In the memory of my parents

and

In the memory of my beloved daughter, Tayyaba

CAPITAL UNIVERSITY OF SCIENCE & TECHNOLOGY
ISLAMABAD

Expressway, Kahuta Road, Zone-V, Islamabad
Phone:+92-51-111-555-666 Fax: +92-51-4486705
Email: info@cust.edu.pk Website: https://www.cust.edu.pk

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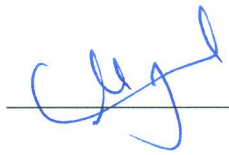
Student Name :	Mr. Muhammad Riaz (PE-071003)	

The Examining Committee unanimously agrees to award PhD degree in the mentioned field.

Examination Committee :

(a)	External Examiner 1:	Dr. Junaid Mughal Professor CIIT, Islamabad	
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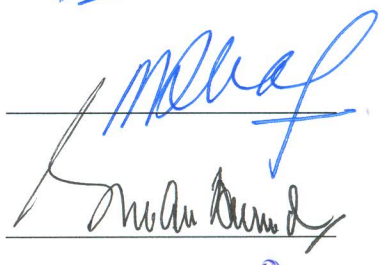
(c)	Internal Examiner :	Dr. Muhammad Ashraf Associate Professor CUST, Islamabad	
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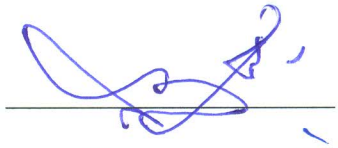
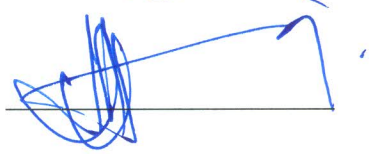
Name of HoD :		Dr. Noor Muhammad Khan Professor CUST, Islamabad	
Name of Dean :		Dr. Imtiaz Ahmad Taj Professor CUST, Islamabad	

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Registration No. PE071003

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List of Publications

1. M. Riaz, M. M. Ahmed, and U. Munir, "An improved model for current voltage characteristics of submicron SiC MESFETs," *Solid State Electronics*, vol. 121, pp. 54-61, 2016.

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Abstract

In the first part of the thesis, a detailed analytical mathematical model describing $I-V$ characteristic of a submicron SiC MESFET has been presented. Poisson's equation with appropriate boundary conditions is solved to determine potential distribution inside the channel. The location of Schottky barrier gate with corresponding depletion layer width where the carrier's velocity gets saturated is evaluated. It has been demonstrated that the depletion modification underneath the Schottky barrier gate causes finite output conductance in the saturation region of operation. $I-V$ characteristics of submicron SiC MESFET have been modeled and compared with conventional velocity saturation techniques, where the depletion layer after the onset of current saturation has been treated as constant. It is noted that the proposed depletion layer modification technique, when incorporated in the device modeling, gave $\sim$15.9% improvement in the modeled out characteristics of a submicron SiC MESFET.

In the second part, an improved empirical model has been presented to simulate DC and pulsed $I-V$ characteristics of SiC MESFETs. A comparative analysis has been carried out by employing swarm optimization technique and it has been established that the proposed model, dependent upon the device characteristics, is $\sim$7-24% better than its counterparts. Based on simulated characteristics, numerous parameters defining the device geometrical structure have been estimated to a good degree of accuracy. It has been shown that the developed technique is versatile enough and can be a useful tool for device simulation softwares.

In the third part, a technique has been developed to estimate intrinsic small signal parameters of submicron SiC MESFETs, designed for high power microwave applications. In the developed technique, small signal parameters are extracted by involving drain-to-source current, I_{ds} instead of Schottky barrier depletion layer expression. It has been demonstrated that in SiC MESFETs, the depletion layer gets modified due to intense transverse electric field and/or self-heating effects, which are conventionally not taken into account. Thus, assessment of AC small signal parameters by employing depletion layer expression loses its accuracy for

devices meant for high power applications. A set of expressions for AC small signal elements have been developed using I_{ds} and their dependence on device biasing have been discussed. The validity of the proposed technique has been demonstrated using experimental data.

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Abbreviations

AlGaN	Aluminium gallium nitride
AlGaAs	Aluminium gallium arsenide
APAR	Active phased array radar
BFOM	Baliga figure of merit
CMOS	Complementary metal-oxide-semiconductor
CW	Continuous wave
C-MESFET	Conventional MESFET
CG-MESFET	Clival gate MESFET
CDLT	Conductance deep-level transient spectroscopy
DIBL	Drain induced barrier lowering
DW-MESFET	Dual well MESFET
DRUP-MESFET	Double upper gate and recessed p-buffer layer MESFET
DR-MESFET	Double recessed MESFET
DRUS-MESFET	Double recessed with a partly undoped space MESFET
DSFP-MESFET	Double source-field plates MESFET
DS-RPB	Recessed p-buffer on drain side
DRB-MESFET	Double recessed p-buffer layer MESFET
ESD	Electro-static discharge
FPs	Field-plates
FMR-MESFET	Floating metal region MESFET
GaAs, GaN	Gallium arsenide and gallium nitride
HEMT	High electron mobility transistor

HD-MESFET	Heavily doped MESFET
I-V	Current-voltage
InP	Indium phosphide
ICs	Integrated circuits
JFET	Junction field effect transistor
JFOM	Johnson figure of merit
KFOM	Keyes figure of merit
LSFP	L-gate and source field plate
LP-MESFET	L-gate and partial p-type spacer MESFET
MESFET	Metal semiconductor field effect transistor
MOSFET	Metal-oxide semiconductor field effect transistor
MMIC	Monolithic microwave integrated circuit
MAG, MSG	Maximum available and stable gain
MR-MESFET	Multi recessed MESFET
MR2-MESFET	Multi recessed metal ring MESFET
MRD-MESFET	Multi recessed source/drain drift MESFET
PAE	Power added efficiency
PD	Power density
PSO	Particle swarm optimization
RF	Radio frequency
RMSE	Root mean square error
R-MESFET	Recessed MESFET
RDRP-CG-MESFET	Drain drift region and recessed p-buffer layer clival gate MESFET
Si, SiC	Silicon and silicon carbide
SRD-MESFET	Single recessed source/drain drift MESFET
SS-RPB	Recessed p-buffer layer on source side
TWT	Traveling wave tube
ΓRP-MESFET	Γ-gate and recessed p-buffer layer MESFET
UU-MESFET	Ultra-high upper gate MESFET
VBR	Breakdown voltage

Symbols

a	Channel epi-layer thickness
a_{eff}	Effective available channel
b	Buffer-layer thickness
c	Speed of light
C_{gs}, C_{gsm}	Conventional and modified gate-to-source capacitance
C_{gd}, C_{gdm}	Conventional and modified gate-to-drain capacitance
C_{ds}, C_{dsm}	Conventional and modified drain-to-source capacitance
c_1, c_2	Cognitive and social parameter
d_m	Distance
E	Applied electric field
$E(x)$	Electric field at any point x inside the channel
E_s	Saturation field
E_g	Energy bandgap
E_{crit}	Critical electric field
f_T, f_{Tm}	Conventional and modified unity gain frequency
f_{max}	Maximum operating frequency
g_m, g_{mm}	Conventional and modified transconductance
g_d, g_{dm}	Conventional and modified output conductance
G_A	Maximum available gain
G_S, G_0, G_L	Power gains
G	RF gain
g_{best}	Swarm optimization global best
h_x	Depletion layer height at any point x

h_0, h_d	Depletion layer height nearer to the source and drain
h_1	Depletion height where carriers attain v_s
I_d, I_{ds}	Drain and drain-to-source current
I_{dsmax}	Breakdown current
I_{dsQ}	Optimum I_{ds}
I_{dss}	Drain-to-source current at $V_{gs} = 0$
I_p	Pinch-off current
$I_{d(sat)}$	Saturation current
I_c, I_{ch}	Channel current
J_d	Drain current density
L_g	Gate-length
L_1, L_2, L_3	Gate length at specific locations
L_s, L_d	Separation between source-gate and drain-gate
m	Swarm size
n	Swarm dimension
N_d	Channel doping concentration
N_{ref}	Reference doing concentration
N_b	Buffer layer doping density
P_{max}	Maximum output power
P_{in}, P_{out}	Input and output power
P_{DC}	DC power
P_{MD}	Maximum power dissipation
p_{best}	Swarm optimization personal best
q	Electron charge
R_s, R_d, R_b	Source, drain and buffer layer resistors
R_c	Contact resistance
R_i, R_{im}	Conventional and modified channel resistance
R_{th}	Thermal resistance
r_0	Output resistance
S_{21}	Forward gain
S_{22}	Output port reflection coefficient

T	Absolute temperature
u_0	Normalized depletion layer width nearer source electrode
u_d	Normalized depletion layer width nearer drain electrode
u_1	Depletion width where carriers attain v_s
$V(x)$	Potential at any point x inside the channel
V_g, V_{gs}	Gate voltage and gate-to-source voltage
V_{gse}	Effective gate-to-source voltage
V_d, V_{ds}	Drain voltage and drain-to-source voltage
V_{dse}	Effective drain-to-source voltage
V_{bi}	Built-in potential
$V_{d(sat)}$	Drain saturation voltage
$V(L_1), V(L_2), V(L_3)$	Voltages at specific location
V_T	Threshold voltage
ΔV_T	Shift in threshold voltage
V_{dsQ}	Optimum V_{ds}
V_{dsmax}	Breakdown voltage
V_P	Pinch-off voltage
v_{max}	Swarm particle maximum velocity
v_{pbest}, v_{gbest}	Swarm particle personal and global best velocity
v_{ij}	Modified velocity of a swarm particle at specific dimension
W, z	Gate width
w_{ij}	Inertia of swarm particle at specific dimension
X	Extension of gate depletion layer
x_p, x_n	Width of depletion layer in p and n-region
x_{min}, x_{max}	Initial and final position of a swarm particle
x_{ij}	Modified position of a swarm particle at specific dimension
$p, N_r, \alpha, \beta, \gamma, \psi, \xi, \lambda, \delta$	Fitting parameters
μ	Electron mobility
μ_{min}	Minimum mobility at degenerate doping levels
μ_{max}	Maximum mobility at intrinsic levels
μ_0	Low field mobility

$\mu(E)$	Field dependent mobility
ε_s	Relative permittivity of SiC
ε_0	Permittivity of free space
Φ_1, Φ_2	Swarm random numbers
η	Drain efficiency
Γ_S, Γ_L	Source and load side reflection coefficient
$\Gamma_{in}, \Gamma_{out}$	Input and output reflection coefficient
υ	Drift velocity
υ_s	Saturation velocity
$\upsilon(E)$	Field dependent velocity
κ	Thermal conductivity
τ, τ_m	Conventional and modified transit time

Chapter 1

Introduction

1.1 Background

Silicon Carbide (SiC) devices have broad spectrum of applications in the field of power electronics and communication due to their unique electrical characteristics. They have large operating temperature range, high breakdown field, high thermal conduction coefficient, high sublimation temperature, high switching speed and are thermally stable [1]. Due to these superior characteristics, SiC devices can comfortably perform in harsh environments, both, in the field of power electronics and communication. SiC based Metal Semiconductor Field Effect Transistors (MESFETs) are capable of operating in S-band and X-band microwave frequencies with significant output power density and power added efficiency (PAE). Because of these superb properties, SiC devices are getting greater attraction in power electronics and in high power microwave industry. SiC MESFETs have outclassed Si based JFETs and GaAs based MESFETs in power electronics. For a given output power, a smaller chip area is occupied by SiC devices than its counter parts, i.e. Si and GaAs [2]. Furthermore, due to high input and output impedances offered by SiC based devices, matching circuitry is easy to design. Also peripheral circuits such as DC to DC converters are simplified for SiC circuitry because it requires smaller cooling systems due to its larger thermal conduction coefficient [3].

TABLE 1.1: Comparison of the performance of GaAs and SiC MESFETs.

Parameter	**GaAs MESFET**	**SiC MESFET**
Breakdown voltage	$\sim 16V$	$\sim 200V$
Operating voltage	$\sim 8V$	$\sim 105V$
$I_{d(sat)}$mA/mm	404	734
Power density (W/mm)	0.78	17.37
PAE	comparable	$> 35\%$
Operating temprature	Low	As large as 500°C (ultimate limit is ceramic packaging)
f_{max} (GHz)	> 200	~ 34
f_T (GHz)	> 100	~ 10
Impedance	Low, on-chip matching	$25 - 50\Omega$ no on-chip matching

On account of poor performance of Si and GaAs MESFETs have been fabricated for microwave applications. Due to unavailability of data for Si MESFET, only comparison of GaAs and SiC MESFETs performance is shown in Table 1.1 [3–7].

1.2 General Properties of SiC

SiC is a semiconductor material having suitable properties for high power, high frequency and high temperature applications. SiC is a wide bandgap semiconductor material with high breakdown electric field strength, high saturated drift velocity of electrons, robust structure, and a high thermal conductivity as compared to many other semiconductors as explained in the Table 1.2 [8, 9]. In this table, E_g is bandgap, ε_s represents relative permittivity, μ is the electron mobility, υ_s represents saturation velocity, E_{crit} is the critical electric field at which breakdown takes place and κ represents thermal conductivity. Additionally, SiC is a

TABLE 1.2: Comparison of average properties of semiconductors.

Material	E_g(eV)	ε_s	μ(cm^2/Vs)	υ_s(cm/s)	E_{crit}(MV/cm)	κ(W/cm.K)
Si	1.12	11.7	1400	1×10^7	0.3	1.5
GaAs	1.40	12.8	8500	1×10^7	0.4	0.5
GaN	3.39	9.00	900	2.5×10^7	3.3	1.3
4H-SiC	3.26	9.66	1000	2.2×10^7	2.0	4.9

hard substance with a Young's modulus of 394 GPa [10]. It is chemically inert and reacts poorly with any known material at room temperature.

The most commonly used poly type of SiC is 4H-SiC, which has a bandgap of 3.265 eV. The wide bandgap made SiC an attractive choice for high temperature electronics fabrication. The breakdown field of SiC is six times higher than Si, making it a natural choice for high power electronics. Therefore, devices fabricated using SiC can operate at much higher voltages and temperatures compared to Si and GaAs.

Drift velocity plays a significant role in the operation of a device especially, when the device is meant for high frequency applications. In SiC, the saturation drift velocity, $\upsilon_s = 2.2 \times 10^7$ cm/sec, which is twice that of Si. A high value of υ_s allows faster communication between the two electrodes needed for microwave applications. Further, an increase in temperature, generally, changes electrical properties of a device, like, mobility of free carriers, μ, drift velocity, υ, etc., which normally affects the device in a negative way. SiC is a thermally stable material relative to its counterparts, therefore, variation in its electrical properties is relatively low. This can be judged by comparing thermal conductivity of SiC with known conductors. For example, thermal conductivity of copper and silver is 4 W/(cm-K) and 4.18 W/(cm-K), respectively [11]; whereas, the value of thermal conductivity for SiC is 5 W/(cm-K) as reported in [12]. A relatively high value of thermal conductivity indicates that SiC devices will allow heat to dissipate quickly thus, keeping intact the electrical performance of the device. Assuming

that lattice temperature of a semiconductor is represented by T, its value depends on the maximum power dissipation, P_{MD} and thermal resistance, R_{th} as given below

$$T = P_{MD} \times R_{th} \ . \tag{1.1}$$

Since, R_{th} of SiC is smaller than its counter parts therefore, under high power operating conditions, low lattice heating is observed. Thus, devices fabricated from SiC require simple, smaller and lighter cooling systems.

Another important factor, which is commonly used to assess the performance of a device is its free carriers mobility. In SiC, electron low field mobility, μ_0 is described as [11]:

$$\mu_0(N_d) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N_d/N_r)^{\alpha}} \ , \tag{1.2}$$

where N_d represents impurity concentration in conducting channel, μ_{min} and μ_{max} are the minimum and maximum mobilities, respectively. N_r and α represent empirical constants. A plot of Eq. (1.2) as a function of N_d for 4H-SiC is shown in Fig. 1.1. This is a typical Fermi-Dirac distribution profile where μ_0 is reducing at higher values of N_d due to increased ionized impurity scattering.

At elevated temperature, the amplitude of lattice vibration increases, causing more obstruction to the flow of carriers thus, reducing μ_0. This requires modification in Eq. 1.2, which leads to a temperature dependent μ_0 defined as [13]

$$\mu_0(N_d, T) = \mu_{min} \left(\frac{T}{300} \right)^{-\beta} + \frac{(\mu_{max} - \mu_{min})\,(T/300)^{-\beta}}{1 + (N_d/N_r)^{\alpha}} \ , \tag{1.3}$$

where T represents temperature in Kelvin and β is a fitting variable whose value is defined in Table 1.3 [13]. Eq. 1.3 shows reduction in mobility by increasing the temperature whose value can be controlled by β at a given temperature.

For a given device, the value of μ is also dependent on the applied electric field, E, which is given by [11]

$$\mu(E) = \frac{\mu(N_d, T)}{\{1 + [\mu(N_d, T)E/\upsilon_s]^p\}^{1/p}} \ , \tag{1.4}$$

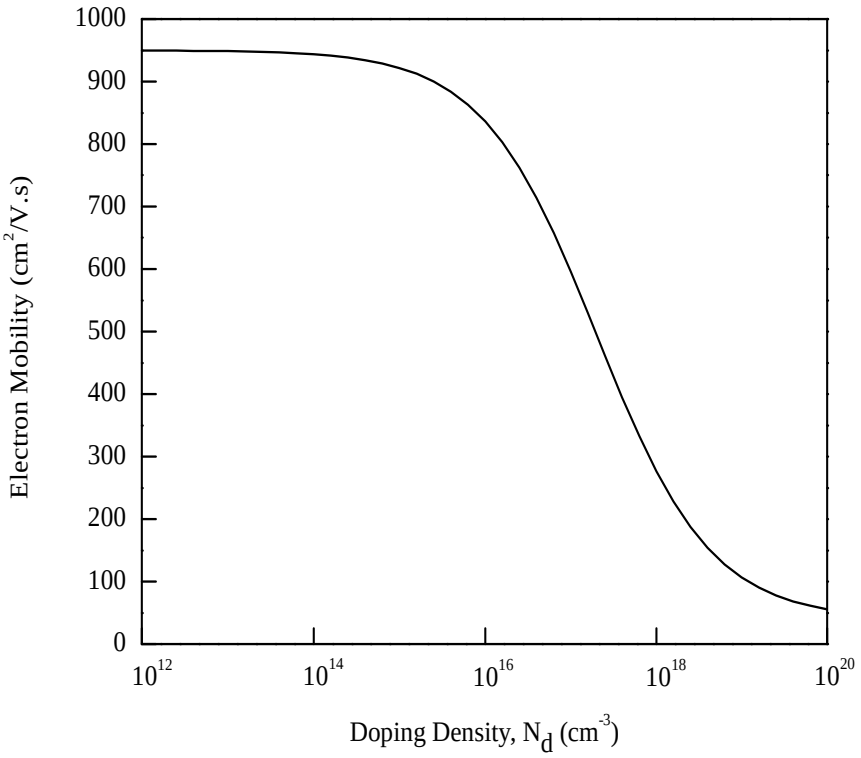


FIGURE 1.1: Mobility as a function of donor impurities.

where p is an empirical constant. Relationship between μ and υ of a device is governed by the expression

$$\upsilon\,(E) = \mu\,(E) \times E\ . \tag{1.5}$$

By assuming the values given in Table 1.3, variation in υ as a function of E at different temperatures is shown in Fig. 1.2. The plot exhibits that pre-saturation υ shows strong dependence on temperature and it decreases with increasing temperature values. This reduction in υ is primarily associated with the reduction in μ at elevated temperature due to increased lattice scattering $\sim 1\times10^{6}$ V/cm. Further, it is also evident from Fig. 1.2 that υ saturates at E commonly known as saturation field, E_s. Majority of figure-of-merits of SiC are based on carrier's mobility and velocity detail of which are given in the next section.

TABLE 1.3: Parameter values for the mobility model of 4H-SiC [13].

Parameters	Value
N_r	9.5×10^{16} cm^{-3}
υ_s	2.2×10^{7}cm/s
μ_{max}	960 cm^2/V.s
μ_{min}	10 cm^2/V.s
α	0.65
β	2.25
p	1.2

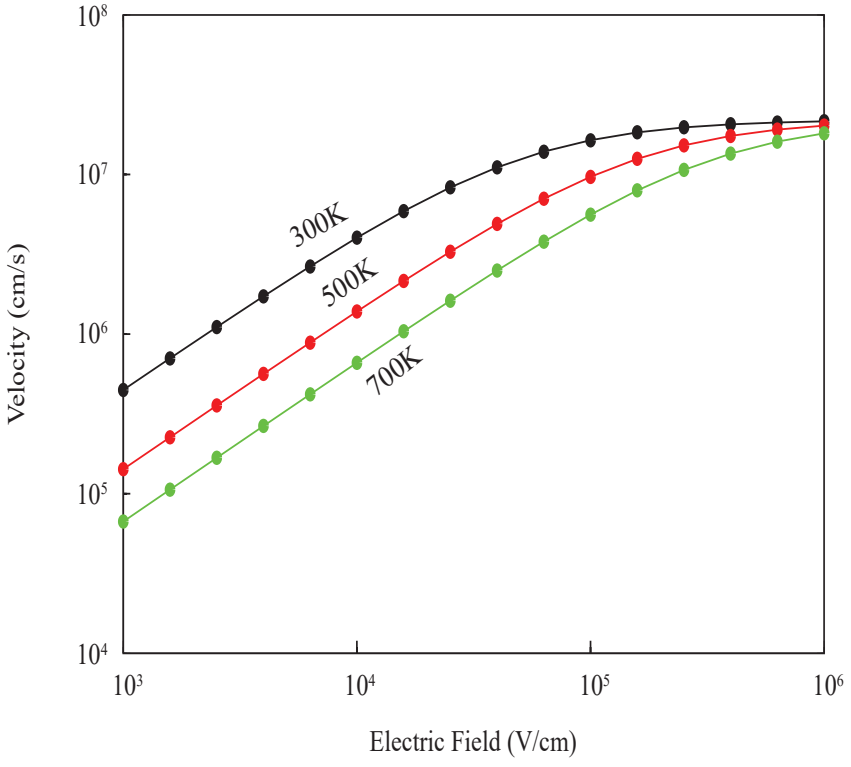


FIGURE 1.2: Velocity as a function of electric field and temperature.

1.3 Figure of Merit

There are several criteria (Figure of Merits) to compare the performance of semiconductor materials and devices, for high frequency and high power applications. Johnson suggested a figure of merit (JFOM), which considers the potential of power handling and high frequency capability of a device. JFOM takes into account E_{crit} and υ_s, as given in the following equation [14]:

$$\text{JFOM} = \frac{E_{crit}^2 \upsilon_s^2}{4\pi^2} \ . \tag{1.6}$$

JFOM does not take into account the material's thermal properties, which are critically important at high power operation, so, Keyes [15] proposed another figure of merit (KFOM), which provides thermal limitation to the switching behavior of transistors used in integrated circuits.

$$\text{KFOM} = \kappa \sqrt{\frac{c\upsilon_s}{4\pi\varepsilon_s}} \ , \tag{1.7}$$

where c represents speed of light in vacuum. Neither JFOM nor KFOM gives any information about power handling capabilities of a device and consequently, Baliga proposed another figure of merit (BFOM) [16], which involves material parameters to address conduction losses.

$$\text{BFOM} = \varepsilon_s \mu_0 E_g^3 \ , \tag{1.8}$$

where E_g is the bandgap of a semiconductor.

Table 1.4 presents a summary of figure-of-merits of SiC relative to Si. It shows that SiC power devices have greater potential in performance over Si and GaAs power devices.

TABLE 1.4: Comparison of figure-of-merits of SiC and GaAs normalized to Si [17].

Figure-of-Merit	Si	GaAs	4H-SiC	6H-SiC
JFOM	1	9	1640	900
KFOM	1	0.41	5.9	5
BFOM	1	22	1840	920

1.4 SiC MESFET

Metal Semiconductor Field Effect Transistor (MESFET) was proposed by Mead [18] and subsequently fabricated by Hooper and Lehrer using GaAs epitaxial layer on semi-insulating GaAs substrate [19]. It has a similar construction and operation as that of Junction Field Effect Transistor (JFET). For the gate terminal, MESFET uses a Schottky junction (metal-semiconductor junction) instead of a PN-junction. It is usually fabricated using compound semiconductors such as SiC, GaAs, AlGaN, InP, etc. and is faster than Si based JFET or MOSFET. A cross-sectional view of a SiC MESFET is shown in Fig. 1.3. It has a lateral structure, where Schottky barrier gate is sitting in a recess. The length (L_g) of the Schottky barrier gate defines the device length; whereas, its width (W) would be the device width. In Fig. 1.3, the epitaxial layer has been etched to define the thickness of the channel, a, which determines the available channel for the flow of current. The electronic current will flow from source to drain; whereas, the conventional current, i.e. drain to source current (I_{ds}) will have the direction of flow from the drain to the source terminals. Both drain and source are ohmic contacts with a high degree of linear response. Separation between gate-source and gate-drain defines the source side and the drain side resistance of the device, respectively. In an operating MESFET, as shown in Fig. 1.3, the drain is at higher potential compared to the source terminal, resulting in a varying drain potential in the channel thus, causing a tapered gate depletion. The substrate, which is used for the fabrication of SiC MESFET is normally of high resistance hence, confining the charge flow within the channel thickness defined by a. The thickness a is chosen as per the

mode of operation of the device and for normally ON devices, it complies with the condition:

$$|V_P| > \frac{qN_d a^2}{2\varepsilon_s} \ , \tag{1.9}$$

and for normally OFF devices, it fulfills the condition defined by:

$$|V_P| < \frac{qN_d a^2}{2\varepsilon_s} \ , \tag{1.10}$$

where q is the electron charge and V_P is the pinch-off voltage. For n-channel devices, typical value of N_d $\sim 3\times10^{17}\text{cm}^{-3}$. To reduce the ohmic contact resistance, usually an additional layer is also used on top of the channel layer with a relatively higher doping $\sim 10^{18}\text{cm}^{-3}$. Fabrication parameters such as L_g, a and W of the device are chosen based on its operation. For high frequency devices, L_g would be of submicron dimension with relatively thinner a. For power devices, to meet the specific power requirements, the value of W is chosen accordingly.

1.4.1 Output Characteristics

An operating MESFET is shown in Fig. 1.3 wherein, the drain-source is biased by a voltage source called V_{ds}, and the Schottky barrier gate is connected with negative terminal of another voltage source referred to as V_{gs}. It is a depletion type device where the channel has got n-carriers and the device can be depleted by gradually increasing the magnitude of V_{gs} to the point where the entire channel is occupied by the gate depletion. At $V_{ds} > 0$, I_{ds} will have a finite value and it will increase linearly by increasing V_{ds} to a certain value of V_{ds} called $V_{ds(\text{sat})}$. When $V_{ds} > V_{ds(\text{sat})}$, the channel carriers attain maximum velocity and, thus, define a current called $I_{ds(\text{sat})}$. Any increase in V_{ds} beyond $V_{ds(\text{sat})}$ will, ideally, have no effect on I_{ds} and, thus, it remains constant ($I_{ds(\text{sat})}$). This naturally defines two distinct regions of $I_{ds}(V_{ds})$ characteristics: the first region is known as the linear region; whereas, the region in which the current is not changing by changing V_{ds} is known as the saturation region.

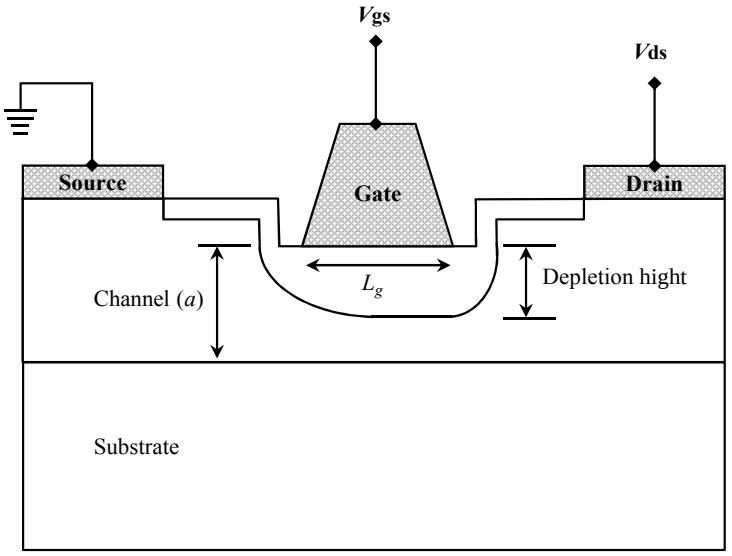
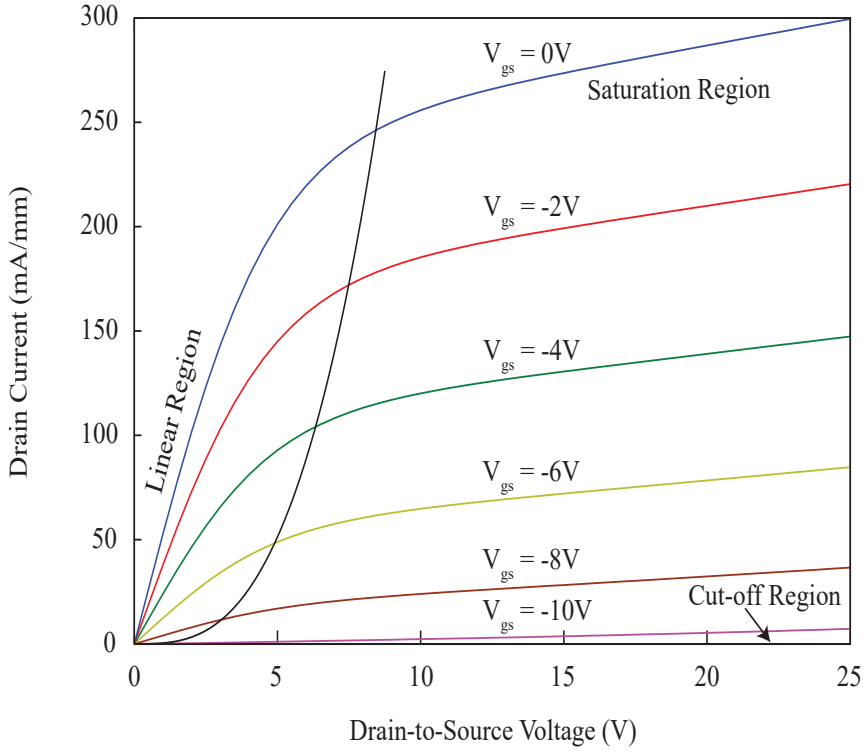


FIGURE 1.3: Cross-sectional view of the schematic of a MESFET.

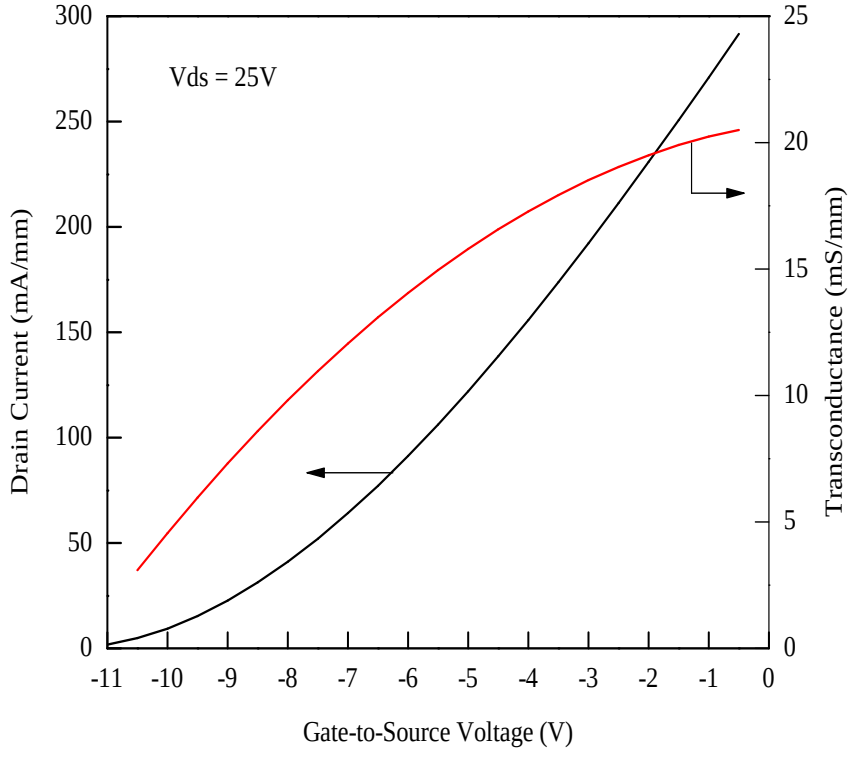
By changing V_{gs} magnitude, the current changes both in the linear as well as in the saturation region thus, defining a family of I_{ds} curves as a function of V_{ds} and V_{gs}. These characteristics are known as output characteristics of a MESFET, as shown in Fig. 1.4(a). This figure clearly shows that by increasing V_{gs} negatively, the maximum value of I_{ds} decreases in the saturation region of operation, and eventually it reaches to the point where the channel is fully depleted and the device reaches the region called cut-off region. For microwave applications, like amplifier design, the device Q-point is chosen in the saturation region of operation, such that there should be no signal cut-off when there is a variation in the input signal at the gate electrode.

It is pertinent to mention here that after the on-set of current saturation, the device usually does not follow the ideal behavior and there is still a finite change in $I-ds$ for $V_{ds} > V_{ds(\text{sat})}$. This leads to a finite output conductance in the saturation region of operation, which is considered a negative feature of a MESFET. In SiC MESFET, the output conductance is inevitable because of the short value of L_g. The output conductance, g_d of a SiC MESFET is defined as

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=\text{constant}} . \tag{1.11}$$



(a)



(b)

FIGURE 1.4: (a) Output and (b) transfer characteristics of a SiC MESFET.

In the saturation region of operation, as a first order approximation, I_{ds} in the saturation region of operation is given by the Shockley's equation

$$I_{ds} = I_{dss}\left[1 - \frac{V_{gs}}{V_P}\right]^2 , \tag{1.12}$$

where I_{dss} is the saturation current at $V_{gs} = 0$V. By changing the geometrical parameters and the device technology, the saturation current can be adjusted as per the design requirements. By and large, I_{ds} depends on the physical parameters of the device: a, W, and N_d. The knowledge of the output characteristics plays an important role in designing the circuits involving SiC MESFETs.

1.4.2 Transfer Characteristics

Transfer characteristics define the relationship between I_{ds} and V_{gs} known as transconductance, g_m of the device, which is given by:

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=\text{constant}} . \tag{1.13}$$

g_m is one of the most important performance parameters for the device, i.e. high value of g_m indicates that the device gain will also be high. Characteristic curves for I_{ds} and g_m in response to the variation in V_{gs} for a submicron SiC MESFET are shown in the Fig. 1.4(b). It is apparent from the two curves that there is a non-linear relationship between the quantities, which can also be seen from Eq. (1.11).

The magnitude of g_m can be increased by making the channel thinner and heavily doped. Thus, for microwave applications, it is always desired to optimize the thickness of the channel in order to achieve the desired output characteristics.

1.5 RF Power Performance

Power amplifiers are the primary consumers of DC voltage source. Therefore, consideration of the amplifier efficiency is of significant importance, specially, in case of hand-held wireless devices. Since, Class-A amplifier is ideally linear in operation, it is therefore preferred in low noise applications. The maximum output RF power of a SiC MESFET, under class-A operation, is computed by

$$P_{(max)} = \frac{\left[V_{ds(\max)} - V_{ds(\text{sat})}\right]\left[I_{ds(\max)} - I_{ds(\text{sat})}\right]}{8} \ , \tag{1.14}$$

$$V_{dsQ} = \frac{V_{ds(\max)} - V_{ds(\text{sat})}}{2} \ , \tag{1.15}$$

$$I_{dsQ} = \frac{I_{ds}\left[V_{ds(\text{sat})}\right] - I_{ds}\left[V_{gs(\min)}\right]}{2} \ , \tag{1.16}$$

where $V_{ds(\max)}$ is the breakdown voltage of the device. Using Eqs. (1.14) to (1.16), one can have a feel about RF performance of SiC MESFET and based on these expressions, an optimum point for the operation of device can be observed for its power performance.

1.5.1 Power Gain

The available power gain of an RF amplifier is defined as:

$$G_A = \frac{\text{Power available from the two-port network}}{\text{Power available from the source}} \ . \tag{1.17}$$

The overall power gain of an RF amplifier depends on the source impedance, the load impedance and the reflection coefficients of the respective ports. The available gain in terms of S-parameters and the circuit reflection coefficients is given by

$$G_A = \frac{|S_{21}|^2\left(1 - |\Gamma_S|^2\right)\left(1 - |\Gamma_L|^2\right)}{|1 - \Gamma_S\Gamma_{in}|^2|1 - S_{22}\Gamma_L|^2} \ , \tag{1.18}$$

or

$$G_A = \frac{|S_{21}|^2\left(1 - |\Gamma_S|^2\right)\left(1 - |\Gamma_L|^2\right)}{|1 - S_{11}\Gamma_S|^2|1 - \Gamma_{out}\Gamma_L|^2} \ , \tag{1.19}$$

where Γ_S is the reflection coefficient looking towards the source, Γ_L is the reflection coefficients looking towards the load, and Γ_{in} and Γ_{out} are the reflection coefficients at the input and output ports of the device, respectively. The above equation can be written as:

$$G_T = G_S \; . \; G_0 \; . \; G_L \; , \tag{1.20}$$

where

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \; , \tag{1.21}$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out}\Gamma_L|^2} = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \; , \tag{1.22}$$

and

$$G_0 = |S_{21}|^2 \; . \tag{1.23}$$

For perfect match, an ideal condition, $G_S = G_L = 1$ and $G_A = |S_{21}|^2$ which is also called matched gain or maximum available gain (MAG). However, the simultaneous matching for input and output terminations and the device respective ports, is seldom achieved. Another metric for rating and comparing the gain of the various devices, operating under stable conditions, is the maximum stable gain (MSG) and is given by:

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} \; . \tag{1.24}$$

As an example, a plot for MAG, MSG and the relative phase between input and output of MSG, for 10W SiC MESFET is shown in Fig. 1.5. The frequency-phase curve shows that the device is stable within the bandwidth.

1.5.2 Efficiency of an RF Amplifier

The drain efficiency η, which is the ratio of RF output power to the DC power, of an amplifier does not give the knowledge about the input power to the amplifier, where the gain of the active device is low. A better measure, which also takes into account the effect of input RF power, is the power-added efficiency (PAE)

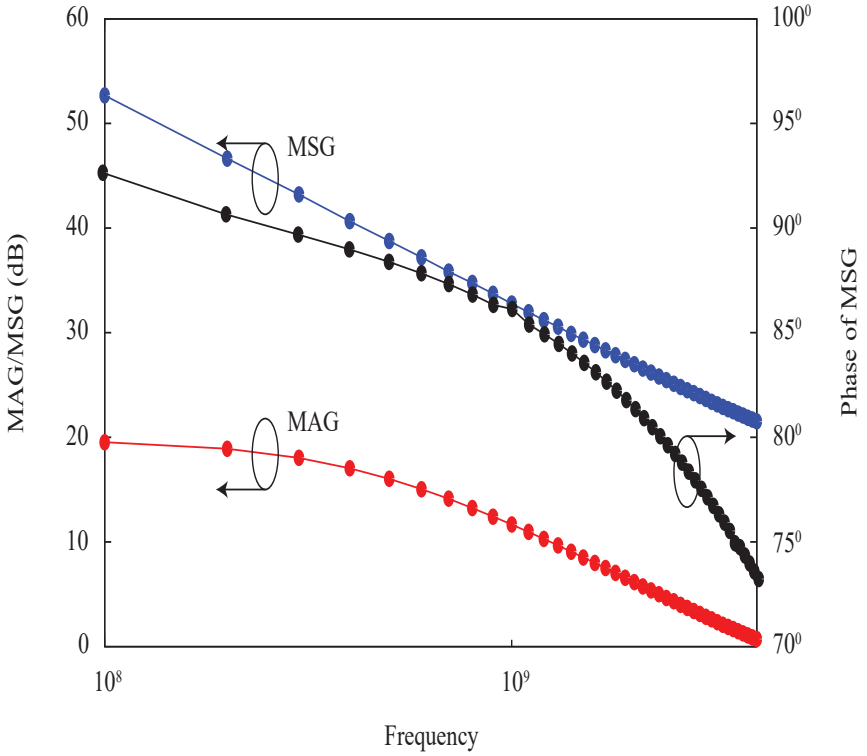


FIGURE 1.5: Plot for MAG, MSG and the phase of MSG for SiC MESFET.

calculated as:

$$\text{PAE} = \frac{[P_{out}]_{RF} - [P_{in}]_{RF}}{[P_{DC}]_{\text{total}}} = \left(1 - \frac{1}{G}\right)\eta \ , \tag{1.25}$$

where $\eta = [P_{out}]_{RF} \,/\, [P_{DC}]_{\text{total}}$ is the drain efficiency and $G = [P_{out}]_{RF}\,[P_{in}]_{RF}$ is the RF gain of an amplifier. PAE is a function of frequency and drops with its increasing values. A plot for RF gain, output power and PAE of an RF amplifier, designed using 4H-SiC-MESFET [4], is shown in the Fig. 1.6.

1.6 SiC MESFETs Applications

SiC MESFETs, due to their unique material characteristics, are highly preferred devices for high power RF applications, especially those where large bandwidth is required. These devices exhibit a mean failure time in excess of 500 hours at a junction temperature of 410°C [20]. There are numerous companies, which are commercializing SiC MESFETs and their RF modules for high temperature electronics and communication related applications. Power handling capability

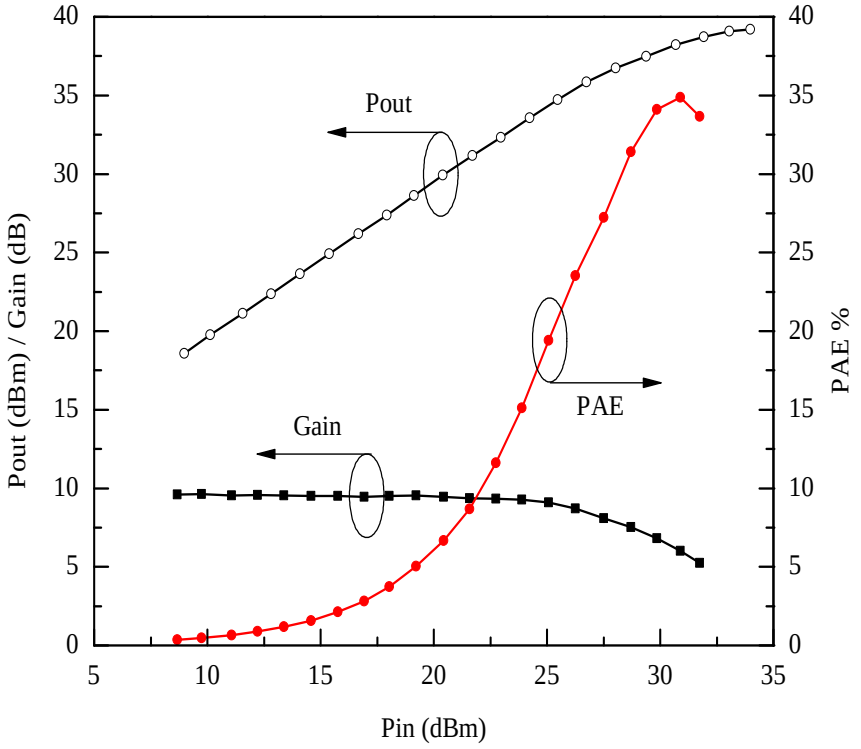


FIGURE 1.6: Power performances measurement at 2 GHz of a 4H-SiC MESFET.

of SiC MESFETs is as high as ∼7.8 W/mm [21]. The PAE for such devices is ∼70% for class AB configuration. Under such a configuration, these devices are used in military aircrafts, powerful microwave electronics, radar, air traffic control, satellite communications and cell phone base stations.

Faster switching speed coupled with high thermal conduction with no additional requirement of cooling systems made these devices a natural choice to be used in hot and harsh environments; in automotive, aerospace and deep-well drilling industries.

By employing SiC MESFET technology, the size and the cost of the power conversion and distribution systems have been greatly reduced [8, 9, 22, 23]. From green energy perspective, SiC devices have relatively lesser issues associated to global environment. These devices, because of reduced power conversion losses and less heat dissipation, have also created a significant impact on power electronics sector, solar cells, electric cars and power converters, etc. [2]. Today, we have SiC based lamps and tube rods, which are replacing the conventional technologies.

SiC integrated circuits (ICs) are also under investigation and many SiC based ICs have been fabricated. High-power SiC MMIC amplifiers have also been demonstrated with excellent yield and reliability. These MMIC amplifiers showed power performance characteristics not previously available with conventional GaAs technology [24, 25]. In general, one can say, that SiC ICs brought a major improvement in power systems, especially those meant for harsh environments, such as radar, cellular communication towers, sensors and control electronics, etc. [26, 27].

1.7 Motivations

As mentioned earlier, SiC MESFET devices have scores of applications in the field of RF engineering and thus can comfortably operate at X-band and S-band with significant output power, PAE and other benefits. Design and optimization of SiC MESFET based RF components depend on the degree of accuracy of the modeling of the device. Therefore, SiC MESFET's modeling is a hot area for the researchers to realize enhanced performance of RF systems involving SiC MESFETs.

Many models for MESFETs are reported in the literature; but a few of them are specifically developed for SiC MESFETs [28–31]. The accuracy and validity of these models are based on the device dimensions and their global validity cannot be guaranteed, especially for the devices having submicron L_g. Thus, a comprehensive model which should cover a wide range of SiC MESFETs design with an acceptable accuracy, is still a requirement of design engineers.

As mentioned before, the performance of a SiC MESFET depends on its physical parameters such as L_g, a and N_d, substrate and buffer layers thicknesses etc. An accurate analytical model, based on the closed form expressions, with improved channel potential understanding would provide a better explanation about the device response, especially at high biasing. By employing the gathered information, the device physical parameters can be further optimized to achieve enhanced performance. Due to the unique characteristics of SiC MESFETs, caused by self

heating and high biasing, an improved analytical model is also required to use the device to its fullest potential.

SiC MESFET intrinsic small signal parameters play a crucial role in determining the RF response of the device. A straight forward technique to assess the intrinsic small signal parameters is lacking, which could be employed to have the initial assessment to answer how the device would respond when subjected to RF applications? It would be, therefore, beneficial to have the assessment of the device intrinsic small signal parameters using its assessed DC characteristics. Such a technique would be relying on the accuracy of the DC model employed, followed by the assessment of the device AC parameters. We would like to established an AC parameters assessment technique based on SiC MESFET DC characteristics to develop its AC equivalent circuit.

1.8 Thesis Outline

This thesis presents analytical and semi-empirical modeling of SiC MESFETs meant for high power microwave applications. Techniques have been developed to predict the response of submicron SiC MESFETs by evaluating channel conditions and material parameters. Small signal parameters are evaluated by using DC characteristics of the device. The techniques developed in this thesis can potentially be employed in simulation tools of high power microwave MESFETs involving submicron devices. The remaining organization of the thesis is as follows:

Chapter 2: This chapter summarizes the current state of SiC MESFET technology. It presents SiC MESFETs characteristics and their applications in high power industry. Progress made so far in the device design to get improved performance is presented. The device potential for high power microwave communication systems is highlighted. Stable performance, which the device can offer at high ambient temperature and in radiation rich environment is discussed. The work reported by different research groups about SiC MESFETs' power requirement along with superior linearity characteristics in microwave amplifiers is explored. It is shown

that owing to relatively better thermal conductivity, SiC MESFETs provide superior conduction of heat generated under high power operating conditions thus, maintaining their stable performance.

Novel structures of SiC MESFETs, which are reported in the literature to improve the device power handling capabilities and to increase its f_T and f_{max} operation are also discussed. While reviewing the device current state of technology, physical parameters used to improve g_m and g_d of the device are explored.

To determine the fullest capacity of the device and to know its physical behavior, simulation and modeling techniques are usually employed. Analytical, empirical and semi-empirical models developed for SiC MESFETs and their origins are discussed. A need of a comprehensive model is established to predict DC characteristics. Moreover, it is discussed that an accurate AC model is needed to predict intrinsic small signal parameters of the device designed for microwave power applications.

Chapter 3: This chapter presents a detailed mathematical model describing $I-V$ characteristics of submicron SiC MESFETs. Poisson's equation with appropriate boundary conditions is solved to determine potential distribution inside the channel. Location of the Schottky barrier gate, where the carrier's velocity gets saturated is evaluated. The finite output conductance in the saturation region of operation, which is usually observed in submicron devices is explained with Schottky barrier depletion layer modification. $I-V$ characteristics of submicron SiC MESFET are modeled and compared with the conventional velocity saturation technique, where the depletion layer after the onset of current saturation is treated as constant.

Chapter 4: This chapter presents a comparative analysis of semi-empirical DC models of SiC MESFETs and their degree of validity/accuracy to a number of submicron devices by employing Particle Swarm Optimization (PSO) technique. An improved model is presented to simulate DC and pulsed $I-V$ characteristics of SiC MESFETs. The validity of the model is demonstrated by applying it on submicron devices, especially designed for power applications. A comparative

analysis is carried out by employing PSO technique. Moreover, in this chapter, expressions are developed to simulate g_d and g_m of the device. Based on the simulated characteristics, parameters defining the device geometrical structure are estimated to a good degree of accuracy.

Chapter 5: This chapter reports a technique to assess AC small signal parameters of submicron SiC MESFETs using its DC characteristics. Effects caused by self heating and high transverse electric field on the device characteristics, especially when channel length is reduced to submicron regime are discussed in this chapter. It is shown that the conventional models used to assess FET devices, meant for low voltage operation, loose their accuracy in predicting small signal elements of a microwave SiC MESFET. Thus, there is a need to establish a technique, which can predict small signal elements of submicron SiC/GaN MESFETs, which are specially designed to operate under harsh environment and at high temperatures. A set of expressions is developed to assess small signal elements of SiC MESFETs and their validity is demonstrated.

Chapter 6: This chapter presents the conclusion drawn from this research and provide suggestions on possible future extension of the work.

Chapter 2

Literature Review

2.1 Introduction

SiC is a wide band-gap material with large breakdown field, high saturation velocity, and large thermal conduction. SiC MESFETs can operate at high voltage and have high thermal robustness with large output resistance relative to other semiconductors such as Si, GaAs MESFETs and GaN HEMTs. SiC MESFETs are good candidates for high power microwave applications even in harsh thermal environments because of many superior electrical characteristics such as high mobility, high breakdown voltage, low series source (R_s) and drain (R_d) resistances, and high power density, etc [32]. Furthermore, SiC MESFETs are thermally stable devices and exhibit a maximum of 10% change in their electrical parameters when operated at 500°C and over the course of 500 hours in an air ambient [33]. The maximum temperature range to which SiC MESFETs can operate is limited by the ceramic packaging. Reliability of SiC MESFETs is a well established fact thus, they are well suited for high temperature applications [34]. Although, GaN devices exhibit similar properties, but SiC has two main advantages over GaN. The first one pertains to high thermal conductivity of SiC; and the second one offers both bulk and surface conduction devices. Of the three materials, Si, GaAs, and SiC, the last one offers highest absolute power density due to large breakdown voltage

[5]. Therefore, SiC MESFETs are very attractive for microwave applications such as transmitters and RADAR. Development made so far has been summarized in a tabular form and is given in Table 2.1.

2.2 RF Power Performance

Use of SiC MESFETs in RF applications has frequently been discussed in the literature. Song et al. [41] fabricated 4H-SiC MESFETs on a conducting SiC substrate and the fabricated devices exhibited unity gain frequency, $f_T = 3.2$GHz, maximum operating frequency, $f_{max} = 12.4$GHz, an RF power gain of 5.9dB, and a maximum output power of 25.3dBm (0.85W/mm) at 2GHz, which is much higher than Si and GaAs equivalent size transistors. They observed that the devices offered low breakdown voltage and degraded RF power due to the leakage in the conducting substrate. Sadler et al. reported a 30 watts output power from a single 12mm SiC transistor under pulsed-mode conditions in X-band [42]. For small (250μm) devices, they also reported output power of 5.2W/mm at 3.5GHz and 4.5W/mm at 10GHz.

H. Chen et al. fabricated 4H-SiC MESFET having 4×20mm total gate width. The pulsed (300μs, 10%) output power, gain and power-added efficiency (PAE) of the internally-matched device measured at 2GHz were 250W, 10.5dB, and 30%, respectively [43]. S. Sriram et al. [44] fabricated SiC MESFETs by using source connected field plates (FPs) and demonstrated maximum stable gain (MSG) exceeding 15.7dB at 3.1GHz in a Class-AB bias condition, and RF output power density greater than 4W/mm was achieved. H. Jia et al. [45] designed 4H-SiC microwave MESFETs using n-shielded, buried channel and field plate; to improve DC and RF performance. Experimental results showed a relatively broad and uniform transconductance (g_m) versus gate voltage using a 0.1μm n-shielding. The resultant device showed 5.27W/mm power density, 6.7dB power gain and 43% PAE at 2.3GHz under pulse operation.

TABLE 2.1: SiC development history

Year	Development	Author	Reference
1977	Muench fabricated first SiC MESFET with g_m = 1.75mS/mm	Muench	[35]
1987	SiC MESFETs with g_m of 1.6 and 2.3mS/mm	Kong,	[36]
		Kelner	[37]
1991	α-SiC MESFET with g_m of 47mS/mm, PAD and PD of 23.4% and 4W/mm, respectively	Trew	[1]
1993	SiC MESFET with 2W/mm at 1GHz and f_T =7GHz	Driver	[38]
1994	S-Band operation of SiC power MESFET with 20W output power, 4.4W/mm PD and 60% PAE	Henry	[24]
1995	SiC MESFET with g_m, f_{max}, f_T, PD, and PAD of 42mS/mm, 12.9GHz, 6.7GHz, 2.8W/mm and 12.7%, respectively	Weitzel	[5]
1995	Two region analytical model of SiC MESFET	Tsap	[28]
2002	S-band 4H-SiC MESFETs with PD of 5.6W/mm and 36% PAE, and 80 W(CW)with PAE of 38%	Clarke	[3]
2004	Electrical operation of 6H-SiC MESFET at 500°C for 500 hours in air ambient	Spry	[33]
2006	SiC MESFET with PD of 7.8W/mm at 3GHz, PAE 70% at Class-AB bias.	Andersson	[21]
2006	A three-region analytical model for short-channel SiC MESFETs	Zhu	[30]
2016	A comprehensive semi-empirical model for SiC MESFETs	Riaz	[39]
2017	Analytical model for submicron SiC MESFETs	Ahmed	[40]

Wojtasiak et al. [46] designed and fabricated a 100W high power L-band amplifier for active phased-array radar (APAR) by using two 60W SiC MESFETs. The package temperature increased from 60°C to 140°C. The output power dropped to 0.5dB and the rise in temperature was over 140°C, which damaged the ceramic transistor package.

S. Sriram et al. [47] fabricated ion-implanted SiC MESFETs and evaluated their DC and RF performance which were comparable to that of epitaxial-channel devices. The fabricated MESFET with a gate length, L_g of 0.4μm showed MSG $\sim$ 15.7dB at 3.1GHz in class-AB bias conditions. In RF power operation at 3.5GHz, an output power of 4.1W/mm with a PAE $\sim$ 63%, and a linear gain of 15.9dB were obtained.

Niclas et al. [48] successfully fabricated and measured two types of SiC MESFETs with different epistacks having different doping and the devices were scaled both vertically and laterally. Improvements were shown using a thinner heavily doped channel layer. DC and AC measurements were used to assess the performance and their results were either matching or in some cases better than what have been reported by other groups. An increase in f_T and f_{max} of 27% and 18%, respectively, were obtained for SiC MESFETs having higher channel doping.

Deng et al. [49] fabricated SiC microwave MESFETs by using a standard structure but with multi-recessed gate. The multi-recessed gate structure proved to be effective in increasing the output power due to increased breakdown voltage. A SiC MESFET with 250mm gate periphery biased at a drain voltage, V_{ds} = 65V demonstrated a pulsed wave saturated output power of 2.24W with a linear gain of 8dB at 2GHz. RF power output greater than 8.9W/mm was also achieved, indicating that a SiC MESFET with a multi-recess gate is a promising structure for high-voltage devices for their potential use in high-power solid-state amplifiers.

Tao et al. [50] fabricated 2×30mm high-power SiC MESFETs. By load-pull testing at 1.5GHz and at V_{ds} = 48V, they reported output power of 107W, PAE 48.1%, and a gain of 10.3dB under continuous wave RF operation. They also reported

TABLE 2.2: RF Power Performance of submicron SiC MESFETs.

$L_g(\mu m)$	W (μm)	PD(W/mm)	f_{max}(GHz)	f_T(GHz)	$PAD\%$	Reference
0.3	200	1.8 CW	33	11.3	-	[6]
0.4	400	7.8 CW	21.2	9.9	70	[21]
0.5	400	0.85	12.4	3.2	34.5	[41]
0.6	200	7.8 CW	25.5	8.7	40	[53]
0.7	100	5.27	18.8	8.2	43	[45]
0.8	250	8.9	-	-	30	[49]

that 1mm SiC MESFETs exhibited 35dBm output power, PAE greater than 55%, and a gain of 12.3dB under continuous RF operation at 1.5GHz and at $V_{ds} = 48$V.

R. Thakkallapally et al. [51] analyzed the performance of a unidirectional normally-on 3C-SiC/Si power MESFET. Electrical analysis showed that the drain current of this device was 100% higher than a lateral device of the same dimension, while occupying 33% less area compared to a lateral device. Their study showed that at $V_{gs} = 0$V, the drain current, $I_{dss} = 600$ mA/mm; the breakdown voltage reached to 600V, and the critical breakdown electric field increased to 3.9×10^6 V/cm. Thermal analysis was also conducted using Si substrate as a heat sink at $T = 300$K. Drain current was set 600mA/mm and $V_{ds} = 600$ V. Results showed that highest surface temperature, due to self-heating, did not exceed 312K.

M. Alexandru et al. [52] developed a new 4H-SiC planar-MESFET for high density ICs integration using a typical Si CMOS layout approach. ICs scalability requirement was demonstrated at room as well as at higher temperatures. They also fabricated high density SiC based ICs having three different metal levels (the transistor's electrodes metal plus the two thick interconnection metals) demonstrating a fabrication flow similar to that of a Si-CMOS process. Their fabrication paved a way for high power SiC based ICs for RF applications. Table 2.2 shows RF performance of SiC MESFETs as a function of L_g and W.

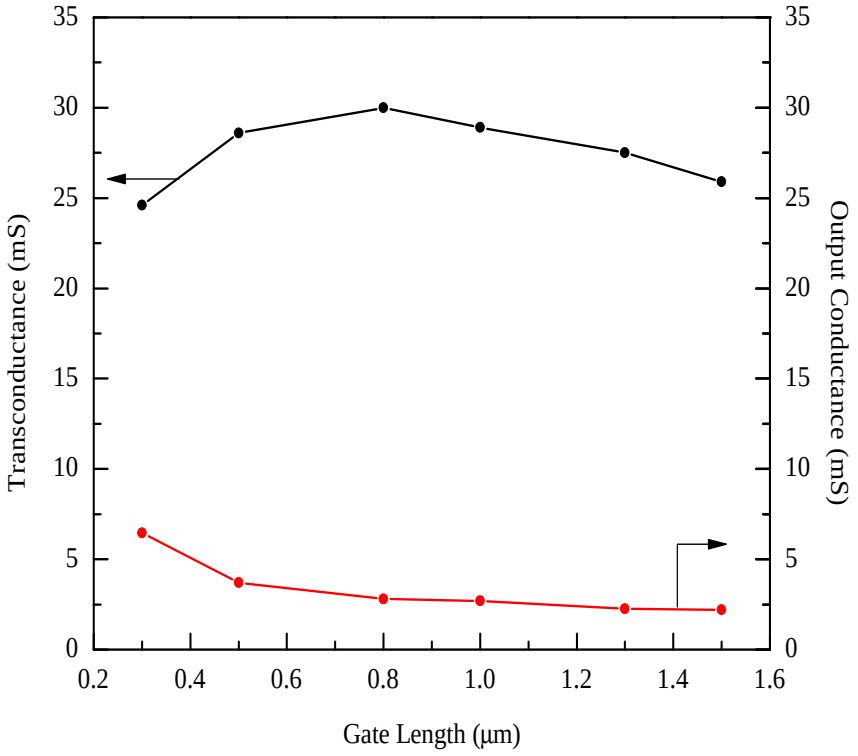


FIGURE 2.1: g_m and g_d as function of L_g.

2.3 Short Channel Effects

RF performance of a MESFET depends on its L_g and saturation velocity, υ_s of its carriers. With reduction in L_g, an obvious benefit is an increase in f_T. However, when L_g is less than 1μm, the device suffers from short channel effects and performance of the device is degraded [54], which included reduction in g_m and an increase in g_d of the device as shown in Fig. 2.1 [6]. The figure shows that g_m increases from 25.9 to 30 mS mm^{-1} as L_g decreases form 1.5 to 0.8μm and decreases from 30 to 24.6 mS mm^{-1} as L_g decreases from 0.8 to 0.3μm. The figure also indicates that g_d increases from 2.2 to 6.45 mS mm^{-1} as L_g decreases from 1.5 to 0.3μm.

In short channel devices, the horizontal electric field becomes stronger and even at smaller drain biasing, the mobility of carriers starts to reduce. Young et al. [55], in their study of transport characteristics of SiC MESFETs, reported that υ_s and the low field mobility, μ_0 of the carriers are 1.7×10^7 cm/s and 300 cm^2/Vs, respectively, which are smaller than previously reported values.

TABLE 2.3: Power density for gate width of 100, 200, 400 μm SiC MESFETs [2].

$L_g(\mu$ m)	$W = 100$ μm	$W = 200$ μm	$W = 400$ μm
0.3	1.64	1.88	1.86
0.5	1.82	1.96	2.27
0.8	1.83	2.38	2.13
1.0	1.36	2.32	2.22
1.3	1.27	1.84	1.87
1.5	1.14	1.70	1.80

Another important short channel effect is drain induced barrier lowering (DIBL). Primarily, Schottky barrier depletion layer is controlled by the gate biasing. However, with increased drain biasing, there is an enhancement in charge layer accumulation near the drain-side of the gate. These charges create their image charges in the gate electrode, as a result, there is a reduction in the magnitude of gate potential, which reduces Schottky barrier called as DIBL. In short channel devices, this effect becomes more prominent and leads to an increase in g_d.

Furthermore, in short channel devices, carriers become hot due to high field available in the channel and get diverted towards the substrate, resulting in large substrate current. Honda et al. [6] and Manabu et al. [2] in their respective investigations of short channel effects, observed that when L_g is less than 1μm, gate loses its control over the channel current due to DIBL. As a result, f_T and f_{max} started to saturate and at $L_g \sim 0.3\mu$m, they were even less than the maximum values as shown in Fig. 2.2. They also observed that g_d increases and V_T shifts towards more negative values to pinch off the channel. Moreover, V_T also became strong function of V_{ds} and increases with its increasing values. Furthermore, power density (PD) also starts to reduce by decreasing the gate width as evident from Fig. 2.3.

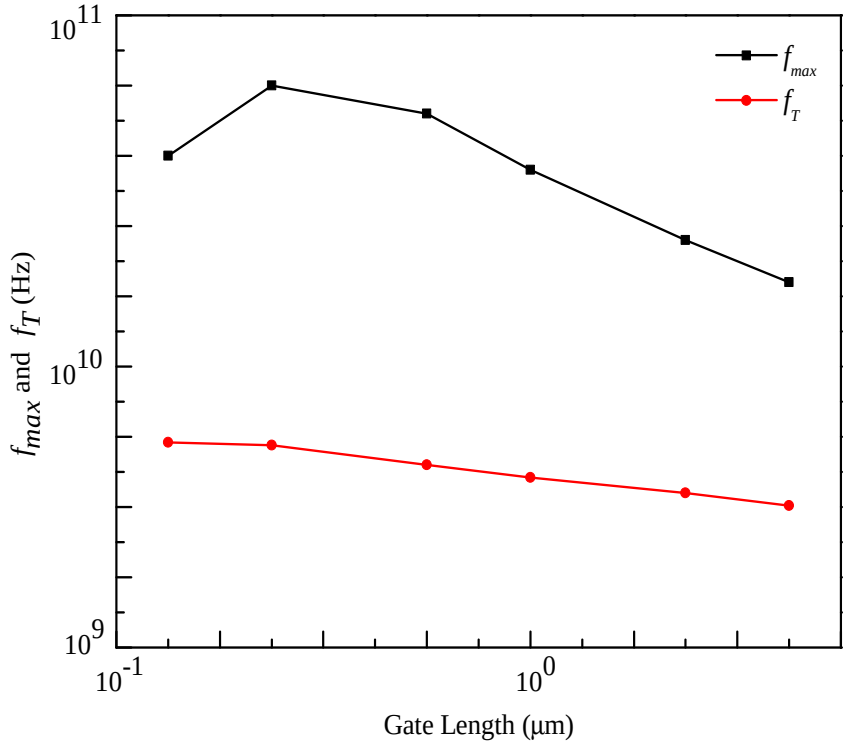


FIGURE 2.2: f_{max} and f_T as a function of L_g.

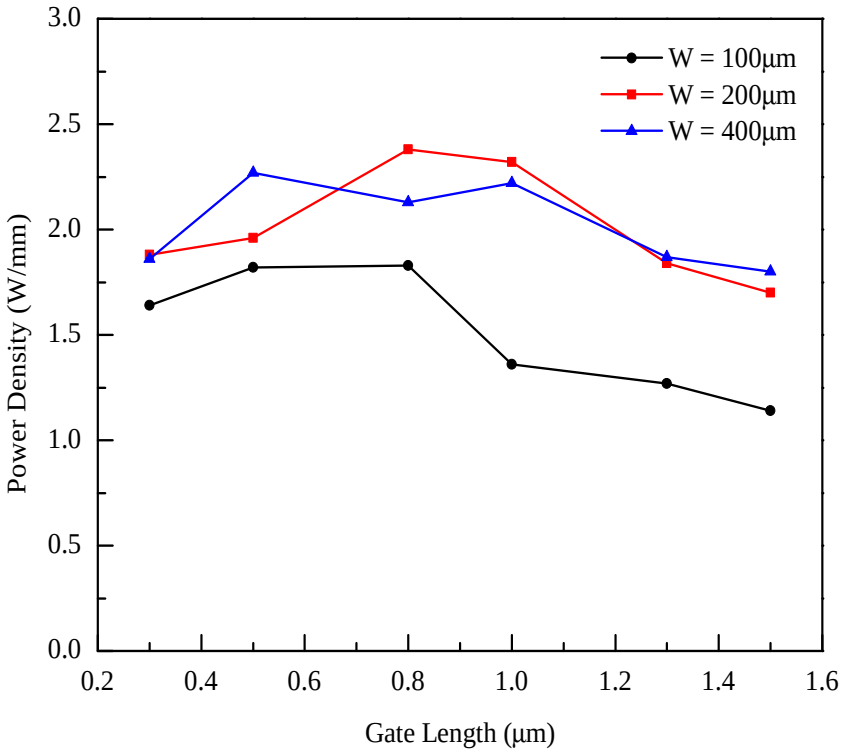


FIGURE 2.3: Power density as a function of L_g and W.

2.4 Effects of Buffer Layer

Short channel effects can be controlled to some extent by optimizing device fabrication parameters. Rorsman et al. [56] used thin highly doped p-type buffer layer in their devices which resulted in reduction in short channel effects. They reported an increase of 20% and 25% in f_T and f_{max}, respectively, and a 12% increase in output power. This is a significant improvement compared to lightly doped thick buffer layer [6]. Hyuk et al. [54], in their experiment, with SiC MESFETs, also demonstrated that short channel effects can be reduced with shallow rather than deeper channel doping. Thus, further optimization of SiC MESFET's physical parameters is required, together with more lateral scaling to improve its output power, PAE and high frequency performance.

Song et al. [41] fabricated SiC MESFET and investigated effects of p-type buffer layer grown between n-type channel and conducting substrate. They demonstrated that a heavily doped p-type buffer between the channel and the conducting substrate reduces the parasitic substrate current, thus, increases output power. They also reported that if the buffer layer thickness is increased from 2.2 to 6μm, the breakdown voltage increases from 38V to 275V.

2.5 Trapping and Substrate Effects

SiC is a wide-band gap material such that the vast majority of recombination events are indirect via recombination levels (trapping centers) in the band gap. The resulting energy loss by recombination, as a heat, is given up to the lattice. Any impurity or impurities and lattice defects can serve as recombination centers if these are capable of receiving a carrier of one type and capturing a carrier of opposite type as shown in Fig. 2.4.

Trapping effects are known to come either from surface traps or from substrate traps and create instability in I_{ds}. Also, traps influence the power performance through the formation of quasi-static charge distributions on the wafer surface, in

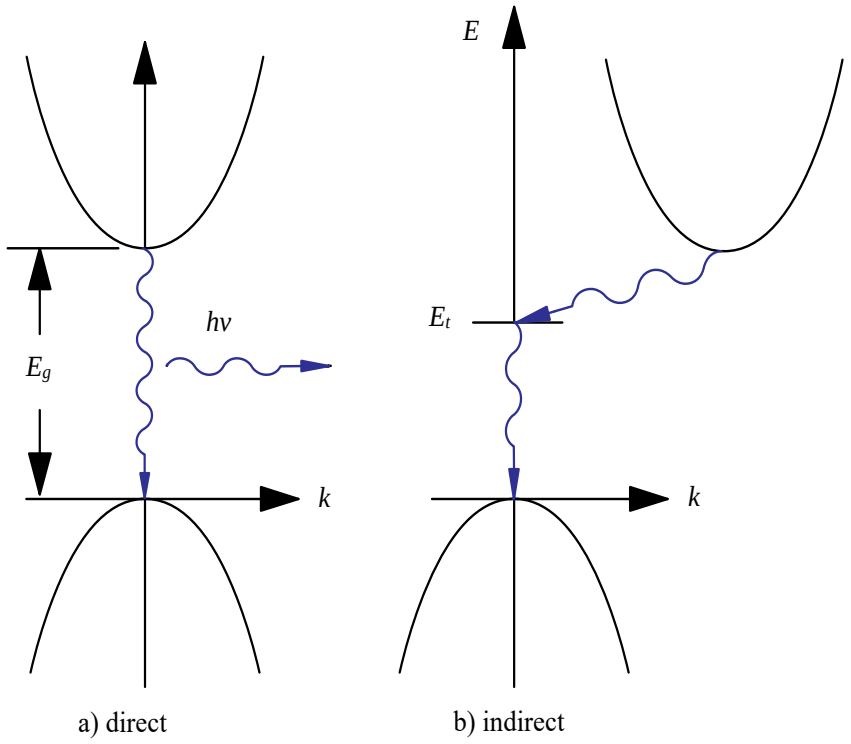


FIGURE 2.4: Direct and indirect transition in semiconductor (a) Direct transition with emission of photon, (b) Indirect transition via defect level.

the buffer layers underlying the active channel or in the substrate. The accumulated parasitic charge acts to limit I_{ds} and voltage swing, thereby restricting the high-frequency power output [57–59].

Hjelmgren et al. [60] compared measured and simulated transient characteristics by taking into account effects of self-heating, gate tunneling, substrate and surface traps. They found that inclusion of bulk traps even for high-purity semi-insulating substrate resulted in good agreement with measured drain lags. They also demonstrated that by reducing the occupation of near interface traps, it is possible to obtain a good agreement between measured and simulated characteristics. Andrei [61], in his experiment, demonstrated that trapping takes place at the acceptor layer of the substrate in the devices with and without buffer layer. Asmi et al. [62] investigated the impact of traps and self-heating on the performance of SiC MESFETs, meant for microwave applications. Their results showed that an increase of trap concentration from 10^{14}cm^{-3} to 10^{16}cm^{-3} reduces f_T by $\sim$ 40%, and an increase in the temperature by $\sim$ 50K above the room temperature reduces f_T by $\sim$

45%. Siriex et al. [63] investigated trapping effects in power SiC MESFETs using pulsed DC and AC measurement systems and reported that major contribution comes from substrate (buffer) traps which are sensitive to V_{ds} and cause reduction in RF power. Sankha [64] reported an analytical model for SiC MESFET by incorporating trapping and thermal effects. In his study, he stated that trapping and detrapping from the surface, control the channel opening at the drain-end, thus causing the drain resistance to be gate and drain voltage dependent. He also reported that a significant reduction in trapping phenomenon is observed in the devices having thicker buffer layers.

S. Mitra et al. [65] fabricated MESFETs by ion implantation using nitrogen source on a bulk semi-insulating 4H-SiC substrate and measured g_m and frequency dispersion to observe bulk and surface traps in the channel region. Five traps were recorded in the energy range of 0.18-0.65eV. Traps at 0.52eV and 0.65eV were the bulk traps in the channel region. The three traps at 0.4, 0.3 and 0.18eV were surface traps found at ungated surface region. Henry et al. [24] fabricated SiC MESFETs using an undoped-spacer-layer on top of the channel, forming a buried-channel structure, which stopped the induced surface states to approach the conducting channel. As a result, RF dispersion got reduced with relatively broad and uniform g_m. M. Gassoumi et al. [66] performed conductance deep-level transient spectroscopy (CDLT) to obtain the information about the traps of 4H-SiC MESFETs. Two unexpected hole-like traps, one with activation energy of 0.9eV and second with activation energy of 0.56eV were observed in the spectra. Thus, investigation of the traps, their causes and minimization still requires the attention of researchers for better performance of the device.

H J. Na et al. [67] fabricated 4H-SiC MESFETs by employing an ion implantation process instead of recess gate etching technique and reported $I_{dss} = 500$mA/mm, $g_m = 41$mS/mm and $f_T = 9.3$GHz. The reported MESFETs were free from drain current instability, which is usually observed in SiC MESFETs due to trapping effects. They observed that drain current recovery characteristics were also improved by passivating the surface with thermally evaporated oxide layer, which minimizes the surface traps.

Song Kun et al. [68] proposed a novel SiC MESFET structure having buried gate and p-type spacer layer on top of the channel to suppress surface traps and to reduce gate-drain capacitance, C_{gd}. Simulation results showed relatively smaller frequency dispersion and reduced current instability. The gate lag ratio (ratio of I_d transient to I_d quiescent) showed improvement and it was close to 90% at V_{ds} = 20V. C_{gd} also showed reduction up to 17.8%, and improvement in f_T and f_{max} was also shown.

Deep levels in semiconductors can act as carriers traps, which increase the resistance of the sample. They can also act as a recombination centers limiting the carriers life time. Deep levels in 4H-SiC are called as life time killer. K. Kawahara et al. [69] investigated deep levels in n-type 4H-SiC epilayer. They employed different techniques to study deep level defects in the same samples. They showed that deep levels were the dominant defects responsible to degrade the device performance.

2.6 Frequency Dispersion in SiC MESFETs

Frequency dispersion of a parameter is a variation in its intrinsic value with respect to the frequency. Ideally, intrinsic parameters of a device should be independent of frequency, in a desired frequency band, for satisfactory performance. When bulk traps are present in the gated region of the channel, their occupancy and hence the depletion width, under the gated channel region, becomes frequency dependent. As a result, g_m and the gated channel resistance (R_i) also become frequency dependent. AC signal at the gate, modulates the gate-source and gate-drain leakage current, which in turn also modulates the occupancy of surface states in the ungated gate-source and gate-drain channel regions. In SiC MESFETs, like GaAs, low frequency dispersion in their output and transfer characteristics is observed, which can cause errors in power and efficiency computation in an RF power amplifier design.

Sghaier et al. [70] compared MESFETs fabricated on a highly V-doped Si substrates versus low-metal-content substrate. The static output characteristics measurements as a function of temperature were performed along with frequency dispersion of g_m and g_d. Results gave clear evidence of the presence of deep traps having an activation energy of 1.05eV in V-doped substrates. These traps have a capture cross-section between 10^{-18} cm^{-2} to 10^{-19} cm^{-2}. They suggested that the easiest way to suppress these parasitic effects is to use high purity Si substrates.

Deng et al. [71] performed a two dimensional AC and transient analysis to investigate effects of surface traps on the frequency dispersion of g_m in SiC MESFETs. The simulation results showed that g_m exhibited negative frequency behavior. The presence of acceptor traps, acting as electron traps on the surface have been identified as an important cause of current degradation in SiC MESFETs.

H. Lu et al. [72] presented a comprehensive model describing traps properties and their influence on SiC MESFETs frequency characteristics. The frequency dispersion of g_m and R_i were analyzed in detail by considering the gate and the drain biasing. They found that traps located at buffer and substrate are the main cause of frequency dispersion in SiC MESFETs.

2.7 Threshold Potential (V_T)

A constant V_T and low g_d are desirable parameters for a microwave SiC MESFET. But for short-channel devices, V_T is a function of L_g and V_{ds}. Gate-length to channel-thickness ratio, L_g/a should be large enough to make V_T independent of L_g and V_{ds} as shown in Figs. 2.5 and 2.6 [2]. This is possible only when a is reduced for short channel devices, but to meet the target I_{ds} and to maintain g_m, the doping of the channel ought to be increased.

Rusli et al. [73] fabricated thin channel SiC MESFETs with increased doping and demonstrated that V_T is almost independent of V_{ds}. Their devices had $L_g =$

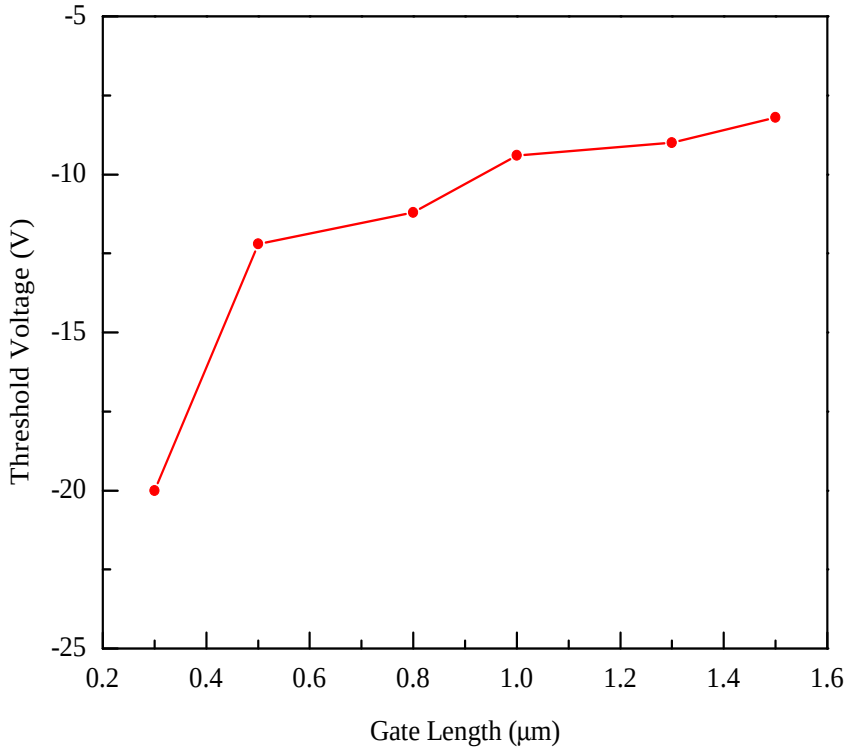


FIGURE 2.5: V_T as a function of L_g.

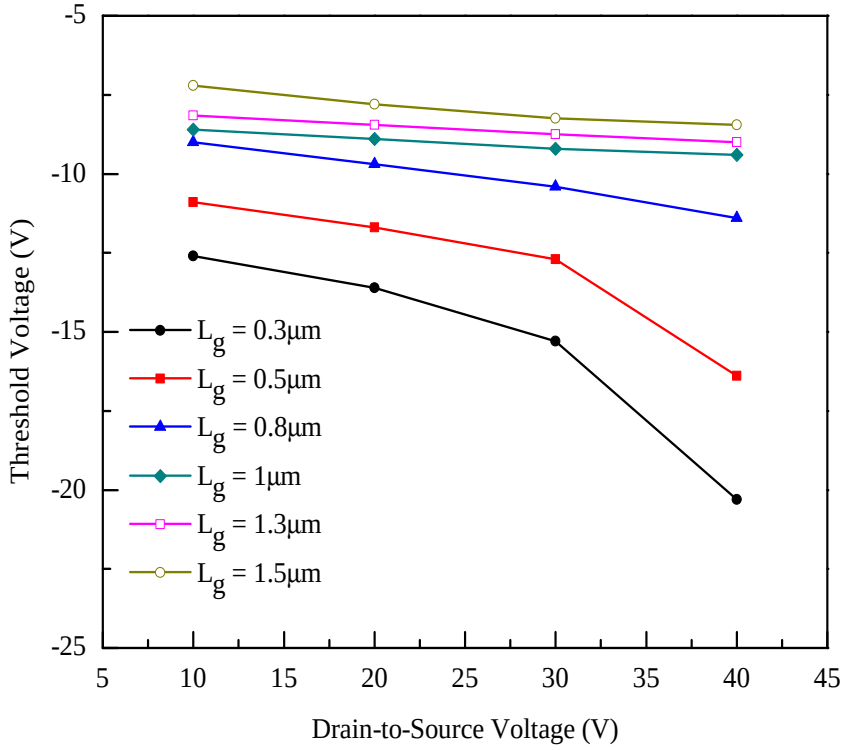


FIGURE 2.6: V_T as a function of V_{ds} and L_g.

1μm and exhibited fairly small g_d. This improvement was achieved at the cost of reduced g_m.

H. Yim et al. [54] fabricated SiC MESFETs with variable L_g, ranging from 0.3 μm to 3.0 μm to investigate short channel effects. They demonstrated that for $a =$ 0.32 μm devices, V_T shifted from -10.7V to -25.6V as L_g reduced from 3μm to 0.3 μm. The dependence of V_T on L_g became larger at $V_{ds} = 40$V than at $V_{ds} = 10$V where the observed shift in V_T was -10V to -18V. More precisely, V_T is a function of L_g/a and is almost constant for $L_g/a > 3$, but increases towards negative values as the ratio got lowered than 3. For $a = 0.22\mu$m devices, the short-channel effects enhanced when L_g/a got lowered than 5. Therefore, for submicron devices, one can say that V_T is a function of V_{ds}, L_g and a.

2.8 Transport Parameters in SiC MESFETs

Electrical performance of a SiC MESFET is greatly dependent on its transport properties; associated with carriers mobility and drift velocity. Accurate knowledge of transport characteristics helps to optimize the design and thus the performance of a SiC MESFET.

Transport parameters, especially, mobility and velocity of the carriers are the most important parameters and have significant influence on $I - V$ characteristics and RF performance of a SiC MESFET. Therefore, knowledge of transport parameters in the development of a model, aimed to represent the device characteristics, is of paramount importance. Hongliang et al. [74] used multi parameters mobility model to develop an analytical model for SiC MESFET and its velocity characteristics. Their multi-parameters model based on Monte Carlo calculation reproduced accurately the drift velocity characteristics of SiC carriers. The resulting $I - V$ characteristics were in good agreement with experimental data.

For low field, the velocity of carriers is linearly related to the applied electric field. However at high field the proportionality ceases due to increased scattering

and carrier's velocity saturates at certain value of electric field. Imran et al. [75] reported experimental measurements of υ_s for 6H and 4H-SiC as a function of applied electric field at 23°C and 32°C. Data confirm that υ_s of SiC carriers saturate $\sim 2\times10^7$cm/s and it is dependent on ambient temperature.

On the other hand, mobility of a charge carrier represents an ease by which a carrier can move. Mobility of n-carriers in SiC is relatively smaller; however, this smaller value is compensated by larger value of υ_s and it is twice as that of Si. Generally speaking, mobility is a function of temperature, impurity concentration and applied electric field. Based on these parameters, number of mobility models are reported in the literature. Caughey et al. [11] presented an empirical expression to achieve mobility profile as a function of doping and electric field. They demonstrated the validity of their proposed expression using experimental data for Si. Roschke et al. [76], based on experimental data and Monte Carlo results, developed a mobility model consisting of an analytical equation for 4H, 6H, and 3C-SiC. The model showed dependence of carrier mobility on doping concentration, temperature, and field.

Bertilsson et al. [77] used Monte Carlo, drift diffusion and hydrodynamic models to extract mobility, saturation velocity, and relaxation time for short channel 6H and 4H-SiC MESFETs. They exhibited a good agreement in modeled and experimental data. They also showed superiority of 4H-SiC over 6H-SiC by computing I_{dss}, g_m and f_T for both the devices.

Tucker et al. [78] fabricated MESFETs on semi-insulating 4H-SiC substrate by ion implantation. Effective channel carrier mobility was measured to be 29cm^2/Vs, and bulk carriers mobility of the channel found to be 240cm^2/Vs.

2.9 Breakdown Voltage of SiC MESFET

Performance and reliability studies are essential parts of SiC MESFET development. Anil Prasad et al. [79] studied effects of surface on breakdown voltage by

comparing different surface structures of 4H-SiC MESFETs such as non-recessed, channel-recessed, non-recessed buried-gate and channel-recessed buried-gate structures. Buried gate structure with recessed channel showed highest breakdown voltage compared to all other structures but with low I_{dss} magnitude. In addition, the effect of depth of buried region and L_g on breakdown voltage were also studied by them [79]. It was established that better device performance in terms of breakdown voltage could be achieved when L_g is 0.7μm and depth of buried region is 0.15μm with source and drain doping concentrations at 10^{19}cm^{-3}.

Electro-Static discharge (ESD) stress is one of the main sources of failure in electronic devices [80]. Phulpin et al. [81] investigated the robustness of a SiC-MESFET to ESD. The ESD robustness was rather low and found to be related to both current non-uniformity and a quite unexpected parasitic NPN bipolar transistor triggering. The outcome of this study allowed proposing first guidelines to optimize ESD robustness of such devices. He stated that SiC devices failure mechanism appears to be significantly different than Si devices [82]. This is mainly due to two reasons which are related to SiC material properties. First, its higher dielectric strength induces higher junction breakdown, which, as a consequence, tends to narrow the classical ESD design window by reducing or even inverting the triggering and oxide breakdown margin. This requires higher caution for metal-layers layout design and/or working on the dielectrics strength. Second, as SiC has no liquid phase at atmospheric pressure and is thus sublimated while attaining high temperatures, the observed defects would essentially be different than those observed in Si. While melted and recrystallized regions are often observed as ESD related defect in Si, material-hole defects are observed is SiC as shown in [82]. Wherein, structure has been proposed against ESD failure for SiC MESFETs. It is demonstrated experimentally in [83] that internal protection against ESD is higher in planar SiC MESFET. Adding a Zener, allows to increase the ESD robustness of this device. As this protection doesn't change the static characteristics it is, therefore, a promising solution for the development of robust SiC devices.

The simulation results presented in [84] reveal that a 95% improvement in breakdown voltage can be obtained with a metal plate between gate and drain electrodes

without causing much negative to its f_T. Ali A. Orouji et al. [85] proposed a novel structure of 4H-SiC MESFET with partly undoped space region in the n-channel between gate and drain. The simulation results showed that breakdown voltage increased from 109V to 144V. Breakdown voltage can also be enhanced by using multiple-recessed gate as proposed in [86]. Modification in the gate drain region changes the depletion region in the channel towards the drain-side, which in turn improves the electrical characteristics of the device. Amini et al. [87] reported a novel super junction MESFET where a p-type pillar is introduced in the drift region in order to improve breakdown voltage. The performance of the super junction MESFET was evaluated by two-dimensional simulation and compared with a conventional MESFET. On the basis of simulation results, the presence of p-type pillar improved breakdown voltage by modifying the electric field distribution inside the channel. Investigation showed that output power improved by a factor of 3 relative to a conventional MESFET.

A novel symmetrical structure of SiC MESFET was presented by Ramezani et al. [88] to improve the breakdown voltage and other electrical parameters. Using two-dimensional device simulation, they observed that breakdown voltage improved by a factor 3.3 in comparison with a symmetrical conventional MESFET structure. Also, the maximum output power improved $\sim$250% compared to conventional MESFET structures.

2.10 RF Characteristics

SiC MESFETs can comfortably operate in L and S-bands and, therefore, are very attractive devices for present communication systems such as cellular and satellite communications, and microwave links, etc. Due to their superior characteristics such as: high breakdown field; large υ_s and high thermal conduction, SiC MESFETs are replacing the bulky, low efficient and expensive devices like TWT and magnetron. This provides a cost effective, light weight, smaller size and more importantly, efficient communication systems.

Zhu et al. [30] proposed a double recessed gate SiC MESFET and investigated its electrical performance by a numerical simulation. The simulation showed 77% improvement in I_{dss} over the conventional device structure with small shift in V_T. A 37% improvement in output power density is obtained at the cost of lower breakdown voltage. f_T and f_{max} were 15.3GHz and 70.6GHz, respectively for the double recessed structure, which were higher than the conventional structure. Wojtasiak et al. [46] designed amplifier for L-band transmitter/receiver (T/R) modules, using two 60W SiC MESFETs, for an active phased-array radar with output power of more than 100W for both pulsed and CW operations from 1.2GHz to 1.4GHz frequency range. T/R modules were located directly behind the radiating elements thus, eliminating the feeder loss and noise. Manabu et al. [2] fabricated SiC high frequency MESFETs with f_T = 9.3GHz and f_{max} = 34GHz. The normalized power was 6.3W/mm at 1GHz to 2GHz frequency of operation, which was much higher than Si and GaAs devices. They also demonstrated experimentally that high frequency performance cannot be improved by simply reducing L_g because short channel effects dominate at shorter L_g and deteriorate the device performance.

Deng et al. [89] investigated gate-source scaling effects on SiC MESFET's characteristics by a two dimensional simulation. It was found that by down scaling gate-source distance, both DC and AC characteristics improved. DC and RF simulations and experimental results of a 4H-SiC MESFET for a high purity semi-insulating substrate are reported in [53]. For this purpose, 4H-SiC n-channel MESFETs with 100μm gate periphery were designed and then fabricated. A maximum current I_{dss} = 440mA/mm with a maximum g_m = 33mS/mm was obtained. CW measurement at a frequency of 2GHz exhibited maximum output power 6.6W/mm, with a gain of 12dB and PAE of 33.7%. Observed f_T and f_{max} were 9GHz and 24.9GHz, respectively whereas, simulated results of f_T and f_{max} were 11.4GHz and 38.6GHz, respectively.

In [90], SiC MESFETs were designed by employing a dual p-buffer layer and a multi-recessed gate for an S-band power amplifiers. A SiC MESFET with 20mm gate periphery biased at V_{ds} = 85V demonstrated a pulsed wave saturated output

power of 94W, a linear gain of 11.7dB, and PAE of 24.3% at 3.4GHz. Further, RF power output greater than 4.7W/mm was achieved, showing the potential of the device for high-voltage and high-power RF applications.

2.11 Novel Structures

Elahipanah et al. [84] proposed a double-recessed metal-plate SiC MESFET structure for reliable RF and high power applications. Their results showed that the breakdown voltages of the proposed structure were 55% and 195% larger than double recessed (DR-MESFETs) and recessed MESFETs (R-MESFETs) respectively, while maintaining the same I_{dss}. Maximum output power was 107% and 186% larger than DR-MESFETs and R-MESFETs, respectively. Results of the novel structure, called double recessed with a partly undoped space (DRUS-MESFET), as proposed by Orouji et al. [85], showed improvement in breakdown voltage along with 25.4% increase in maximum output power over DR-MESFETs. Moreover, their f_T and f_{max} were 95.6% and 13.07% larger than DR-MESFETs. MAG of DRUS-MESFETs was 4.5dB higher than DR-MESFETs at 40 GHz. Amirhossein et al. [86] proposed multiple-recessed structure for SiC MESFETs (MR-MESFETs) for improved electrical characteristics. They performed 2D numerical simulation to view the performance of their proposed structure. Their results showed that as the number of recessed gate sections were increased, breakdown voltage enhanced. Also, improvement in f_T, f_{max} and MAG were reported.

In [91], a SiC MESFET structure is proposed by incorporating L-gate and source field-plates (LSFP) for high power and RF applications. Their evaluation showed that the breakdown voltage of LSFP-MESFET is 91% higher than a conventional MESFET. LSFP-MESFET exhibited 77% higher I_{dss} compared to conventional MESFETs (C-MESFETs). The output power increased by a factor of 4 and 7.6dB enhancement in MSG at 3.1GHz over C-MESFET was observed. Also, they reported $f_T \approx 23.1$ GHz and $f_{max} \approx 85.3$GHz for LSFP-MESFET which were much higher than the C-MESFETs.

In [92], authors investigated a multi recessed (MR) SiC MESFET with recessed metal ring (MR2-MESFET) for RF embedded circuits. Their results allowed 119% higher breakdown voltage and 85% higher I_{dss} compared to C-MESFETs. Further, an exceptionally high output power of 23.1W/mm was claimed compared to 5.5 W/mm of C-MESFETs. $f_T \approx 24.9$GHz and $f_{max} \approx 91.7$GHz were obtained for MR2-MESFETs as contrast to 11GHz and 40GHz of C-MESFETs, respectively. H. Jia et al. [93] proposed a SiC MESFET having L-gate and partial p-type spacer (LP-MESFET). They presented 17% improvement in I_{dss}, 36% higher voltage breakdown (VBR) and 95% larger output power compared to C-MESFETs. RF performance of the proposed device also showed improvement due to decrease in C_{gd}. SiC MESFET electrical performance showed improvement by using double source field-plates (DSFP-MESFET) [94]. Simulation results showed improvement in VBR, output power, f_T, f_{max}, and MSG at 3.1GHz when compared with LSFP-MESFETs.

An L-gate SiC MESFET structure with a partial p-type spacer layer in source/drain drift region was proposed in [95]. Their results demonstrated improved DC performance and C_{gs} of the device reduced by 26% compared to LP-MESFET structure. The partial p-type spacer modulated the channel transverse electric field thus, the distribution of the depletion layer under the gate was modified. This improved the device performance by showing reduction in C_{gs} and C_{gd}. S. M. Razavi et al. [96] proposed two novel SiC MESFET structures; in 1st structure a recessed p-buffer layer on the source-side (SS-RPB) of the device, and in 2nd structure towards the drain-side (DS-RPB) of the device were incorporated. They showed that in SS-RPB devices there were reduction in C_{gs} and thus, improvement in f_T and f_{max} and g_m of the devices were observed relative to DS-RPB structures. Further, it was reported that short channel effects in SS-RPB structure were lower compared to DS-RPB structure. Moreover, VBR of DS-RPB were higher than those of SS-RPB devices.

S. M. Razavi et al. [97] also reported three structures for SiC MESFET: a) gate was recessed to the channel along with source side of the device, b) with gate recess, drain side of the device was also recessed to the p-buffer layer and c) along with

gate both source and drain sides of the device were recessed, also to the p-buffer layer. For all the three structures, recessed gate depth into channel and recessed channel depth into p-buffer layer were 0.05μm. Authors compared the results of the proposed structures with the conventional one [96]. Simulation results revealed that structure (c) exhibited increased g_m, increased output resistance (r_0) and relatively high VBR. They also reported that this structure offered lower short channel effects compared to other two structures, i.e. structure (a) and (b).

Jun et al. [98] proposed a new structure for 4H-SiC MESFETs by embedding a thinner and heavily doped buffer layer between the gate and the channel layer. They developed a physics based analytical model to evaluate the performance of the proposed device by solving 2D Poisson's equation. The simulation results showed significant improvement in I_{ds}, f_T, and f_max.

Z. Ramezani et al. [99] proposed a double-recessed structure for 4H-SiC MESFET in which the channel of the device had a floating metal region (FMR-MESFET). The electric field lines were allowed to be scattered by the floating metal thus, more electrons were allowed to participate in the channel current. They demonstrated that VBR and I_{dss} of the device were improved by 54% and 22%, respectively, compared to DR-MESFETs. Moreover, maximum output power improved by a factor of 3.38 compared to DR-MESFETs. They also showed significant improvement in f_T and f_{max} of the device.

H. Jia et al. [100] reported a novel clival gate 4H-SiC MESFET (CG-MESFET). The device characteristics were simulated using ISE-TCAD software. Results indicated I_{dss} of 545 mA/mm which was considerably higher than DR-MESFETs. Moreover, CG-MESFETs offered high VBR, i.e. 15% higer than DR-MESFETs with superior DC performances. Jia et al. [101] in another design also proposed a structure having ultrahigh upper gate (UU-MESFET), conceived by selective source-side etching. The proposed design gave modification in drain-side depletion, which improved simultaneously DC as well as RF characteristics as demonstrated by simulation results. Using ISE-TCAD simulation, they observed that VBR of the proposed structure increased from 109V to 168V compared to DR-MESFETs,

because of the electric field modulation at lower gate corner. UU-MESFETs exhibited $I_{dss} \sim 515.4$mA/mm and normalized output power 10.26W/mm in comparison with 448 mA/mm and 5.77 W/mm of the DR-MESFET, respectively. C_{gs} and C_{gd} of UU-MESFET were ∼17% and ∼8% lower than that of DR-MESFETs at $V_{gs} = 0$V and $V_{ds} = 40$V, respectively; leading to improved RF characteristics.

An improved clival gate 4H-SiC MESFET with recessed drain drift region and recessed p-buffer layer (RDRP-CG-MESFET) was proposed and numerically simulated in [102]. Results showed VBR ∼ 116.3V, which was about 51.8% higher than that of CG-MESFETs. There was an 11.9% increase in I_{dss} of RDRP-CG MESFET compared to CG-MESFET. Maximum output power was ∼70% higher than that of CG-MESFETs, which could, primarily, be associated with increased I_{dss} and VBR. Capacitor C_{gs} showed 32% and 27% reduction whereas, capacitor C_{gd} exhibited a reduction of 21% and 23.8%, and g_0 showed an improvement by 38% and 28%, compared to DR-MESFETs and MR-MESFETs, respectively.

An improved 4H-SiC MR-MESFET with double-recessed p-buffer layer (DRB-MESFET) was proposed and simulated in [103]. The simulation showed that I_{dss} of DRB-MESFET was ∼42.4% higher than that of MR-MESFETs. DRB-MESFETs g_m was ∼15% higher than that of MR-MESFETs, which was close to that of DR-MESFETs when $V_{gs} = 0$V and $V_{ds} = 4$V. The proposed structure showed an improvement of 26.1% and 74.2% in maximum output power compared to that of MR-MESFETs and DR-MESFETs, respectively. Furthermore, the proposed structure exhibited smaller C_{gs} capacitance therefore, reported f_T and f_{max} were 24.6GHz and 63.7GHz, compared to 21.1GHz and 58.2GHz, respectively, for MR-MESFETs.

A 4H-SiC MESFET with Γ-gate and recessed p-buffer layer (ΓRP-MESFET) was proposed and simulated to evaluate its performance parameters [104]. Results showed that I_{dss} and VBR of the proposed structure were ∼18.5% and 19.4% higher compared to DR-MESFET. Maximum output power was 42% higher than that of reported one. Due to smaller C_{gs}, offered by the Γ-gate, the obtained f_T was also higher than DR-MESFETs.

An improved structure of 4H-SiC MESFET with multi-recessed source/drain drift regions (MRD-MESFET) is proposed in [105]. Simulated results indicated that VBR of MRD-MESFET is 141V compared to 119V of single-recessed source/drain region MESFET (SRD-MESFET). Maximum output power was ∼19.1% larger than that of SRD-MESFETs. Also, f_T and f_{max} of the proposed structure were 17GHz and 68GHz compared to 15GHz and 59GHz of SRD-MESFETs. The lowest C_{gs} and C_{gd} of the MRD-MESFETs were obtained by optimizing source drain drift region recess depth.

In 2016, a 4H-SiC MESFET with a novel dual well in the buffer layer (DW-MESFET) was presented by Orouji [106]. There was 34.7% increase in I_{dss} whereas, maximum output power and g_m showed an increase of 45.23% and 72.5%, respectively, compared to C-MESFETs. In 2016, Jia et al. also presented a novel structure of 4H-SiC MESFET with double upper gate and recessed p-buffer (DURP MESFETs) [107]. A 22.5% increase in I_dss and a 17.9% increase in VBR compared to DR MESFETs were reported for DURP-MESFET. C_{gs} of DURP-MESFET was 0.439 pF/mm compared to 0.573 pF/mm of DR MESFET thus, offering promising RF characteristics.

An improved double-recessed p-buffer 4H-SiC MESFETs with a partial heavy doped channel (HD-MESFET) is proposed in [108]. Simulation showed that I_{dss} of the proposed structure increased by 18.4% relative to DURP-MESFETs. There was a slight decrease in VBR however, maximum output power was still showing an upward trend and an increase of ∼16.5% was observed when compared with DURP-MESFETs. In addition, g_m showed an increase of ∼32% relative to that of DURP-MESFETs.

2.12 Radiation Hardness

Along with other specific advantages offered by SiC technology, radiation hardness is another feature, which makes SiC MESFETs suitable to operate in radiation-rich environments. Electron and neutron irradiation has negligible effects on SiC

schottky barrier junction characteristics as discussed in [109, 110]. The study of gamma-rays irradiation to 4H-SiC MESFET showed a slight variation in V_T after an absorbed dose of 10.4MGy. Further, it is shown in [111] that $I-V$ characteristics of a SiC MESFET showed little variation by gamma irradiations thus, the device can comfortably be used in an electromagnetic/gamma rich environment.

Ohyama et al. [112] studied impact of radiation damage on the performance of 4H-SiC MESFETs. For this purpose they irradiated SiC MESFETs by electrons having energy 2MeV, at room temperature, and also by 20MeV protons. No performance degradation was observed by 1×10^{12} e/cm^2 and 5×10^{11} p/cm^2 doses, while a slight increase of the linear drain current together with a decrease in V_T were noticed above higher fluence. The damage coefficient for protons was $\sim$3 orders of magnitude larger than that for electrons. Zhang Lin [113] investigated radiations related degradation of 4H-SiC MESFETs by using 1MeV neutron. It was observed that irradiating a SiC MESFET with a neutron flux of 10^{13} n/cm^2, there was a slight change in $I-V$ characteristics of the device. However, increasing the neutron flux from 10^{13} n/cm^2, there was sufficient damage caused by the impinging neutrons and as a result a decrease in I_{ds} coupled with an increase in V_T magnitude were noticed. It was also shown that a high doping concentration of the active region improve the neutron radiation tolerance.

2.13 Self-Heating Effects

SiC is a wide band-gap semiconductor material with excellent thermal conduction characteristics. Compared to other semiconductor materials such as Si and GaAs, SiC MESFETs based devices can operate over a large temperature range and thus, can comfortably be used in harsh environments [114]. SiC MESFETs and their integrated circuits had been successfully fabricated and their characteristics were investigated at elevated temperatures by many reserchers [115, 116].

Although, thermal conduction of SiC is much better than other semiconductors, yet due to large power dissipation, the temperature of a SiC MESFET quickly

rises referred to as self-heating of the device. Due to self-heating, μ_0 and υ_s of the carriers in the active part of the channel decrease thus, degrading the performance of the device. Thermal resistance associated with self-heating effects is a function of device surface layout parameters and the power it can handle [117, 118].

It is an established fact that with increase in the device inner temperature, due to self-heating effects, there is a change in the device static as well as dynamic characteristics. The self-heating, due to the large power dissipation, leads to the lowering of current derive capabilities in the static regime of operation and hence, the performance of the device is degraded. Therefore, self-heating effects must be taken into account in device modeling and design processes for correct assessment of its performance [119]. Bisewski et al. investigated thermal parameters of SiC MESFETs and evaluated thermal resistance and transient thermal impedance [120]. They showed that both of the parameters are strong function of ambient temperature and power dissipation caused by the device.

Deng et al. [89], reported an electrothermal analytical model of multi-finger 4H-SiC MESFETs while taking into account self-heating effects. They investigated the dependence of peak temperature on V_{ds}, gate-to-gate pitch and substrate thickness. Hans et al. [13] performed electrothermal simulation and showed that effects of electrical heating had significant role on power MESFETs transport characteristics and must be taken into account for precise modeling and parameters assessment.

2.14 SiC MESFET Modelling

For efficient and economical design of a device, a reliable model capable to predict the device characteristics is required. If a model gives a closed form solution, in terms of device geometry, doping profile, field dependent electron velocity, low-field mobility, barrier height, impact ionization, surface states, etc., and is able to give insight of the device then it is referred to as an analytical model. In case of SiC MESFETs, the development of an analytical model requires solution of two

dimensional Poisson's equation subject to certain boundary conditions determined by the device geometry.

An extensive work has been carried out on the development of analytic models of junction field effect transistors including MESFETs [121–124]. The models were developed for the devices fabricated using Si, GaAs, and other semiconductor materials. Analytical model developed for SiC MESFETs so far, are based upon the theory of GaAs MESFETs. Since SiC MESFETs can comfortably be used at higher temperature ($\sim 300°C$) and also in harsh environment, moreover, they offer high VBR and high v_s, etc. therefore, SiC MESFETs models require further amendment for their improved high temperature operation both at DC and AC levels.

A number of analytical models for SiC MESFETs are reported in the literature. Tsap et al. [28] developed an analytical model by dividing the depletion layer underneath the Schottky barrier gate into two regions: a region below the velocity saturation and a region operating at velocity saturation. Their model also considered field-dependent mobility and velocity saturation as per the channel conditions. They reported that since the critical field for velocity saturation is large in SiC MESFETs, unlike GaAs MESFETs, the electrons do not reach their saturation velocity for a reasonable portion of the channel. As a result, the constant mobility approximation is adequate to describe the electron transport in major part of the channel otherwise it will lead to an inaccurate estimation of I_{ds} and the device characteristics.

Murray et al. [29] developed an improved two region analytical model for SiC MESFETs which takes into account not only the field-dependent mobility of the electrons near the source, but also the charge buildup effects due to the velocity saturation at the drain-end of the channel. However, the model did not consider the voltage drop across the un-gated section of the depletion region, especially, high field region near the drain. Thus, the accuracy is compromised, especially, for the devices which offer high I_{dss}.

Zhu et al. [30] proposed an analytical model by dividing the depletion layer underneath the Schottky barrier into three regions: a) a region operating below velocity saturation; b) a region operating at velocity saturation and c) a region defining extension of charges after the onset of velocity saturation towards the drain-side of the device. They also incorporated effects of parasitic resistances and an incomplete ionization of dopants. The model gave better results than that of Murray model devices having $L_g < 1\mu$m, but still considerable deviations from experimental data were there, especially for the devices having high g_d.

On the other hand, scientists and engineers working on the device design require quick handling of the device geometry and its relation to the targeted characteristics without involving much into the device physics. They preferred an expression, which can predict the device characteristics by involving the device design parameters and biasing referred to as empirical expression. In an empirical expression, there are number of empirical variables, which require optimization tool and thus, an optimization tool is usually needed in an empirical modeling process. Such models are frequently employed in device characterization and circuit design softwares and offer sufficient accuracy [31, 125, 126].

There is yet another approach, which is more popular than the empirical modeling called as semi-empirical technique; to model the device characteristics. In semi-empirical approach, 1$^{\text{st}}$ order behavior of the device is determined by an analytical expression; square law in case of a MESFET, and 2$^{\text{nd}}$ order effects are then incorporated by appropriately modifying the square law expression. Such an approach does not deviate much from the device physics, yet it offers a simple comprehensive expression to accommodate all those variables which can potentially affect the device performance. There are numerous examples of semi-empirical models reported in the literature [127–129]. These models, by and large, are based on the fundamental square law expression of a MESFET, which is modified to accommodate different 2$^{\text{nd}}$ order effects namely: a) finite g_0 after the onset of current saturation; b) V_T dependance on V_{ds}; c) shift in V_T due to submicron geometry; d) non-ideality in Schottky barrier junction; e) depletion layer modification at high V_{ds}, etc.

AC response of a SiC MESFET can be evaluated by knowing its intrinsic small signal parameters. Primarily, these parameters are associated with the device Schottky barrier depletion and dielectric relaxation time of the material [130]. It is a known fact that Schottky barrier depletion is a function of V_{ds} and V_{gs}. Thus, intrinsic small signal parameters are also biased dependent. Ladbrooke [130] developed a set of expressions which can predict biased dependent intrinsic AC parameters of a GaAs MESFET. He also demonstrated the variation of these parameters as a function of device biasing. The concept discussed by Ladbrroke in [130] is, in general, valid for SiC MESFET, but it does not take into account the intense channel conditions which are usually there in SiC MESFETs.

By extending the concept of Ladbrooke, Murray et al. [29] also developed a set of expressions by involving charge accumulation in Schottky barrier depletion layer, to predict AC small signal parameters. In Murray model first DC characteristics are modeled and based on DC assessment, AC small signal parameters are then evaluated. It was reported that Murray model gives good DC accuracy for low current devices and its accuracy deteriorates when I_{dss} of the device is $\sim$ 50mA or higher [39], which is usually the case for SiC power MESFETs. Thus, the need to have an AC small signal model, which can predict AC response of the device meant for microwave power applications is still alive.

In conclusion, one can say that there are different techniques available in the literature to model DC and AC characteristics of SiC MESFETs but, their applicability is limited. They are not fully accommodating high biasing conditions of the device especially, when the device L_g is in submicron regime. Thus, there is still a need to have a comprehensive DC as well as an AC model particularly, for the devices having submicron L_g; to predict the device response accurately and to allow its integration in high power circuitry in an optimized way.

2.15 Summary

In this chapter an overview of SiC MESFETs, their characteristics and applications are presented. Progress made so far in the device design to get improved performance is discussed. It is shown that the device has a very good potential to be used in microwave communication systems. It is discussed that SiC MESFETs exhibit stable performance at high ambient temperature and also in radiation rich environment. The work reported by different research groups established the fact that SiC MESFETs could stand with high power requirement along with superior linearity characteristics in microwave amplifiers. Furthermore, owing to relatively better thermal conductivity, SiC MESFETs provide superior conduction of the heat generated by high power operating conditions thus, maintaining their stable performance. The ultimate operating temperature of the device is determined by its ceramic packaging, so new packaging materials for the circuits containing SiC MESFETs should be searched to realize full benefits of the device.

Novel structures of SiC MESFETs are discussed, which are reported in the literature, to improve the device power handling capabilities and to increase its f_T and f_{max} of operation. To improve g_m of the device and to reduce its g_0, in the saturation of operation, different channel layers and recessed technologies are discussed. It has been established that a thin heavily doped channel with low drain side resistance would provide relatively high g_m and VBR.

To explore the fullest capacity of the device, and to know its physical behavior, simulation and modeling techniques are usually employed. Analytical, empirical and semi-empirical models developed for SiC MESFETs were reviewed. A need of a comprehensive model was established to predict DC characteristics. Moreover, it is discussed that an accurate AC model is needed to predict intrinsic small signal parameters of the devices designed for microwave power applications.

Chapter 3

Analytical Model for Submicron SiC MESFETs

3.1 Introduction

SiC offers low intrinsic carrier concentration, larger band gap than Si, a high avalanche break down electric field, and high electron saturation velocity [131]. Thus, for high power applications SiC MESFETs are preferred than GaAs MESFETs. Current-Voltage ($I-V$) characteristics of a SiC MESFET is the primary evaluation used to assess the quality of a device. Because of wide band gap and high thermal conductivity, SiC devices can handle relatively higher power than GaAs/AlGaAs based FETs and are usually subjected to harsh environmental conditions. Moreover, in order to allow these devices to operate at microwave frequencies, it is mandatory that gate length, L_g of the device should be in submicron regime [39, 132]. However, a submicron L_g device requires stringent fabrication constraints and, thus, non-uniformities in the device characteristics are commonly witnessed [133]. Like other MESFETs, submicron SiC MESFETs also exhibit short channel effects which include [134–136]:

1. high output conductance in the saturation region of operation;

2. compression in its transconductance and

3. shift in pinch-off voltage

Short channel effects are classified as second order effects in their nature, imposing additional challenges to engineers and scientists involved in the device modeling; whereby, making the device's analytical modeling a more demanding and cumbersome task.

This chapter discusses in detail the analytical modeling techniques of submicron SiC MESFETs. In the fist part of the chapter, the mobility of free carriers under a channel electric field is discussed, whilst, the second part of the chapter deals with potential distribution inside the channel. In this section regions have been identified underneath the Schottky barrier gate responsible for the flow of the carriers initially with constant mobility followed by the constant velocity region. In the third part of the chapter, the idea of depletion layer modification has been introduced to achieve improved accuracy in the device modeling, and finally to establish the validity of the proposed idea, modeled and observed $I-V$ characteristics have been presented.

3.2 Field Dependent Mobility and Velocity

Consider an operating submicron SiC MESFET, as shown in Fig. 3.1, the device is n-doped with channel doping $1.7\times10^{17}cm^{-3}$. The Schottky barrier gate is placed in recess which defines the desired target current, I_{dss} and pinch-off voltage, V_P. The depletion layer underneath the Schottky barrier gate is divided into three regions [137]: Region-I is the one where carriers are moving below saturation velocity limit, and the mobility in this region can be taken as constant. Region-II is the region where carriers are moving with saturation velocity (υ_s) and drain current of the device, under ideal conditions, becomes independent of drain potential. Region-III represents the extension of the depletion layer towards the drain side of the

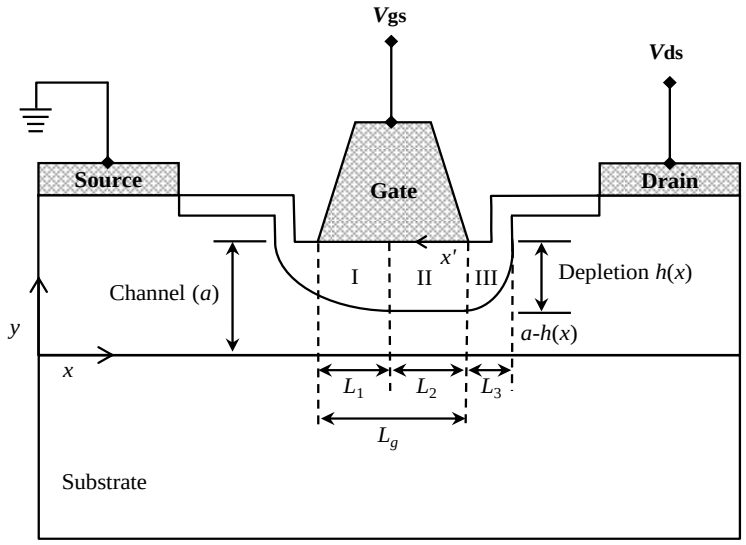


FIGURE 3.1: An operating submicron SiC MESFET with three distinct depletion layer regions underneath Schottky barrier gate.

device. This region defines the maximum electric field of the device and, thus, is responsible for its breakdown.

It is an established fact that doping dependent mobility, μ_0 follows a Fermi-Dirac profile and can be expressed as [11, 138]

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + (N_d/N_r)^{\alpha}} \ , \tag{3.1}$$

where μ_{min} and μ_{max} are the minimum and maximum mobilities, respectively. N_d is the doping concentration. N_r and α represent empirical constants. Field dependent mobility, $\mu(E)$ can be expressed as [72]

$$\mu(E) = \frac{\mu_0}{\left[1 + (\mu_0 E(x)/\upsilon_s)^{\beta}\right]^{1/\beta}} \ , \tag{3.2}$$

where β is a constant having value $\leqslant 1$ and υ_s represents saturation velocity. By using (3.2) one can write the field dependent velocity, $\upsilon(E)$ of carriers moving in a SiC MESFET channel as [139]

$$v(E) = \frac{\mu_0 E(x)}{\left[1 + (\mu_0 E(x)/\upsilon_s)^{\beta}\right]^{1/\beta}} \ . \tag{3.3}$$

TABLE 3.1: Data used for simulation of Fig. 3.2

Parameters	**Values**
μ_{min}	40 cm^2/V-s
μ_{max}	950 cm^2/V-s
N_{ref}	1×10^{17} cm^{-3}
N_d	1.7×10^{17} cm^{-3}
α	2.6

Figure 3.2(a) demonstrates the β dependent $\mu(E)$ for a SiC device; whereas, Fig. 3.2(b) illustrates dependence of $\upsilon(E)$ on the chosen values of β as given in (3.2). The simulated values of both $\upsilon(E)$ and $\mu(E)$ are identical to those which are reported in the literature for SiC devices [74, 76, 77, 138].

Figure 3.2 was plotted by using the data given in Table 3.1. Plots of Fig. 3.2 show that by considering the material quality, device geometry and biasing conditions, α, β and N_r can be chosen appropriately to achieve a reasonable match between modeled and experimental characteristics of SiC MESFETs.

3.3 Potential Distribution Inside the Channel

Consider Fig. 3.1, at $V_{ds} > 0$V, the drain current density, J_d inside SiC MESFET channel is given by $J_d = qN_d\upsilon$, where υ is the low field velocity. The channel current can be defined as [130]

$$I_d = qN_d\upsilon W\left[a - h_x\right] \ , \tag{3.4}$$

where $W[a - h_x]$ is the available channel cross-section for the flow of current as shown in Fig. 3.1, q is the electronic charge, a represents epi-layer thickness and h_x represents depletion layer height at any point x. For low field regions, β can be substituted as unity in (3.3) and combining it with (3.4) yields

$$I_d = qN_d\left(\frac{\mu_0 E\left(x\right)}{1 + \left[\mu_0 E\left(x\right)/\upsilon_s\right]}\right) W\left(a - h_x\right) \ . \tag{3.5}$$

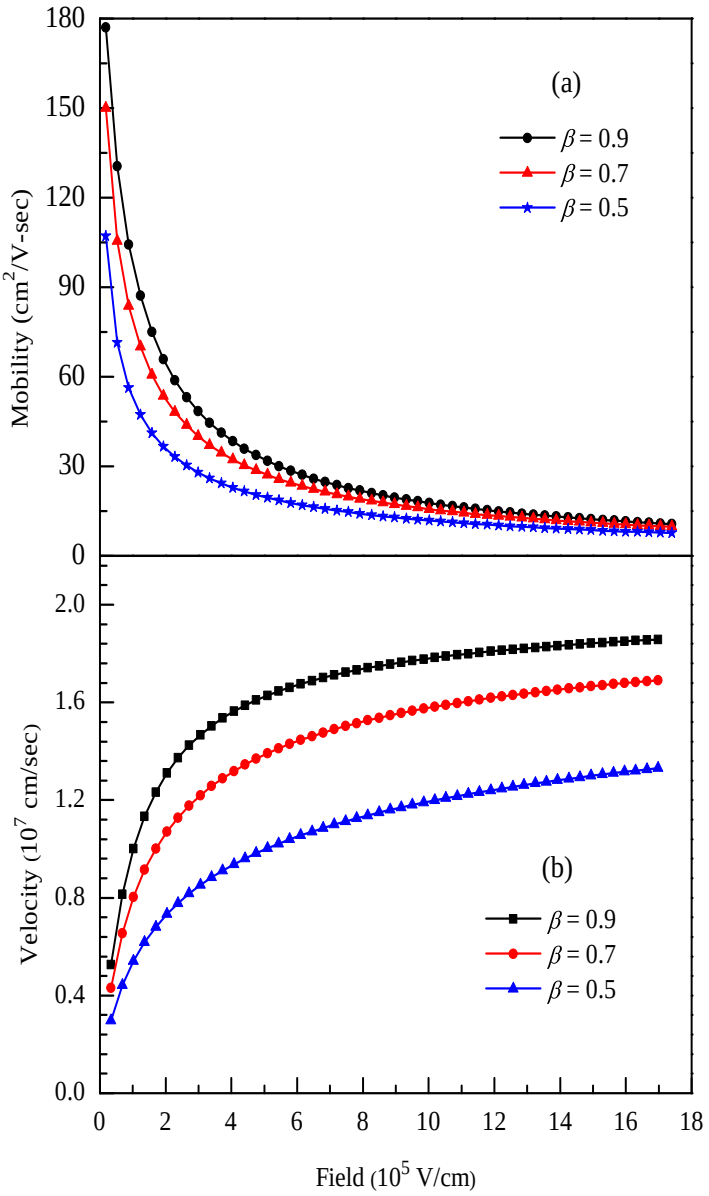


FIGURE 3.2: Field dependent (a) mobility and (b) velocity of a SiC MESFET.

or

$$I_d\left(1+\frac{\mu_0}{\upsilon_s}\frac{dV\left(x\right)}{dx}\right)=qN_d\mu_0 W\frac{dV\left(x\right)}{dx}\left(a-h_x\right)\ . \tag{3.6}$$

Since depletion height underneath the Schottky barrier gate at point x is given by [130],

$$h_x^2=\frac{2\varepsilon_s}{qN_d}\left[V\left(x\right)-V_g+V_{bi}\right]\ , \tag{3.7}$$

where ε_s is the permittivity of SiC, V_g is the gate biasing, V_x is the potential at any point x because of the drain biasing and V_{bi} is the built-in potential. From

the above expression, $2h_x dh_x = [2\varepsilon_s/qN_d]dV(x)$ and substituting the same in (3.6) gives

$$I_d\left(dx + \frac{\mu_0}{\upsilon_s}\frac{qN_d}{\varepsilon_s}h_x dh_x\right) = qN_d\mu_0 W\frac{qN_d}{\varepsilon_s}h_x\left(a - h_x\right)dh_x \ . \tag{3.8}$$

Integrating both sides with appropriate limits as per the geometry of Fig. 3.1:

$$I_d\left(\int_0^{L_g} dx + \frac{qN_d\mu_0}{\upsilon_s\varepsilon_s}\int_{h_0}^{h_d} h_x dh_x\right) = \frac{\left(qN_d\right)^2\mu_0 W}{\varepsilon_s}\int_{h_0}^{h_d} h_x\left(a - h_x\right)dh_x \ . \tag{3.9}$$

or

$$I_d\left[L_g + \frac{qN_d\mu_0 a^2}{2\upsilon_s\varepsilon_s}\left(\frac{h_d^2}{a^2} - \frac{h_0^2}{a^2}\right)\right] = \frac{\left(qN_d\right)^2\mu_0 W}{6\varepsilon_s}a^3\left[3\left(\frac{h_d^2}{a^2} - \frac{h_0^2}{a^2}\right) - 2\left(\frac{h_d^3}{a^3} - \frac{h_0^3}{a^3}\right)\right] \ . \tag{3.10}$$

The normalized depletion layer width, by using (3.7) at source, u_0 and drain, u_d edges of the gate can be expressed respectively as,

$$u_0 = \frac{h_0}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon_s\left[V_{bi} - V_g\right]}{qN_d}} \ . \tag{3.11}$$

and

$$u_d = \frac{h_d}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon_s\left[V_{bi} - V_g + V_d\right]}{qN_d}} \ . \tag{3.12}$$

Consider a submicron SiC MESFET whose device variables are defined in Table 3.2. For this device the depletion layer height, before the onset of current saturation, has been plotted by using (3.12) and shown in Fig. 3.3. It is obvious from the figure that with increasing magnitude of V_g, the depletion layer terminates at lower V_d values because, it is linked with saturation drain voltage, $V_{d(sat)}$, which itself is dependent on V_g. Since the depletion layer is normalized with physical channel thickness (a), its value below unity indicates that for given V_g biasing, a finite thickness of physical channel is still available for the conduction of current. Thus, current saturation in submicron SiC MESFET is caused by the velocity saturation of the carriers contrary to long channel devices where current saturation is associated with the channel pinch-off [130]. Substituting u_0 and u_d from (3.11) and (3.12) in Eqn. (3.10) and rearranging for I_d, we get

TABLE 3.2: Physical parameters of a submicron SiC MESFET.

Parameters	**Value**	**Parameters**	**Value**
ε_0	8.85×10^{-12} Fm^{-1}	V_{bi}	1.1eV
ε_s	$9.7\varepsilon_0$ Fm^{-1}	γ	0.98
υ_s	2×10^7 cms^{-1}	a	0.26 μm
L_s	0.3 μm	L_g	0.7 μm
β	0.87	L_d	0.8 μm
N_d	1.7×10^{17} cm^{-3}	W	332 μm
q	1.6×10^{-19} C	R_b	2 kΩ

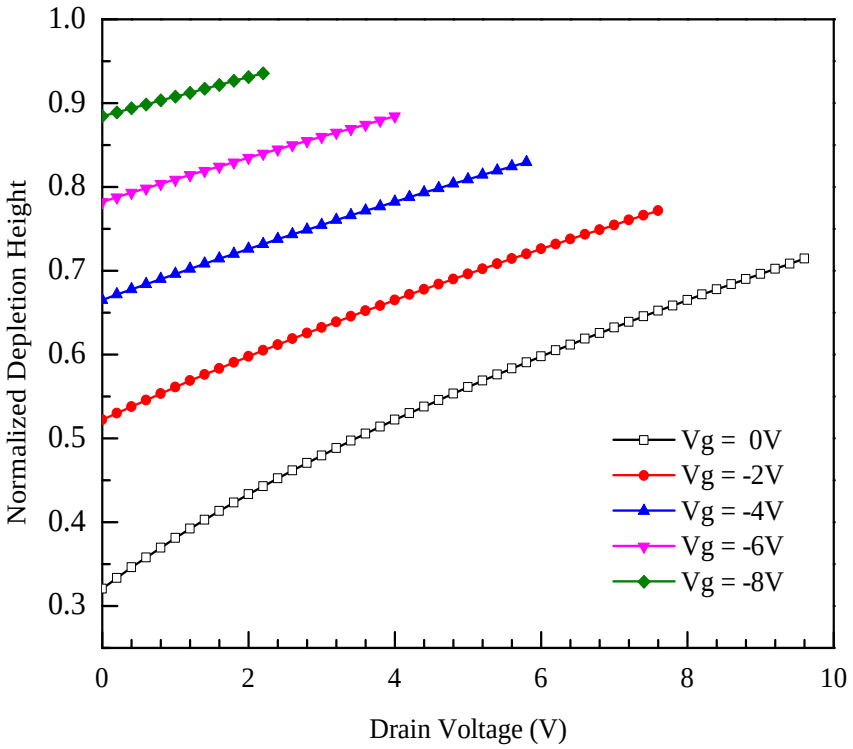


FIGURE 3.3: Variation in Schottky barrier depletion before the onset of current saturation for a submicron SiC MESFET.

$$I_{d(\text{linear})} = \frac{I_p \left[3\left(u_d^2 - u_0^2\right) - 2\left(u_d^3 - u_0^3\right)\right]}{1 + z\left(u_d^2 - u_0^2\right)} , \tag{3.13}$$

where

$$z = \frac{qN_d a^2 \mu_0}{2\varepsilon_s L_g \upsilon_s} . \tag{3.14}$$

and

$$I_p = \frac{q^2 N_d^2 \mu_0 W a^3}{6\varepsilon_s L_g} . \tag{3.15}$$

From (3.3) one can write

$$\frac{\upsilon(E)}{\mu_0} = \frac{E(x)}{(1+[\mu_0 E(x)/\upsilon_s])} \ . \tag{3.16}$$

When $E(x)$ reaches to saturation field, E_s, $\upsilon(E)$ reaches to $\gamma\upsilon_s$ [30], therefore

$$\begin{aligned} \frac{\gamma\upsilon_s}{\mu_0} &= \frac{E_s}{1+\gamma\upsilon_s/\upsilon_s} = \frac{E_s}{1+\gamma} \\ E_s &= \frac{(1+\gamma)\gamma\upsilon_s}{\mu_0} \approx \frac{2\gamma\upsilon_s}{\mu_0} \ , \end{aligned} \tag{3.17}$$

where $\gamma \sim 0.98$. Assuming that current saturation in a SiC microwave MESFET is due to the velocity saturation which is attained by the carriers at a location underneath the Schottky barrier gate where the depletion thickness is represented by h_1, then (3.4) can be rewritten as

$$I_{d(\text{sat})} = qN_dW\gamma\upsilon_s\,(a-h_1) = qN_dWa\gamma\upsilon_s\left(1-\frac{h_1}{a}\right) \ . \tag{3.18}$$

$$I_{d(\text{sat})} = qN_dWa\gamma\upsilon_s\,(1-u_1) \ . \tag{3.19}$$

where u_1 is normalized depletion under which the carrier are moving with saturation velocity at $x = L_1$ wherein, $V\,(x) = V\,(L_1) = V_{sat}$ and $h_x = h_1$. Hence u_1 is obtained simply by replacing u_d by u_1, h_d by h_1 and V_d by $V\,(L_1)$ in (3.12) as under

$$u_1 = \frac{h_1}{a} = \frac{1}{a}\sqrt{\frac{2\varepsilon_s\,[V_{bi}-V_g+V\,(L_1)]}{qN_d}} \ . \tag{3.20}$$

The start of u_1, according to Fig. 3.1, is at the boundary of L_1. Thus, potential drop by using (3.20) for the region defined by L_1, referred to as Region-I, is given by

$$V(L_1) = u_1^2V_p - V_{bi} + V_g = V_{d(\text{sat})} \ , \tag{3.21}$$

where

$$V_p = \frac{qN_d}{2\varepsilon_s}a^2 \ . \tag{3.22}$$

or

$$V(L_1) = V_p\left(u_1^2 - u_0^2\right) \ . \tag{3.23}$$

Assuming that the current in Region-I is represented by I_c then by changing the integration limits of (3.9) from 0 to L_1 and h_0 to h_1, one can write

$$I_c\left(\int_0^{L_1} dx + \frac{qN_d\mu_0}{\upsilon_s\varepsilon_s}\int_{h_0}^{h_1} h_x dh_x\right) = \frac{(qN_d)^2\,\mu_0 W}{\varepsilon_s}\int_{h_0}^{h_1} h_x\,(a - h_x)\,dh_x \ . \tag{3.24}$$

or

$$I_c\left[L_1 + \frac{qN_d\mu_0 a^2}{2\upsilon_s\varepsilon_s}\left(\frac{h_1^2}{a^2} - \frac{h_0^2}{a^2}\right)\right] = \frac{(qN_d)^2\mu_0 W}{6\varepsilon_s}a^3\ \left[3\left(\frac{h_1^2}{a^2} - \frac{h_0^2}{a^2}\right) - 2\left(\frac{h_1^3}{a^3} - \frac{h_0^3}{a^3}\right)\right] \ . \tag{3.25}$$

Substituting u_0 and u_1 in (3.25) as defined in (3.11) and (3.20)

$$I_c\left[L_1 + \frac{qN_d\mu_0 a^2}{2\upsilon_s\varepsilon_s}\left(u_1^2 - u_0^2\right)\right] = \frac{(qN_d)^2\mu_0 W}{6\varepsilon_s}a^3\ \left[3\left(u_1^2 - u_0^2\right) - 2\left(u_1^3 - u_0^3\right)\right] \ . \tag{3.26}$$

Using (3.14) and (3.15), (3.26) can be written as

$$I_c\left[L_1 + zL_g\left(u_1^2 - u_0^2\right)\right] = I_p L_g\left[3\left(u_1^2 - u_0^2\right) - 2\left(u_1^3 - u_0^3\right)\right] \ . \tag{3.27}$$

or the channel current in Region-I is [28]

$$I_c = \frac{I_p\,(L_g/L_1)\,[3(u_1^2 - u_0^2) - 2(u_1^3 - u_0^3)]}{1 + z(L_g/L_1)(u_1^2 - u_0^2)} \ . \tag{3.28}$$

Since at the end of Region-I or at the start of Region-II, $I_c = I_{d(\text{sat})}$, therefore, equating (3.19) and (3.28)

$$qN_d W a\gamma\upsilon_s\,(1 - u_1) = \left(\frac{q^2\ N_d^2\mu_0 W a^3}{6\varepsilon_s L_g}\right)\left[\frac{(L_g/L_1)\,[3\,(u_1^2 - u_0^2) - 2\,(u_1^3 - u_0^3)]}{1 + z\,(L_g/L_1)\,(u_1^2 - u_0^2)}\right] \ . \tag{3.29}$$

Using (3.14), we have the length L_1 where the carriers are attaining saturation velocity

$$L_1 = L_g z\left[\frac{[(u_1^2 - u_0^2) - 2/3\,(u_1^3 - u_0^3)]}{\gamma\,(1 - u_1)} - \left(u_1^2 - u_0^2\right)\right] \tag{3.30}$$

To assess the depletion height at L_1, let us assume two-dimensional potential distribution inside the channel expressed by the Poisson's expression [29, 121, 137, 140]:

$$\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_s} \ . \tag{3.31}$$

Using co-ordinate transformation $x^{'} = x - L_g$, as explained in Fig. 3.1, one can define (3.31) as a sum of two potentials $W\left(x',y\right) = \xi\left(y\right) + V(x,y)$ such that

$$\frac{d^2\xi}{dy^2} = \frac{qN_d}{\varepsilon_s} \ . \tag{3.32}$$

and

$$\frac{\partial^2 W(x',y)}{\partial x^2} + \frac{\partial^2 W(x',y)}{\partial y^2} = 0 \ . \tag{3.33}$$

such that

$$W\left(x',y\right) = V\left(x,y\right) + \frac{qN_d}{2\varepsilon_s}y^2 \ . \tag{3.34}$$

Equation (3.33) can be solved by assuming: a) potential is a continuous function of (x,y) and it diminishes abruptly outside the depletion layer; b) potential at the gate edge is nothing but the applied gate potential or built-in potential if gate biasing is zero and c) the Schottky barrier gate is ideal and the entire gate biasing is consumed in changing the gate depletion layer. A general solution of (3.33) is by separation of variables

$$W\left(x',y\right) = \left(Ae^{kx'} + Be^{-kx'}\right) \times \left(C\mathrm{cos}ky \ + D\mathrm{sin}ky \ \right) \ , \tag{3.35}$$

where $k = \sqrt{\lambda}$. The following is also a solution

$$W\left(x',y\right) = \left(Ae^{kx'} + Be^{-kx'}\right)\left(C\mathrm{cos}ky \ + D\mathrm{sin}ky \ \right) + Ex'y + Fx' + Gy + H \ , \tag{3.36}$$

where A to H are constants to be determined by the boundary conditions. At $y = 0$, potential is $-(V_g + V_{bi})$ and it does not depend on x'. This implies that $C = 0$ and $F = 0$. Thus, $H = -(V_g + V_{bi})$.

At L_1, one can write the potential as $H = -(V_g + V_{bi})$ and the potential caused by the depletion. Hence,

$$V(L_1, y) = \frac{qN_d}{\varepsilon_s}\left[y\left(h_1 - \frac{y}{2}\right)\right] - (V_g + V_{bi}) \ . \tag{3.37}$$

Here it is assumed that the depletion is increasing linearly towards the drain side under gradual channel approximation. Comparing Eqs. (3.36) and (3.37) at $x' = 0$, we have

$$(A+B) \times D\sin ky \ + Gy \ - (V_g + V_{bi}) = \frac{qN_d y h_1}{\varepsilon_s} - \frac{qN_d y^2}{2\varepsilon_s} \ - (V_g + V_{bi}) \ . \tag{3.38}$$

which gives

$$G = \frac{qN_d h_1}{\varepsilon_s} \quad and \quad A = -B \ . \tag{3.39}$$

Thus,

$$W(x', y) = 2AD\sin h\,(kx')\sin ky + Ex'y \ + \frac{qN_d h_1 y}{\varepsilon_s} - (V_g + V_{bi}) \ . \tag{3.40}$$

Differentiating (3.40)

$$\frac{\partial}{\partial y} W(x', y)\bigg|_{y=h_1} = 2AD \sin h\,(kx')\, k \cos kh_1 + Ex' + \frac{qN_d h_1}{\varepsilon_s} \ . \tag{3.41}$$

Now consider (3.34)

$$\frac{\partial}{\partial y} W(x', y)\bigg|_{y=h_1} = \frac{\partial}{\partial y} V(x', y)\bigg|_{y=h_1} + \frac{qN_d h_1}{\varepsilon_s} \ . \tag{3.42}$$

At the edges of depletion, i.e., $y = h_1$

$$\frac{\partial V(x, y)}{\partial y} = 0 \ . \tag{3.43}$$

Comparing Eqs. (3.41) and (3.42)

$$2ADk\sin h\,(kx')\cos kh_1 + Ex' + \frac{qN_d h_1}{\varepsilon_s} = \frac{qN_d h_1}{\varepsilon_s} \ . \tag{3.44}$$

Since, the above expression holds for all x', therefore, $E = 0$ and $k = (\pi/2h_1)$. Now, one can write (3.40)

$$W(x', y) = 2AD\sinh\left(\frac{\pi x'}{2h_1}\right)\sin\left(\frac{\pi y}{2h_1}\right) + \frac{qN_d h_1 y}{\varepsilon_s} - (V_g + V_{bi}) \ . \tag{3.45}$$

If we assume that E changes to E_s at $x = L_g$ or $x' = 0$, then,

$$\frac{\partial}{\partial x'}W(x', y) = 2AD\cosh\left(\frac{\pi x'}{2h_1}\right) \times \frac{\pi}{2h_1} \times \sin\left(\frac{\pi y}{2h_1}\right) \ . \tag{3.46}$$

$$\left.\frac{\partial W(x', y)}{\partial x'}\right|_{x'=0} = AD\frac{\pi}{h_1}\sin\left(\frac{\pi y}{2h_1}\right) \ . \tag{3.47}$$

Equation (3.47) represents a field, which is E_s, thus

$$E_s = -AD\frac{\pi}{h_1}\sin\left(\frac{\pi y}{2h_1}\right) \ . \tag{3.48}$$

At the boundaries of depletion, i.e., $y = h_1$ leads to

$$AD = \frac{E_s h_1}{\pi} \ . \tag{3.49}$$

Now from (3.34)

$$V(x, y) = W(x', y) - \frac{qN_d y^2}{2\varepsilon_s} \ . \tag{3.50}$$

Combining Eqs. (3.45), (3.49), (3.50) and using $x' = L_1 - L_g$ we have

$$V(x, y) = \frac{2E_s h_1}{\pi}\sinh\left[\frac{\pi(L_g - L_1)}{2h_1}\right]\sin\left(\frac{\pi y}{2h_1}\right) + \frac{qN_d h_1 y}{\varepsilon_s} - \frac{qN_d y^2}{2\varepsilon_s} - (V_g + V_{bi}) \ . \tag{3.51}$$

Towards the drain side at $x = L_g$ and $y = h_1$, one can have

$$V(L_g, h_1) = \frac{2E_s h_1}{\pi}\sinh\left[\frac{\pi(L_g - L_1)}{2h_1}\right] + \frac{qN_d h_1^2}{2\varepsilon_s} - (V_g + V_{bi}) \ . \tag{3.52}$$

Since $h_1 = au_1$ and maximum value of $x = L_g$, therefore, (3.52) can also be written as

$$V(L_g, h_1) = \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi(L_g - L_1)}{2h_1}\right] + V_P u_1^2 - (V_g + V_{bi}) \ . \tag{3.53}$$

But $(V_g + V_{bi}) = V_P u_0^2$, therefore,

$$V\left(L_g, h_1\right) = V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi\left(L_g - L_1\right)}{2au_1}\right] \quad . \tag{3.54}$$

In (3.54), $V_P(u_1^2 - u_0^2)$ represents the potential in Region-I, where carriers are moving below saturation velocity; whereas, the second term of (3.54) represents potential drop in Region-II, as shown in Fig. 3.1, where carriers are moving with saturation velocity thus, for $L_2 = L_g - L_1$

$$V(L_2) = \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_2}{2au_1}\right] \quad . \tag{3.55}$$

In Region-III, there is no gate biasing and the potential of Region-II will decay exponentially as a function of x. Let us assume that in Region-III, the depletion height is represented by h_1, as that of Region-II, which approaches to an insignificant value after distance L_3. Under these assumptions, Region-III potential can be approximated as

$$V(L_3) \approx \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_3}{2au_1}\right] \approx \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_g}{8au_1}\right] \quad , \tag{3.56}$$

where L_3 represents the width of Region-III, which for submicron devices can be written as $L_3 \sim L_g/4$ [130, 141]. Now the potential distribution inside the channel of a SiC MESFET can be summarized as

$$V(L_1) + V(L_2) + V(L_3) = V_d \ . \tag{3.57}$$

or

$$V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi\left(L_g - L_1\right)}{2au_1}\right] + \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_g}{8au_1}\right] = V_d \ . \tag{3.58}$$

To solve (3.58) for u_1, after making substitution for L_1 from (3.30), we define a function $f(u_1)$ as

$$f(u_1) = V_P\left(u_1^2 - u_0^2\right) + \left(\frac{2E_s a u_1}{\pi}\right)$$

$$\sinh\left[\left(\frac{\pi L_g}{2au_1}\right) - \left(\frac{\pi L_g z}{2au_1}\right)\frac{(u_1^2 - u_0^2) - (2/3)\left(u_1^3 - u_0^3\right)}{\gamma(1-u_1) - (u_1^2 - u_0^2)}\right] \tag{3.59}$$

$$+\left[\frac{2E_s a u_1}{\pi}\sinh\left(\frac{\pi L_g}{8au_1}\right)\right] - V_d = 0\ .$$

Consider $f(u_1) = f_1 + f_2$ such that

$$f_1 = V_P(u_1^2 - u_0^2) + \left[\frac{2E_s a u_1}{\pi}\sinh\left(\frac{\pi L_g}{8au_1}\right)\right]\ . \tag{3.60}$$

and

$$Df_1 = 2V_P u_1 + \left(\frac{2E_s a}{\pi}\right)\sinh\left(\frac{\pi L_g}{8au_1}\right) + \frac{2E_s a u_1}{\pi}\cosh\left(\frac{\pi L_g}{8au_1}\right)\left(\frac{-\pi L_g}{8au_1}\right)\ . \tag{3.61}$$

also

$$f_2 = \left(\frac{2E_s a u_1}{\pi}\right)\sinh\left[\left(\frac{\pi L_g}{2au_1}\right) - \left(\frac{\pi L_g z}{2au_1}\right)\frac{(u_1^2 - u_0^2) - 2/3(u_1^3 - u_0^3)}{\gamma(1-u_1) - (u_1^2 - u_0^2)}\right]\ . \tag{3.62}$$

and

$$Df_2 = \left(\frac{2E_s a}{\pi}\right)\sinh\left[\left(\frac{\pi L_g}{2au_1}\right) - \left(\frac{\pi L_g z}{2au_1}\right)\frac{(u_1^2 - u_0^2) - 2/3(u_1^3 - u_0^3)}{\gamma(1-u_1) - (u_1^2 - u_0^2)}\right] + \left(\frac{2E_s a u_1}{\pi}\right)$$

$$\times\cosh\left[\left(\frac{\pi L_g}{2au_1}\right) - \left(\frac{\pi L_g z}{2au_1}\right)\frac{(u_1^2 - u_0^2) - 2/3(u_1^3 - u_0^3)}{\gamma(1-u_1) - (u_1^2 - u_0^2)}\right] \times Df_3\ , \tag{3.63}$$

where

$$Df_3 = \left[\left(\frac{-\pi L_g}{2au_1^2} \right) + \left(\frac{\pi L_g z}{2au_1^2} \right) \left(\frac{(u_1^2 - u_0^2) - 2/3(u_1^3 - u_0^3)}{\gamma(1-u_1) - (u_1^2 - u_0^2)} \right) - \left(\frac{\pi L_g z}{2au_1} \right) \right.$$

$$\left. \left(\frac{[\gamma(1-u_1) - (u_1^2 - u_0^2)].[2u_1 - 2u_1^2] - [-\gamma - 2u_1].[(u_1^2 - u_0^2) - 2/3(u_1^3 - u_0^3)]}{[\gamma(1-u_1) - (u_1^3 - u_0^3)]^2} \right) \right]. \tag{3.64}$$

Now the Newton's iterative method [142, 143] having definition $u_{(n+1)} = u_n - f(u_n)/Df(u_n)$ can be employed to find u_1. This evaluation would be for $V_d \geq V_{d(\text{sat})}$ and for the devices having short L_g to ensure that the observed current saturation is caused by velocity saturation of the carriers. Thus, the proposed model may not be valid for long-channel devices wherein the current saturation is usually observed after attaining the pinch-off condition. Further, the validity of the proposed model will be limited to the biasing conditions that maintain the device operation prior to the onset of avalanche breakdown.

Figure 3.4 shows potential accumulation in all the three regions of the device. Figure 3.4(a) represents potential drop in Region-I for a SiC submicron MESFET. The figure is plotted using (3.23) and it shows a non-uniform variation in between two consecutive curves while changing V_g from 0 to -8V. This can be explained by the nonlinear dependence of h on V_g as evident from (3.7). Also in Fig. 3.4(a), the magnitude of the potential in Region-I is decreasing by increasing V_d. This can only be possible if u_1 of (3.23) exhibits a decreasing trend with increasing magnitude of V_d. This is because of the fact that with increasing V_d the carriers will attain saturation velocity relatively early thus, reducing the overall length of L_1.

Figure 3.4(b) is attained using (3.55) and it represents the potential drop for Region-II, where carriers are moving with saturation velocity, v_s. The examination of the figure shows that by increasing V_d, there is a linear increase in potential accumulation in Region-II. The start of the drain voltages in Fig. 3.4(b) is after meeting $V_d = V_{d(\text{sat})}$ condition, and the total magnitude of the potential is dependent upon both V_d and V_g. Thus, for a higher magnitude of V_g, Region-II will hold

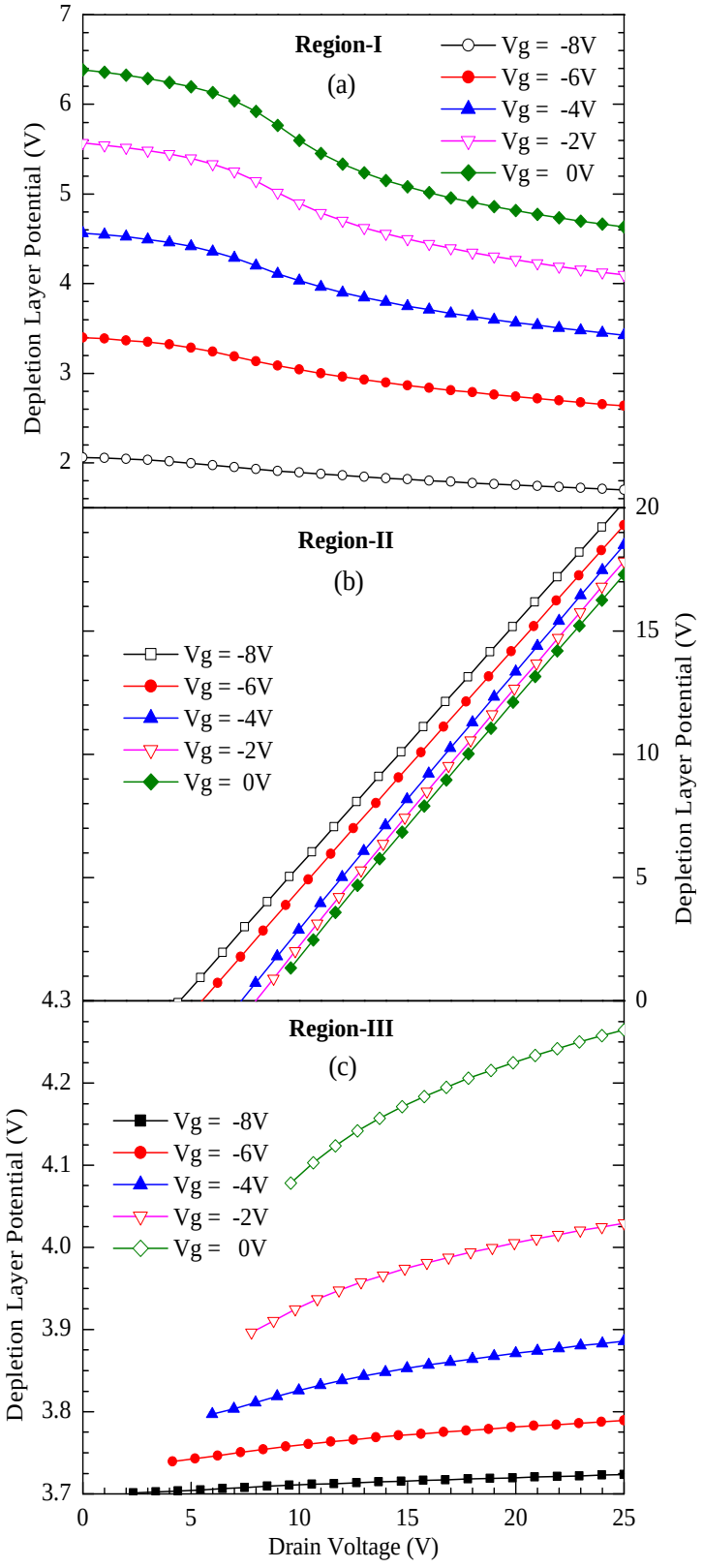


FIGURE 3.4: Depletion layer potential underneath the Schottky barrier gate of a submicron SiC MESFET.

more potential after the onset of current saturation, which is evident from Fig. 3.4(b).

Assuming that the extension of the depletion layer towards the drain side of a submicron SiC MESFET follows quarter circle approximation [141], i.e., $L_3 = L_g/4$. One can estimate the potential drop of Region-III by employing (3.56) as shown in Figure 3.4(c). It is obvious from the figure that there is an enhancement of Region-III potential after the onset of current saturation such that its magnitude is relatively less dependent on the device biasing. For the entire change in V_d and V_g, the total observed variation in $V(L_3) \sim 0.5V$. But, the important point to note is that the potential drop in Region-III is ∼4V which is a significant value and cannot be neglected in the device modeling.

It is pertinent to mention here that the potential variation with respect to V_d, underneath the Schottky barrier gate, is a continuous function for all the three regions discussed hitherto. In Region-I, prior to the velocity saturation, some variation in the magnitude of potential is observed which presumably is due to the drifting of h_1 towards the source side with increasing values of V_d. Whereas, in Region-II, potential increases linearly till the termination of the region. On the other hand, in Region-III, as evident from Fig. 3.4(c), potential variation as a function of V_d is nominal. However, its magnitude is significant, thus, cannot be overlooked in the device modeling.

A two-region analytical model as proposed by Murray et al. [29] works reasonably well for low current (less than ∼10 mA) SiC MESFET. However, it fails for large current devices (∼50 mA or above) which is usually the case for SiC power MESFET. By incorporating the potential drop of Region-III, Zhu et al. [30] has modified Murray model and demonstrated its improved performance over two-region model for relatively large current SiC MESFETs. In this study, the performance of the Zhu et al. model is further improved by incorporating the concept of depletion layer modification after the onset of current saturation.

3.4 Modeled $I-V$ Characteristics

A submicron SiC MEFET with device parameters as listed in Table 3.2 has been selected [30]. A MATLAB code is developed using Eqs. (3.13) and (3.19) for the conditions shown below.

$$I_{d(\text{linear})} = \frac{I_p\left[3\left(u_d^2-u_0^2\right)-2\left(u_d^3-u_0^3\right)\right]}{1+z\left(u_d^2-u_0^2\right)} \text{ for } V_d < V_{d(\text{sat})}$$
$$\text{and} \tag{3.65}$$
$$I_{d(\text{sat})} = qN_dWa\gamma\upsilon_s\left(1-u_1\right) \text{ for } V_d > V_{d(\text{sat})} \ .$$

In Eqn. (3.65), u_1 is a constant as defined by the Zhu and Murray models, and the same is evaluated at $V_d = V_{d(\text{sat})}$. Contrarily our study showed that u_1 is a variable, which can be evaluated using Eqn. (3.65) for $V_d \geq V_{d(\text{sat})}$ and the evaluated data can subsequently be employed to assess $I_{d(\text{sat})}$ by involving Eqn. (3.65).

Further, the effects of parasitic resistances R_s, R_d and R_b have been incorporated by using

$$V_{ds} = V_d + I_d(R_s + R_d) \ , \tag{3.66}$$

where

$$R_s = \frac{L_s}{N_dq\mu aW} + R_c$$
$$\tag{3.67}$$
$$R_d = \frac{(L_d - L_3)}{N_dq\mu aW} + R_c \ ,$$

where L_s and L_d represent separation between source-gate and drain-gate respectively, and R_c is the contact resistance. For $\mu = 300cm^{-2}/Vs$, and $R_c \sim 1.5\Omega$, the calculated values of R_s and R_d were 5.7Ω and 10.3Ω respectively. The drain-to-source current, I_{ds} was then evaluated by using

$$I_{ds} = I_d + V_{ds}/R_b \ . \tag{3.68}$$

and

$$V_{gs} = V_g + I_g(R_s) \ . \tag{3.69}$$

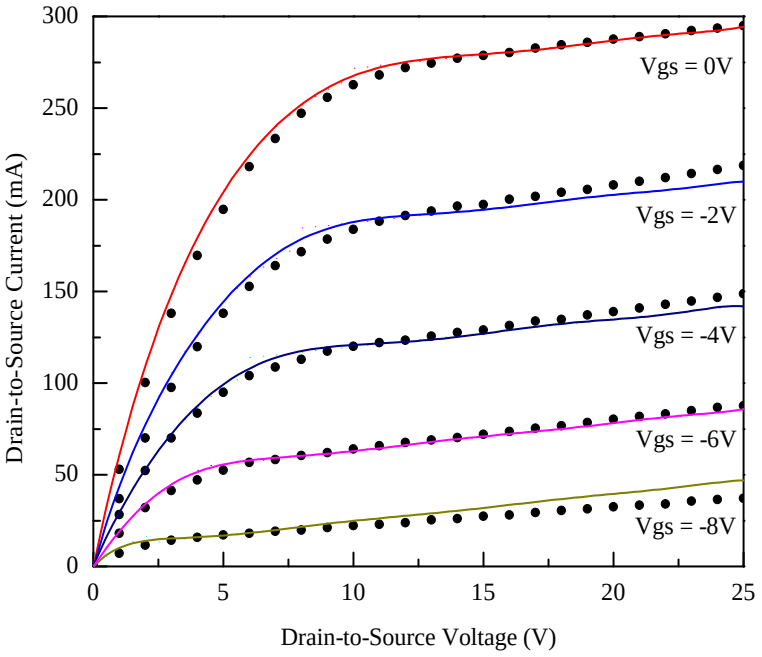


FIGURE 3.5: Modeled (−) and measured (•) output characteristics of a submicron SiC MESFET.

where for submicron devices $I_g \sim 10^{-9}A$ [134] and the buffer layer resistance, R_b, was evaluated using background doping as $10^{15}cm^{-3}$ [130] and found as $R_b \sim 2k\Omega$.

Modeled and observed output characteristics of the chosen device are shown in Fig. 3.5. It is pertinent to mention here that the modeled output characteristics showed some discrepancies, especially near the pinch-off region. Analytical models as presented in [29, 30] assumed that the depletion layer at location L_1 remains constant after the onset of current saturation and any increase in the current afterwards, would be associated with buffer layer conductance which has been incorporated in the model by R_b. Apart from the buffer layer conductance, our study showed that there is an increase in the potential drop after the onset of current saturation in Region-II, as well as in Region-III as evident from Fig. 3.4, which can potentially effect modeled output characteristics of a SiC MESFET.

By involving (3.30) and (3.58) one can evaluate the behavior of L_1 and u_1 as a function of applied potential. Fig. 3.6 shows variation in u_1 after the onset of the current saturation. This figure clearly depicts that the depletion layer at the point

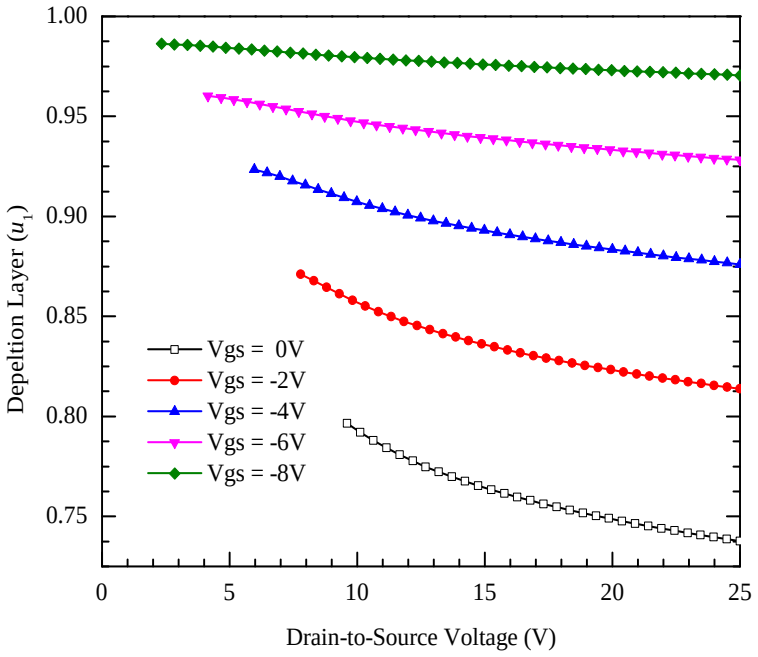


FIGURE 3.6: Variation in depletion layer after the onset of current saturation in a SiC MESFET.

of saturation does not stay constant after the onset of current saturation; rather, it decreases with increasing values of V_{ds}.

Additionally, it is shown in Fig. 3.7 that the saturation length L_1 is dependent on both V_{ds} and V_{gs} of the device. A careful examination of Fig. 3.7 reveals that for $L_1/L_g > 1$, carriers are attaining the saturation velocity after traveling the entire Schottky barrier gate, i.e., up to Region-III of the device. By increasing V_{ds}, x-directed field inside the channel also increases resulting in the shifting of L_1 toward Region-II, which brings $L_1/L_g < 1$. Assuming that the current saturation in a short channel SiC MESFET is due to the velocity saturation of carriers [29, 30], one can conclude that the point where these carriers are attaining saturation velocity is bias dependent, and it shifts towards the source side with increasing magnitude of V_{ds}.

Shifting of L_1 towards the source side of the depletion as observed in Fig. 3.7, can be associated with the fact that by increasing V_{ds} the saturation point is gradually shifting towards the source and u_1 is thus decreasing as seen in Fig. 3.6. As a result there is an increase in the channel cross-sectional area available for the flow

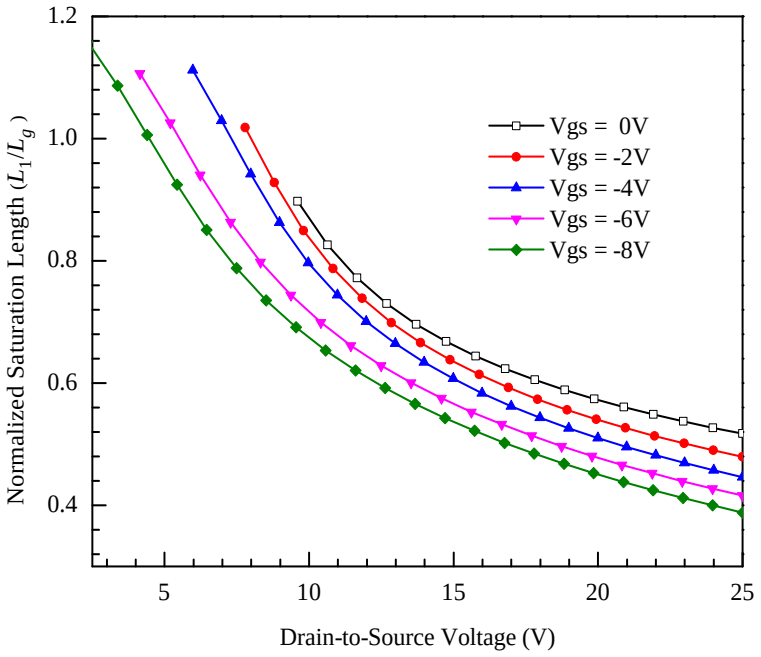


FIGURE 3.7: Shows shifting of saturation length L_1 towards source side of the gate after the onset of current saturation in a SiC MESFET.

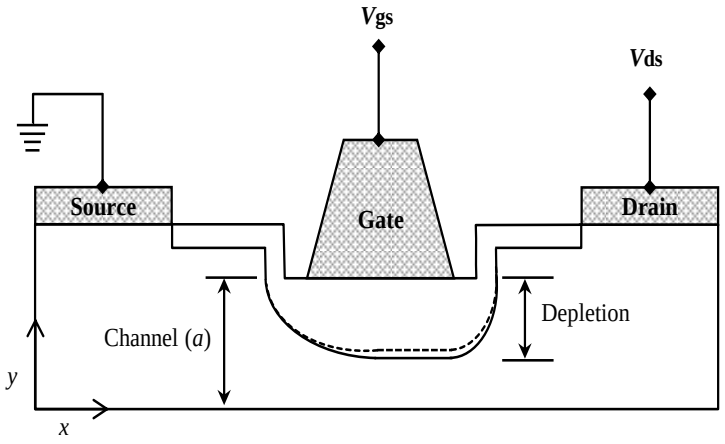


FIGURE 3.8: A crossectional view of an operating SiC MESFET where a dotted line shows reduction in gate depletion layer with increased drain biasing.

of current as illustrated in Fig. 3.8. It has been shown in the figure that with the shifting of saturation point towards the source side of Schottky barrier gate, the channel is slightly widened and the same is represented in the figure by the dotted line. This plausible explanation will lead to an obvious conclusion that finite output conductance in the saturation region of operation, may be associated with depletion layer modification with increasing drain biasing [144].

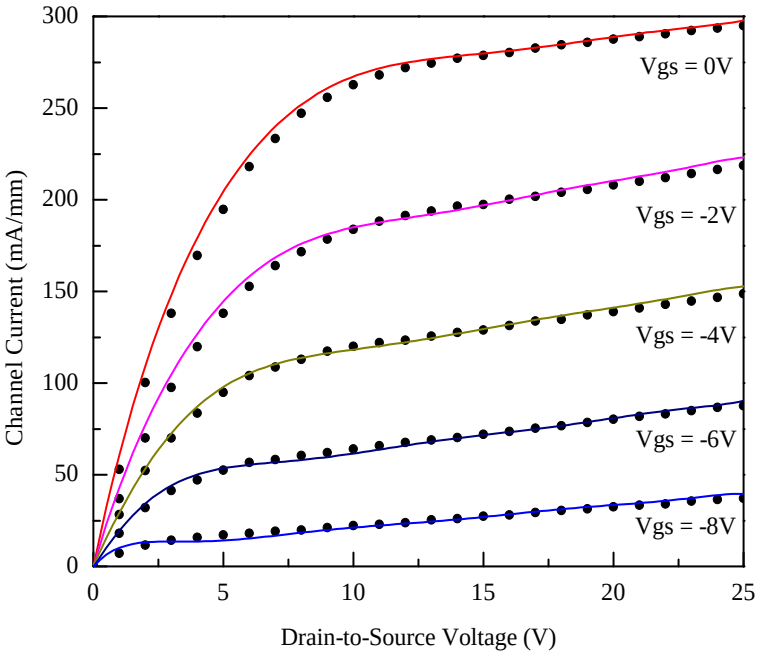


FIGURE 3.9: Output characteristics of a submicron SiC MESFET: measured (•) and modeled (−) with proposed depletion layer modification technique.

TABLE 3.3: Comparison of RMS errors for conventional and proposed modeling technique for the device parameters listed in Table 2.

Model	V_{gs} **= 0V**	V_{gs} **= -2V**	V_{gs} **= -4V**	V_{gs} **= -6V**	V_{gs} **= -8V**	**Avr.RMSE**
Zhu et al. [30]	12.36×10^{-3}	9.48×10^{-3}	5.52×10^{-3}	3.13×10^{-3}	5.28×10^{-3}	7.15×10^{-3}
Proposed	12.36×10^{-3}	8.57×10^{-3}	4.60×10^{-3}	2.87×10^{-3}	1.67×10^{-3}	6.01×10^{-3}

By incorporating the depletion layer modification concept as discussed hitherto, the device of Table 3.2 is again modeled, and the result is shown in Fig. 3.9. A visual comparison of Fig. 3.5 and 3.9 clearly shows a tangible improvement in the modeled characteristics of Fig. 3.9, especially in the saturation region of operation. In Fig. 3.5 at V_{gs} ∼-8V, i.e., near to the pinch-off, there is a relatively higher discrepancy in the observed and modeled characteristics. By looking at Fig. 3.9 for the same curve (V_{gs} = -8V), one can clearly gather that this discrepancy has been adequately addressed.

Table 3.3 provides a comparison between the conventional approach and the one which has been adopted in this research. The table presents RMS errors for each I_{ds}

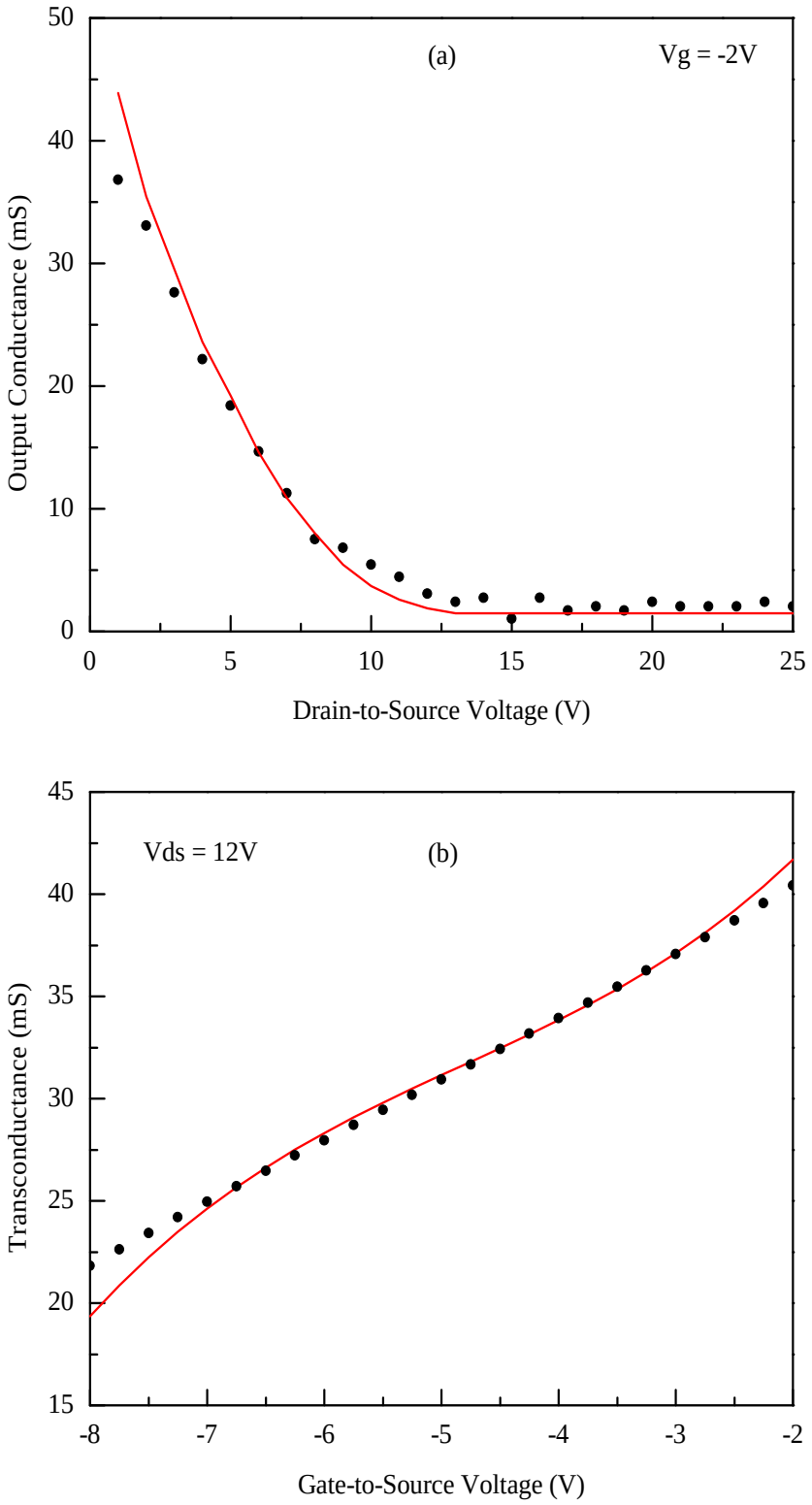


FIGURE 3.10: Modeled (−) and measured (•) (a) output conductance and (b) transconductance of a submicron SiC MESFET.

curve for the device under discussion. The data of the table clearly demonstrates that the proposed technique offers an improvement in SiC MESFET modeling. From average RMSE values one can calculate that the proposed technique is 15.9% better than its counterpart.

Figure 3.10 shows modeled and experimental g_d and g_m of the device under discussion. It can be seen from the figure that the modeled characteristics, in both the cases, follow reasonably well the experimental data. This once again shows the validity of the proposed model to simulate submicron SiC MESFETs characteristics including g_d and g_m. It is a well known fact that g_d of a submicron device is the most unpredictable variable and to estimate its value at a given biasing is considered as the tedious part of the device modeling. Figure 3.10(a) shows that the proposed technique exhibited a reasonably good agreement between the experimental and the modeled g_d characteristics. Since g_d and g_m characteristics are primarily based upon the output DC characteristics shown in Fig. 3.9, which demonstrated the validity of the proposed technique hence, its derivative; represented in the form of g_d and g_m and shown in Figs. 3.10(a) and 3.10(b), respectively.

3.5 Summary

This chapter presents a detailed mathematical model describing $I-V$ characteristics of submicron SiC MESFETs. Poisson's equation with appropriate boundary conditions has been solved to determine potential distribution inside the channel. Location (L_1) of Schottky barrier gate with a corresponding depletion layer width (u_1) where the carrier's velocity gets saturated has been evaluated. It has been demonstrated that, both L_1 and u_1 are biased dependent, and their values are changing by changing drain biasing even after the onset of current saturation. This causes a modification in the depletion layer underneath the Schottky barrier gate and, thus, changes the available channel crossection for the flow of current.

It has been shown that finite output conductance in the saturation region of operation, which is usually observed in submicron devices, can be explained with Schottky barrier depletion layer modification.

$I-V$ characteristics of submicron SiC MESFET are modeled and compared with conventional velocity saturation technique, where the depletion layer after the onset of current saturation has been treated as constant. It is observed that the proposed technique gave $\sim$15.9% improvement in the modeled out characteristics of a submicron SiC MESFET.

Chapter 4

An Improved Model for Current-Voltage Characteristics of Submicron SiC MESFETs

This chapter presents an improved model to simulate $I-V$ characteristics of submicron SiC MESFETs, designed for microwave power applications. The proposed model adequately addresses a non-ideal Schottky behavior, commonly observed in submicron devices, by adjusting the device biasing through simulation variables. Swarm optimization technique has been applied to investigate gate length (L_g) dependent performance of various SiC MESFETs models. It has been found that the proposed model provides an improved accuracy, ranging from 7 % to 24 %, compared to the best models available in the literature. This enhanced performance is primarily associated with the extra control, provided by the proposed model to simulate the movement of the depletion region in the channel as a function of applied voltages. An attempt has been made to identify the location underneath the Schottky barrier gate, where the depletion region gets its maximum height and thus controls the saturation current of the channel. Physical and electrical parameters of various SiC MESFETs having $L_g = 0.4$ μm, 0.5 μm, 0.6 μm and 0.7 μm have also been assessed. An accurate assessment of the physical parameters of the device exhibits the validity of the model for submicron SiC MESFETs.

4.1 Introduction

Silicon Carbide (SiC) MESFETs have shown a great potential in microwave power applications, mainly because of their material properties. Since their inception in the mid-eighties, these devices have improved significantly over a period of time [145]. Today SiC MESFETs offer high power density, high operating voltage and high operating temperature, compared to Si and GaAs based FETs. Moreover, the operating frequency of SiC MESFETs has also improved, and submicron devices can comfortably work in X-band with CW power density as high as 7.8 W/mm [53].

The superior high power performance of SiC MESFETs is primarily associated with the properties offered by SiC which include: a) wide band gap; b) high electron saturation velocity; c) high thermal conductivity and d) high break down electric field. The high operating voltages, on the one hand, provided capability to SiC MESFETs to handle large power, but, on the other hand, it imposed stringent conditions on the device fabrication and physical geometry to realize its intended performance [42, 43, 49, 146, 147].

A simple way to improve the high frequency performance of a SiC MESFET is to reduce its gate length, L_g, as this improves its unity gain frequency, f_T as [148]:

$$f_T = \frac{g_m}{2\pi C_{gs}} \ , \tag{4.1}$$

where g_m is the extrinsic transconductance and C_{gs} is gate to source capacitance. However, reduction in L_g, especially to submicron dimensions, enhances the short channel effects namely: a) shift in threshold voltage, V_T; b) increase in output conductance, g_d, in the saturation region of operation; c) compression in g_m and d) an early self-regulating break down [149].

For S-band applications, Clark and Palmour fabricated $L_g = 0.7$ μm SiC MESFETs and their AC and power characteristics were investigated [3]. Gang *et al.* reported $L_g = 0.6$ μm SiC MESFETs and investigated their pulsed $I-V$ response to determine the effects of self-heating on its DC characteristics [53]. Song *et al.*

fabricated $L_g = 0.5$ μm SiC MESFETs and investigated effects of buffer layer thickness on the device breakdown [41]. Hjelmgren *et al.* fabricated and studied electro-thermal simulation of microwave SiC MESFETs having $L_g = 0.4$ μm. Their devices exhibited self-regulating break down much earlier than the channel pinch-off [13, 21].

Assessment of $I-V$ characteristics of a SiC MESFET is the first step to establish the quality of a device. An accurate assessment of the device $I-V$ characteristics will enable a design engineer to use the device successfully in microwave power amplifiers [150, 151]. There are two main techniques which can be employed to predict the device performance: The first one is the analytical approach which employs the device physics and predicts the output characteristics with nominal or zero fitting variables, whereas the second one is referred to as the empirical or the semi-empirical approach. A semi-empirical, contrary to an empirical approach, is preferred because it involves the ease inherent to an empirical modeling and uses basic variables defining the device characteristics without getting involved into complicated mathematical solutions [129, 132].

There are numerous non-linear models available in the literature with the claim to simulate $I-V$ characteristics of SiC MESFETs [31, 126–128, 152–158]. In this chapter, as a first part, the accuracies of these models have been investigated for $L_g = 0.4$ μm, 0.5 μm, 0.6 μm and 0.7 μm SiC MESFETs. To accomplish this, a device simulator was developed in MATLAB involving particle swarm optimization. In order to know the relative performance of a model, simulated characteristics were then compared with experimental data to assess biased dependent RMS errors. Further, in the 2$^{\text{nd}}$ part of this chapter, a new model is proposed and its gate length dependent performance has been evaluated. It has been demonstrated that the proposed model has the ability to simulate $I-V$ characteristics of submicron SiC MESFETs with an accuracy better than the earlier reported data. It is further demonstrated that the proposed model works equally well to generate static as well as pulsed $I-V$ characteristics of a SiC MESFET.

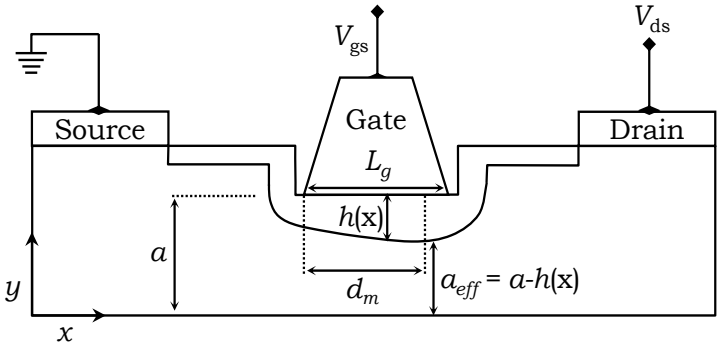


FIGURE 4.1: Crossectional view of a SiC MESFET.

The organization of the remaining part of the chapter is as follows: Section-2 describes the model development whereas, Section-3 contains $I-V$, g_d and g_m characteristics of submicron devices simulated by employing swarm optimization technique. Section-4 presents a comparison of RMS error values of different models, evaluated for the devices under discussion and assessment of their variables thereof. The last section presents the conclusions drawn from this study.

4.2 Model Development

As shown in Fig. 4.1, Schottky barrier height of a SiC MESFET as a function of its biasing parameters is given by:

$$h(x) = \sqrt{\frac{2\epsilon(E_s L_g - V_{gs} + V_{bi})}{qN_d}} \ , \tag{4.2}$$

where ϵ is the relative permittivity of SiC, E_s is the saturation field, V_{gs} is the gate to source potential, V_{bi} is the built-in potential, N_d is the channel doping and q represents the electronic charge. The current flowing through the available channel after the onset of current saturation is defined as:

$$I_{dss} = qN_d v_s[a - h(x)]W \ , \tag{4.3}$$

TABLE 4.1: Physical parameters of submicron SiC MESFET.

Ref. No.	L_g (μm)	W (μm)	a (μm)	N_d
Ref [3]	0.7	250	0.22	3.0×10^{17}
Ref [53]	0.6	200	0.22	3.0×10^{17}
Ref [41]	0.5	400	0.30	1.5×10^{17}
Ref [21]	0.4	200	0.20	2.7×10^{17}

where I_{dss} is saturation drain current at $V_{gs} = 0$ V, a is the channel epi-layer thickness, v_s is the saturation velocity of electrons and W represents the width of the device. According to Schokley, the FET drain current, I_{ds} in the saturation region of operation as a function of V_{gs} and V_T can be represented by a non-linear expression given by [159]:

$$I_{ds} = I_{dss}(1 - V_{gs}/V_T)^2 \ . \tag{4.4}$$

In submicron devices, there is a shift in V_T, caused by the submicron geometry of the device, which is represented by ΔV_T. Thus, the modified representation of the threshold voltage is $V_T + \Delta V_T$. Further, due to finite conductance in the saturation region of operation, V_T of a device also depends on drain to source voltage, V_{ds}, therefore, V_T of a device can be simulated more effectively by writing its expression as $V_T + \Delta V_T + \gamma V_{ds}$ where γ is a fitting variable. Thus, one can write:

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \ . \tag{4.5}$$

In submicron devices, a non-ideal Schottky barrier response is a commonly observed phenomenon and with its presence it is very hard to simulate the device characteristics to a reasonable accuracy [129]. The presence of interface states consumes a finite amount of potential which can be incorporated into the model by adjusting V_{gs} as:

$$I_{ds} = I_{dss}\left(1 - \frac{\delta V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \ , \tag{4.6}$$

where δ is an adjustment factor for interface states. To incorporate the simulation of linear region, (4.6) is multiplied with $\tanh(\alpha V_{ds})$, where α represents the slope of $I-V$ characteristics of SiC MESFET for linear region. Further, the finite output value of g_d after the onset of current saturation and its dependence on V_{ds} and V_{gs} is simulated by $[1+\lambda V_{ds}+\delta V_{gs}/V_{ds(\text{sat})}]$, where λ is a fitting variable and $V_{ds(\text{sat})}$ is the value of V_{ds} where I_{ds} saturates. Thus, (4.6) is modified accordingly as:

$$I_{ds} = I_{dss}\left(1-\frac{\delta V_{gs}}{V_T+\Delta V_T+\gamma V_{ds}}\right)^2 \times \left(1+\lambda V_{ds}+\frac{\delta V_{gs}}{V_{ds(\text{sat})}}\right)\tanh(\alpha V_{ds})\ , \quad (4.7)$$

where

$$V_T = V_{bi} - \frac{qN_d a^2}{2\epsilon}\ . \quad (4.8)$$

Instead of using the values of I_{dss} and V_T determined from (4.3) and (4.8) respectively, one can also evaluate these two variables by an optimization process. Thus, we can redefine these variables of (4.7) as:

$$I_{ds} = \psi\left(1-\frac{\delta V_{gs}}{\xi V_T+\Delta V_T+\gamma V_{ds}}\right)^2 \times \left(1+\lambda V_{ds}+\frac{\delta V_{gs}}{V_{ds(\text{sat})}}\right)\tanh(\alpha V_{ds})\ , \quad (4.9)$$

where ψ and ξV_T are the assessed values of I_{dss} and V_T respectively, for a given device through an optimization process.

To simulate g_d and g_m, (4.9) was differentiated with respect to V_{ds} and V_{gs} respectively, which yielded:

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs(\text{const})}} = \psi\left(1-\frac{\delta V_{gs}}{\xi V_T+\Delta V_T+\gamma V_{ds}}\right)$$

$$\times\left\{\left(1-\frac{\delta V_{gs}}{\xi V_T+\Delta V_T+\gamma V_{ds}}\right)\times\left[\lambda\tanh(\alpha V_{ds})+\alpha\left(1+\lambda V_{ds}+\frac{\delta V_{gs}}{V_{ds(\text{sat})}}\right)\right.\right.$$

$$\left.\left.\times\,\text{sech}^2(\alpha V_{ds})\right]+2\left(1+\lambda V_{ds}+\frac{\delta V_{gs}}{V_{ds(\text{sat})}}\right)\times\frac{\delta\gamma V_{gs}\tanh(\alpha V_{ds})}{(\xi V_T+\Delta V_T+\gamma V_{ds})^2}\right\}\ . \quad (4.10)$$

TABLE 4.2: Shows values of different parameters of (4.9) for submicron SiC MESFETs.

Variables	0.7 μm	0.6 μm	0.5 μm	0.4 μm
$\alpha(1/V)$	0.3402	0.1535	0.1838	0.1277
$\lambda(1/V)$	0.0402	0.0125	0.0253	0.0053
ψ (mA/mm)	296.38	322.89	187.22	427.64
$V_T(V)$	-10.00	-15.00	-12.00	-20.00
γ	0.1051	0.0646	0.1217	0.0633
Δ	-0.2471	0.0017	-0.6623	-0.0988
δ	-0.5110	-0.6229	-1.0409	-0.2148
ξ	-0.2046	-0.6275	-0.2620	-0.0603

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V\,ds(\text{const})} = \psi \tanh(\alpha V_{ds}) \left(1 - \frac{\delta V_{gs}}{\xi V_T + \Delta V_T + \gamma V_{ds}}\right) \times \left\{\frac{\delta}{V_{ds(\text{sat})}} - \frac{2\delta(1+\lambda V_{ds})}{\xi V_T + \Delta V_T + \gamma V_{ds}} - \frac{3\delta^2 V_{gs}}{(\xi V_T + \Delta V_T + \gamma V_{ds}) V_{ds(\text{sat})}}\right\}. \tag{4.11}$$

In brief, (4.9) can be employed to simulate output characteristics of SiC MESFETs whereas, (4.11) defines their transfer characteristics. In these expressions, the effect of parasitic source (R_s) and drain (R_d) resistances were taken care of by the variables α and λ, respectively. Further, (4.9) is a quadratic equation which complies to the fundamental Schokly expression and it represents adequately the device characteristics before its breakdown.

4.3 Simulation

To demonstrate the validity of the proposed model, submicron SiC MESFETs of various L_g were chosen and the detail of which is given in Table 4.1. A MATLAB simulator was developed wherein the respective model equations were used [31, 126–128, 152–157]. Optimization of different variables of a model has been carried

out using Particle Swarm Optimization (PSO) technique and a brief of which is as under [160, 161].

PSO was initialized with random position and velocity for the parameters which were to be optimized. Positions were initialized within a boundary defined by x_{max} and x_{min} and the velocity was initialized somewhere between 0 to v_{max}, where v_{max} is given by:

$$v_{max} = \frac{x_{max} - x_{min}}{2} \ . \tag{4.12}$$

For an n-dimensional problem with m number of particles and for k^{th} iteration, the positions were represented by:

$$X^k = \begin{bmatrix} x_{11}^k & x_{12}^k & \dots & x_{1j}^k & \dots & x_{1n}^k \\ x_{21}^k & x_{22}^k & \dots & x_{2j}^k & \dots & x_{2n}^k \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ x_{i1}^k & x_{i2}^k & \dots & x_{ij}^k & \dots & x_{in}^k \\ \vdots & \vdots & \dots & \vdots & \ddots & \vdots \\ x_{m1}^k & x_{m2}^k & \dots & x_{mj}^k & \dots & x_{mn}^k \end{bmatrix} \tag{4.13}$$

where m is swarm size and n is swarm dimension. The associated velocities of these particles were represented as:

$$V^k = \begin{bmatrix} v_{11}^k & v_{12}^k & \dots & v_{1j}^k & \dots & v_{1n}^k \\ v_{21}^k & v_{22}^k & \dots & v_{2j}^k & \dots & v_{2n}^k \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ v_{i1}^k & v_{i2}^k & \dots & v_{ij}^k & \dots & v_{in}^k \\ \vdots & \vdots & \dots & \vdots & \ddots & \vdots \\ v_{m1}^k & v_{m2}^k & \dots & v_{mj}^k & \dots & v_{mn}^k \end{bmatrix} \tag{4.14}$$

Modification of the particle position was realized by using the current position and the velocity information as defined by:

$$X^{k+1} = V^{k+1} + X^k \ , \tag{4.15}$$

where X^{k+1} was the modified position and V^{k+1} was the modified velocity. The velocity of a particle was calculated by the equation:

$$v_{ij}^{k+1} = w_{ij}v_{ij}^{k} + v_{p\text{best}} + v_{g\text{best}} \ , \tag{4.16}$$

where the term $w_{ij}v_{ij}^{k}$ was called inertia and it specified the velocity which was retained from the previous step. The 2$^{\text{nd}}$ term $v_{p\text{best}}$ of (4.16) was given by:

$$v_{p\text{best}} = c_1 \times \Phi_1 \times (p_{\text{best}}{}_{ij}^{k} - x_{ij}^{k}) \ . \tag{4.17}$$

The 3$^{\text{rd}}$ term $v_{g\text{best}}$ of (4.16) represented global velocity referred to as social influence which was defined by:

$$v_{g\text{best}} = c_2 \times \Phi_2 \times (g_{\text{best}} - x_{ij}^{k}) \ . \tag{4.18}$$

In (4.16) to (4.18) x_{ij}^{k} represented current position of a particle at k^{th} iteration, v_{ij}^{k} current velocity of a particle, v_{ij}^{k+1} modified velocity, Φ_1 and Φ_2 random numbers between 0 and 1, $p_{\text{best}}{}_{ij}^{k}$ personal best, g_{best} global best and w_{ij} weighting factor of the velocity of a particle at position x_{ij}.

Further, c_1 was a cognitive parameter and represented individual best success so far whilst c_2 was a social parameter and neighbor best success so far. Increasing c_1 encourages each particle to move towards its own p_{best} while increasing c_2 encourages exploration of g_{best}. In our simulation the values of c_1 and c_2 were changed iteratively by using following expression:

$$c_1 = c_{1\text{max}} + \frac{c_{1\text{max}} - c_{1\text{min}}}{\text{max.iter}}(\text{max.iter} - k) \ . \tag{4.19}$$

$$c_2 = c_{2\text{max}} + \frac{c_{2\text{max}} - c_{2\text{min}}}{\text{max.iter}}(\text{max.iter} - k) \ . \tag{4.20}$$

The convergence of PSO was achieved by devising an objective function given by:

$$\varepsilon = \sqrt{\sum_{Q=1}^{N}\left\{\sum_{P=1}^{M}\left(I_{ds(\text{exp})}^{P,Q} - I_{ds(\text{sim})}^{P,Q}\right)^2 \Bigg/ \sum_{P=1}^{M} I_{ds(\text{exp})}^{P,Q}\right\}} \ . \tag{4.21}$$

And the root mean square error (RMSE) between the simulated and the experimental data was assessed by using:

$$\text{RMSE} = \sqrt{\frac{1}{M}\sum_{P=1}^{M}\left(I^{P}_{ds(\text{exp})} - I^{P}_{ds(\text{sim})}\right)^{2}}\,. \tag{4.22}$$

In (4.21) P represents steps in V_{ds} starting from zero to its maximum biasing value given by M, whereas Q represents number of steps in V_{gs} with its highest number given by N. To avoid discontinuity, which may be caused by the denominator of the square term of (4.9), optimization variables' bounds were defined to ensure the convergence and the same was observed routinely.

Following steps were used in the implementation of PSO algorithm:

1. define swarm dimension and size with initialized position and velocity;
2. define objective function for error estimation;
3. update each particle's position using (4.15);
4. obtain personal best, p_{best} (according to the particle's previous best positions) with the help of defined objective function;
5. obtain global best, g_{best};
6. update velocity based on previous best and global best positions through (4.16);
7. terminate if stopping criteria are satisfied, otherwise go to step 3.

Fig. 4.2 shows experimental and simulated $I - V$ characteristics of four SiC MESFETs having submicron gate lengths but of varying geometry and doping density as given in Table 1. Simulation was carried out using (4.9) whereas, the variables of the equation were optimized using PSO algorithm discussed hitherto. The values of different variables of (4.9) which were achieved repeatedly after several executions of PSO are listed in Table 4.2.

Fig. 4.3 shows simulated and experimental g_d characteristics for the devices under discussion. Simulation was carried out by using (4.10) and the respective device data is listed in Table 4.2. The plots show that the experimental data is of scattered nature but it follow a definite pattern in which it exhibit a rapid decline in g_d magnitude and subsequently it attain a saturation value.

Fig. 4.4 shows dependence of g_m on V_{ds} and V_{gs} for submicron SiC MESFETs. The figure shows that each device, dependent upon its channel conditions and Schottky barrier quality, offers a unique response. It is pertinent to mention that the simulated g_m characteristics of Fig. 4.4 are attained by employing (4.11) which exhibited a good agreement to the experimental data for entire V_{gs} biasing.

4.4 Discussion

Examination of Fig. 4.2 clearly reveals that the proposed model offers a reasonable accuracy both in the linear as well as in the saturation region of operation for submicron SiC MESFETs. It also demonstrates that (4.9) is versatile enough to simulate, without compromising on accuracy, devices having different physical dimensions (Table 4.1). Further a careful investigation of Fig. 4.2 showed that the profile of $I_{ds}(V_{ds}, V_{gs})$ characteristics differs from device to device. Fig. 4.2(a) exhibits a typical behavior of a short channel device and for such devices the observed V_T conforms well to the value evaluated from (4.8). On the other hand, all the remaining devices exhibited a non-ideal response (shift in V_T) most probably due to the presence of interface states at the Schottky barrier gate [134]. A good agreement between simulated and experimental characteristics showed that (4.9) addresses adequately the device physical parameters and thus can be used for a wider range of $I - V$ characteristics simulation involving SiC MESFETs.

TABLE 4.3: Comparison of RMS error values of simulated and observed $I-V$ characteristics for $L_g = 0.7$ μm SiC MESFET.

Sr. #	Model	$V_{gs} = 0$ V	$V_{gs} = -2$ V	$V_{gs} = -4$ V	$V_{gs} = -6$ V	$V_{gs} = -8$ V	$V_{gs} = -10$ V	Average RMSE
1.	McCamant [126]	64.0767	29.8551	10.7927	2.7182	4.3158	2.4748	19.0389
2.	Statz [157]	19.2515	8.6289	5.8586	9.8817	12.3217	7.1683	10.5184
3.	Quanjun [31]	12.6972	12.8619	11.6023	4.3739	9.4902	6.3954	9.5701
4.	Angelov [154]	11.3748	10.5521	7.3408	5.0490	4.3637	2.1253	6.8010
5.	Curtice Cubic [127]	14.4243	12.5448	9.1742	4.0533	2.6886	0.7722	7.2762
6.	TOM3 [156]	13.2623	5.9781	6.2050	5.6673	7.0449	2.8998	6.8429
7.	Manohar [153]	12.1343	9.1201	1.3711	5.4848	3.6272	2.1425	5.6466
8.	Dobes [152]	11.2693	5.4973	5.7242	4.8875	6.3989	2.3718	6.0248
9.	McNallay [128]	7.3266	4.1321	5.4288	2.2807	1.7310	0.7884	3.6146
10.	Proposed	5.7396	3.3568	3.7161	1.5081	1.7927	0.9815	2.8491

TABLE 4.4: Comparison of RMS error values of simulated and observed pulsed $I-V$ characteristics for $Lg = 0.6$ μm SiC MESFET.

Sr. #	Model	$V_{gs} = 0$ V	$V_{gs} = -3$ V	$V_{gs} = -6$ V	$V_{gs} = -9$ V	$V_{gs} = -12$ V	$V_{gs} = -15$ V	Average RMSE
1.	McCamant [126]	19.9197	12.8061	15.2194	11.4368	8.5160	6.2916	12.3649
2.	Dobes [152]	18.5558	9.4022	12.2580	9.7774	8.6395	6.1346	10.7946
3.	Manohar [153]	14.4182	14.0668	8.7749	5.6574	7.2247	3.3763	8.9197
4.	Statz [157]	11.7194	9.7149	7.1013	5.5615	9.4671	5.7238	8.2147
5.	Quanjun [31]	11.7074	9.1969	10.8905	4.9563	5.9221	4.8107	7.9140
6.	TOM3 [156]	12.2308	6.9659	7.8541	5.5355	7.5383	4.3661	7.4151
7.	McNallay [128]	14.3405	6.5084	9.9534	7.6486	4.0030	1.8211	7.3792
8.	Angelov [154]	11.0768	7.4610	9.4935	5.2868	7.7218	2.8725	7.3188
9.	Curtice Cubic [127]	12.0517	9.8707	9.1814	5.1111	2.1994	1.1570	6.5952
10.	Proposed	8.4683	6.2710	6.4509	4.2810	3.0655	1.2315	4.9614

TABLE 4.5: Performance comparison of various models used to simulate $I-V$ characteristics for $L_g = 0.5$ μm SiC MESFET.

Sr. #	Model	$V_{gs} = 0$ V	$V_{gs} = -2$ V	$V_{gs} = -4$ V	$V_{gs} = -6$ V	$V_{gs} = -8$ V	$V_{gs} = -10$ V	Average RMSE
1.	Quanjun [31]	11.0271	8.8984	10.8880	3.0078	6.6033	9.0938	8.2531
2.	McCamant [126]	12.6637	4.4472	8.6165	9.0970	3.8954	5.8057	7.4209
3.	Statz [157]	12.2399	6.7847	2.5536	3.3498	7.6273	7.3939	6.6582
4.	Dobes [152]	11.3211	4.2043	5.6500	6.7281	4.5907	5.5839	6.3463
5.	Curtice Cubic [127]	10.3334	10.1003	8.5879	5.2977	2.5341	1.0969	6.3251
6.	TOM3 [156]	11.3769	3.9043	5.4832	6.6559	4.6282	5.6040	6.2754
7.	Manohar [153]	9.6982	7.5871	3.4433	4.7577	4.2250	2.8025	5.4190
8.	McNallay [128]	6.4532	3.7352	4.7306	3.9954	3.3952	9.5265	5.3060
9.	Angelov [154]	4.1173	2.7018	4.3114	2.4930	3.0239	1.7988	3.0744
10.	Proposed	3.7750	2.9790	3.0838	2.5088	1.8359	0.9967	2.5299

TABLE 4.6: A comparative analysis of RMS error values for $L_g = 0.4$ μm SiC MESFET.

Sr. #	Model	$V_{gs} = 0$ V	$V_{gs} = -4$ V	$V_{gs} = -8$ V	$V_{gs} = -12$ V	$V_{gs} = -16$ V	Average RMSE
1.	Statz [157]	44.9791	17.9251	12.3408	24.0375	23.6267	24.5819
2.	Quanjun [31]	21.6728	23.2851	16.5332	10.7469	23.8640	19.2204
3.	McCamant [126]	28.8111	15.4188	9.2325	14.5757	12.3475	16.0771
4.	Dobes [152]	16.9427	10.6453	11.2868	10.6669	10.7732	12.0630
5.	Manohar [153]	11.7292	9.0861	7.4474	7.9619	6.3995	8.5248
6.	Curtice Cubic [127]	14.5864	11.3852	3.4714	6.4696	3.1167	7.8059
7.	McNallay [128]	11.1004	9.2427	4.9724	5.3301	2.7765	6.6844
8.	TOM3 [156]	7.7455	5.0381	4.5421	7.5330	5.0194	5.9756
9.	Angelov [154]	9.2921	9.8149	3.3570	4.7859	2.2903	5.9080
10.	Proposed	9.0400	8.2382	3.5631	4.6199	1.9076	5.4738

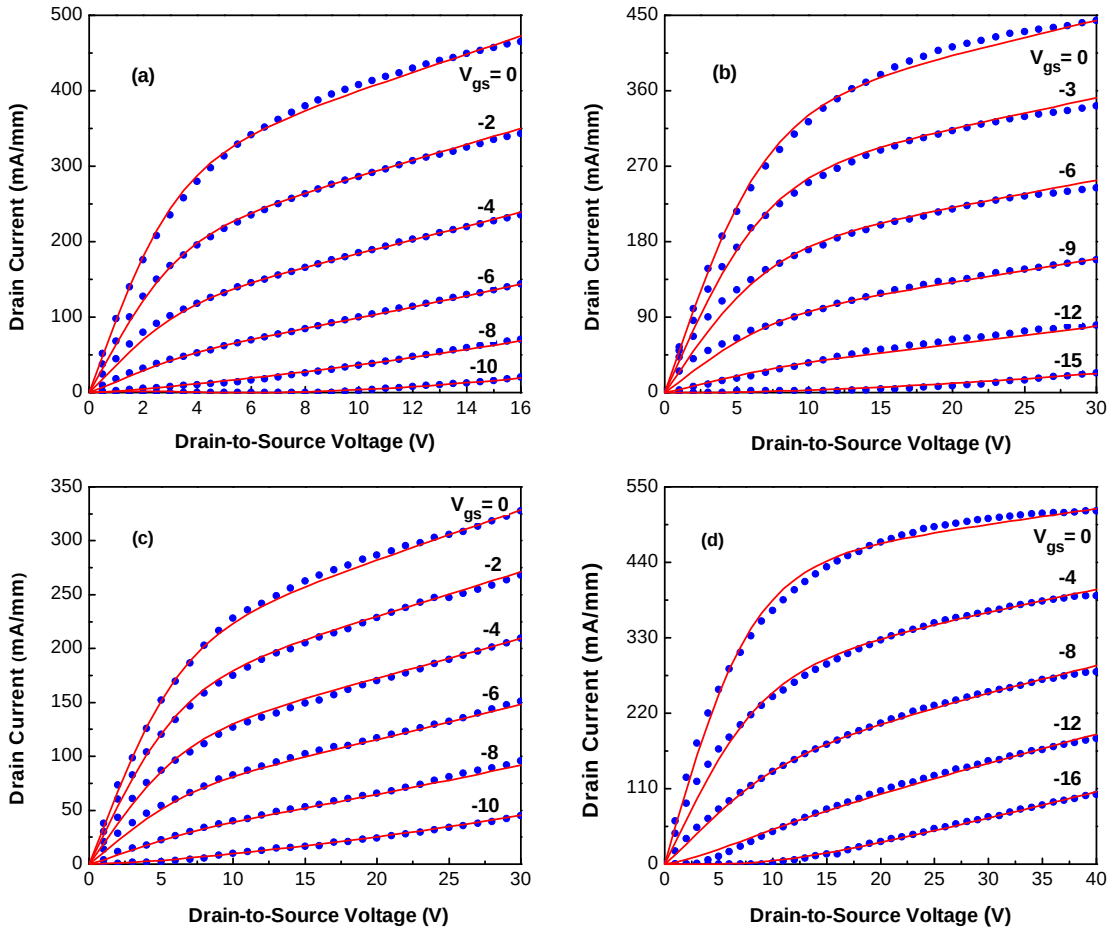


FIGURE 4.2: Experimental (•) and simulated (−) output characteristics of submicron SiC MESFETs (a) 0.7 μm gate length device, (b) 0.6 μm gate length device, (c) 0.5 μm gate length device and (d) 0.4 μm gate length device.

To compare the performance of (4.9) with other models commonly used for MESFET simulation a comprehensive comparative study was carried out. Table 3 shows RMS error values at different V_{gs} biasing evaluated using (4.22) for L_g = 0.7 μm device. The last column of the table also lists the average RMS error by which a model can be compared with its counterparts. From data of Table 4.3, it is evident that the proposed model for $L_g = 0.7$ μm device offers 21.17 % improved performance compared to the 2$^{\text{nd}}$ best observed model, i.e., McNallay model [128].

A similar comparison was also carried out for devices having $L_g = 0.6, 0.5, 0.4$ μm and the results are shown in Table 4.4, 4.5 and 4.6 respectively. Table 4.4 shows that for $L_g = 0.6$ μm device, the proposed model is 24.77 % better than the 2$^{\text{nd}}$ best observed model which in this case is the Curtice Cubic model [127]. The

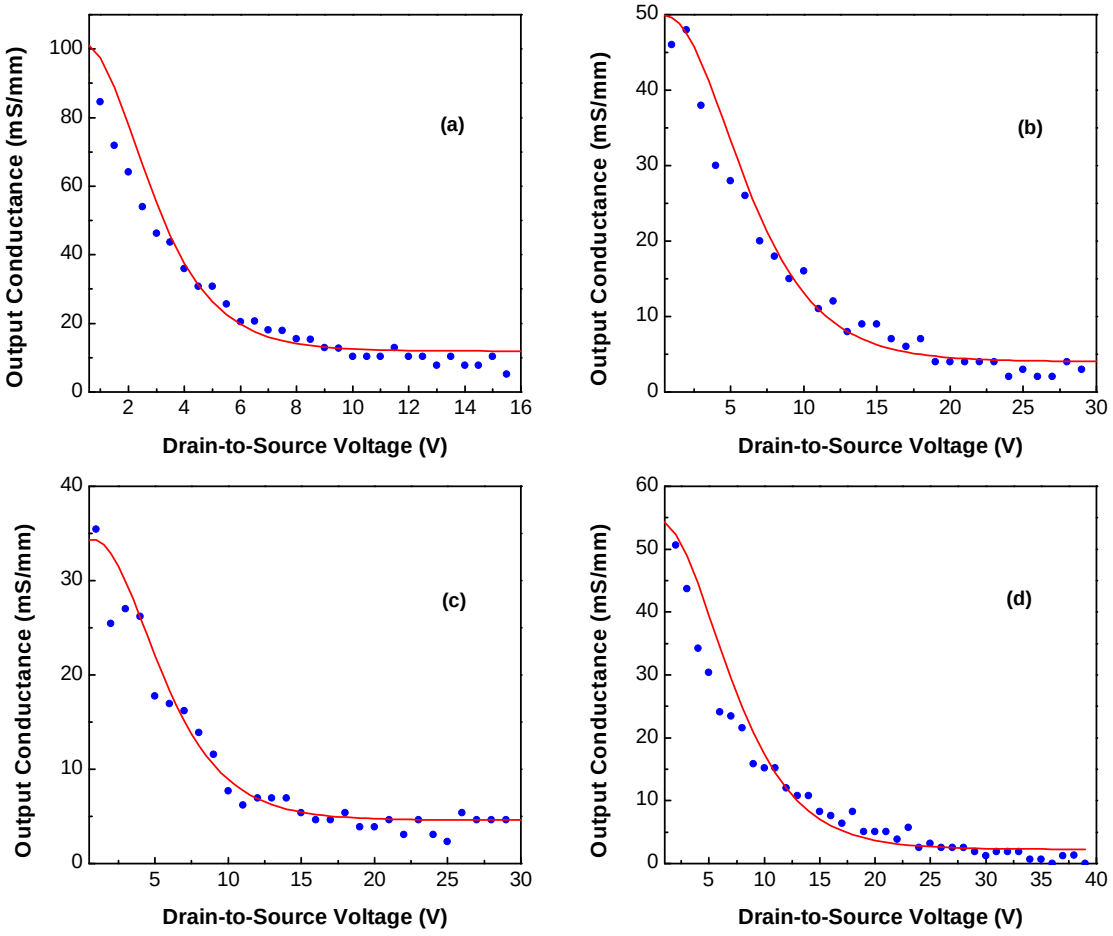


FIGURE 4.3: Experimental (•) and simulated (−) output conductance as function of gate and drain biasing of submicron SiC MESFETs (a) 0.7 μm gate length device, (b) 0.6 μm gate length device, (c) 0.5 μm gate length device and (d) 0.4 μm gate length device.

comparative analysis of Table 4.4 was for pulsed $I-V$ characteristics which were chosen in order to observe the model performance for pulsed input. The data demonstrated that the proposed model has once again out performed with good margin the other models listed in the table.

Table 4.5 shows that for $L_g = 0.5$ μm device, the proposed model offers 17.71 % improved performance compared to the next best observed model which in this case is the Angelov model [154].

Table 4.6 provides error data for $L_g = 0.4$ μm SiC MESFET. The characteristics of this device were the most difficult one to simulate because, the device at higher biasing exhibited self-regulating break down as evident from the plot. A good

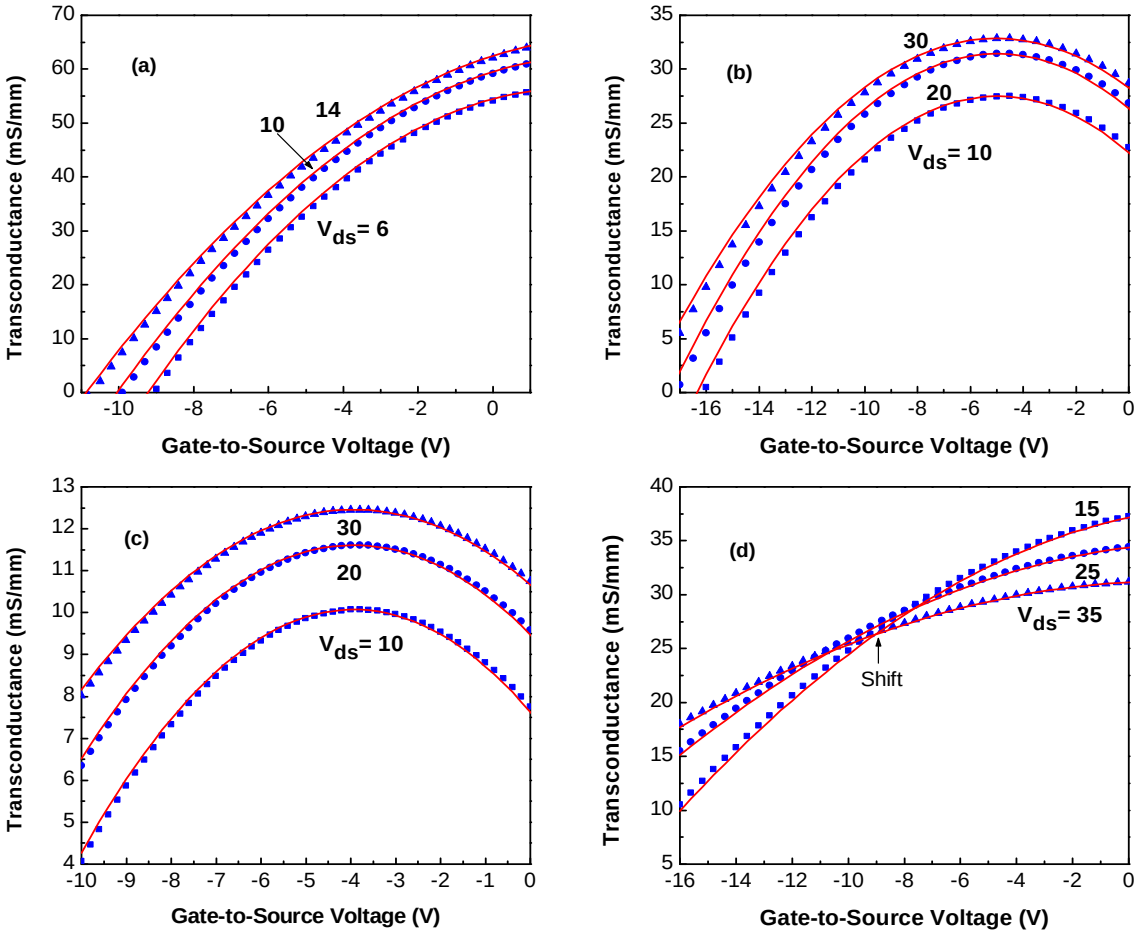


FIGURE 4.4: Experimental (•) and simulated (−) transconductance as function of gate and drain biasing of submicron SiC MESFETs (a) 0.7 μm gate length device, (b) 0.6 μm gate length device, (c) 0.5 μm gate length device and (d) 0.4 μm gate length device.

observed accuracy in simulated characteristics as seen in Fig. 4.2(d) demonstrates that the proposed model is a quite comprehensive one and takes into account 2^{nd} order effects which can influence the device behavior.

Table 4.6 data clearly shows that the error margin for this device is higher than all previously reported cases. However, the proposed model has once again shown better performance relative to other models. The next best observed model in this case was the Angelov model but, the proposed model performance in aggregate was 7.35 % better than the Angelov model.

In general, one can say that (4.9) can be employed to simulate both static as well as pulsed $I - V$ characteristics of SiC MESFETs with a high degree of accuracy,

TABLE 4.7: Fundamental values used for the evaluation of SiC MESFET parameters.

Variable	Value
Mobility, μ_0	0.095 (m/V-s)
Saturation field, E_s	2×10^7(V/m)
Relative permittivity, ϵ	8.854×10^{-11}
Saturation velocity, v_s	2.0×10^5 (m/s)
Built-in-potential, V_{bi}	1.1 eV

especially for those devices which are designed for microwave power applications. Further, (4.9) is based on fundamental square law which governs the channel characteristics of a device as a function of its geometrical parameters.

Output conductance (g_d) of the devices under discussion exhibits an exponential decay as a function of V_{ds} as evident from Fig. 4.3. The simulation which was carried out using (4.10) complies well with the experimental data. The point at which g_d saturates is the same where I_{ds} saturates for a given V_{gs}. Examination of Fig. 4.3(a) shows that g_d saturates at $V_{ds} \sim$ 7 V whereas, this is $\sim$ 17 V for the device of Fig. 4.3(d). Saturation at relatively higher V_{ds} values is primarily associated with high source resistance and the value of α in (4.10) simulates this effect. From Table 4.1, $\alpha = 0.3402$ for the device of Fig. 4.3(a) and $\alpha = 0.1277$ for the device of Fig. 4.3(d). A relatively high value of α will then mean that the device g_d will saturates quickly thus, indicating that the device offers low source resistance.

Simulation of g_m by (4.11) and its compliance to the experimental data is demonstrated in Fig. 4.4. It is a well-established fact that for a good Schottky barrier device, the transconductance peak normally occurs at $V_{gs} \sim 0$ V. However, a shift in g_m peak towards higher V_{gs} values may be witnessed in devices having submicron L_g as observed in Fig. 4.4(b) & (c). This shift is normally caused by the interface states as discussed in [135]. A good compliance of (4.11) to the experimental data once again exhibits that the proposed model is versatile enough

TABLE 4.8: Extracted parameters for submicron SiC MESFET at biasing voltage $V_{ds} = 15$ V and $V_{gs} = 0$ V, if otherwise reported.

Sr. #	Estimated Parameters	$L_g = 0.7$ μm	$L_g = 0.6$ μm	$L_g = 0.5$ μm	$L_g = 0.4$ μm
1.	Channel thickness, a	220.91 nm	219.8 nm	300.99 nm	199.96 nm
2.	Built-in-depletion	62.7 nm	63.7 nm	88.68 nm	66.12 nm
3.	Available channel, a_{eff}	30.85 nm	32.29 nm	39.00 nm	49.49 nm
4.	Saturation current, I_{dss}	76.2 mA	61.4 mA	74.88 mA	171.2 mA
5.	Depletion height, h at d_m	190.06 nm	187.2 nm	261.99 nm	150.47 nm
6.	Distance d_m	0.45 μm	0.42 μm	0.425 μm	0.23 μm
7.	Threshold Voltage, V_T (V)	-12.77	-12.019	-11.5706	-8.9699
8.	L_g/a Ratio	3.18	2.727	1.67	2.00
9.	Output conductance, g_d	2.98 mS	1.4 mS	2.33 mS	3.51 mS
10.	Maximum observed g_m	16 mS	6.05 mS	4.36 mS	12.6 mS
		at V_{gs}=0 V	at V_{gs}=-5.8 V	at V_{gs}=-4 V	at V_{gs}=-3 V

to simulate $I - V$ characteristics of the devices having different gate lengths and Schottky barrier qualities. Once a good dc simulation is achieved, ac parameters can then be assessed by using a technique given in [132].

Plot of Fig. 4.4(d) shows that $g_m(V_{gs})$ characteristics are changing its nature at certain gate and drain biasing marked in the figure. The point where the g_m slope changes its profile represents that the Schottky barrier gate is losing its control and this could be associated with the carrier generation inside the channel under intense electric filed. Probably, due to this fact the device of Fig. 4.4(d) exhibits pinch-off at much higher value ($V_T = -20$ V) compared to what has been calculated by using (4.8), i.e., $V_T = -9$ V.

By assuming the parameters listed in Table 4.7, various parameters of the devices were then assessed and given in Table 4.8. The value of a evaluated from electrical measurements by using (4.2) and (4.3) and given on serial No. 1 of Table 4.8 matches well with the wafer data as listed in Table 4.1 .

Variation in built-in depletion region as shown at the serial No. 2 of the table is due to the channel doping variation and the highest assessed value is 88.68 nm which is for the device having lowest value of N_d. Further, effective channel width, a_{eff} available for the flow of carriers is assessed from the $I-V$ data and given at serial No. 3 of the table.

$$a_{\text{eff}} = \frac{I_{dss}}{qNv_sW} \ . \tag{4.23}$$

An important factor given in Table 4.8 is the distance d_m as marked in Fig. 4.1. It is the point where it is assumed that the depletion region gets its maximum width underneath the Schottky barrier gate and thus controls the flow of current for a given biasing. The variable d_m is evaluated by using (4.2), where L_g has been replaced with d_m and the magnitude of d_m is then evaluated for a known depletion region height.

The assessed value of V_T for $L_g = 0.7$ μm device conforms to the experimental value whereas, all remaining devices exhibited higher $|V_T|$ than what has been calculated. The reported values are based on (4.8), which does not take into account the quality of Schottky barrier and the changes in the device channel under intense electric field inside the channel may cause carrier generation; flow of current from the buffer layers and gate depletion region modification resulting into wider channel crossection. These factors could potentially contribute to shift the magnitude of V_T to a higher value. The assessed value of V_T for $L_g = 0.4$ μm device is $\sim$ -9 V and by examining Fig. 4.4(d) one can clearly see that this is the point where, there is a shift in the profile of the curve indicating that the channel conditions have been changed and (4.8) might not be valid under these conditions.

It is also noted that a SiC MESFET having aspect ratio, $L_g/a \sim 3$ offers better performance compared to low aspect ratio devices given in Table 4.8.

4.5 Summary

In this chapter, an improved model has been presented to simulate DC and pulsed $I-V$ characteristics of SiC MESFETs. The validity of the model is demonstrated by applying it on submicron SiC MESFETs especially designed for power applications. A comparative analysis has been carried out by employing swarm optimization technique and it has been established that the proposed model, dependent upon the device characteristics, is $\sim\ 7-24$ % better than its counterparts. Expressions have been developed to simulate output conductance (g_d) and transconductance (g_m) of submicron SiC MESFETs which showed a good compliance to the experimental data. Based on simulated characteristics, numerous parameters defining the device geometrical structure have been estimated to a good degree of accuracy. It has been shown that the developed technique is versatile enough to predict the device characteristics even if it exhibits 2^{nd} order effects and thus the technique could be a useful tool for device simulation softwares.

Chapter 5

Assessment of Intrinsic Small Signal Parameters

5.1 Introduction

SiC MESFETs offer large breakdown field, high saturation velocity, and high thermal conductivity [13, 41]. They can operate at high biasing voltages and have high thermal robustness with large output resistance relative to other semiconductor devices, such as GaAs MESFETs [3, 53, 84]. SiC MESFETs exhibit stable thermal performance, i.e. only 10% change in their characteristics is observed when operated at 500°C [33]. They offer the highest absolute power density due to large breakdown voltage [5, 49, 90]. Therefore, SiC MESFETs are very attractive for high power microwave applications, such as transmitters for communication and RADAR.

SiC MESFETs used in RF applications have been reported in the literature. Song et al. [41] fabricated 4H-SiC MESFETs on a conducting SiC substrate and measurements showed that unity current gain frequency, f_T = 3.2GHz, maximum frequency of oscillation, f_{max} = 12.4GHz, an RF power gain of 5.9dB, and a maximum output power of 25.3dBm (0.85 W/mm) at 2GHz, which is much higher than Si and GaAs equivalent size transistors.

It is an established fact that RF performance of a MESFET depends on its gate length, L_g and saturation velocity, υ_s of its carriers. In general, with reduction in L_g, the value of f_T increases. However, when L_g is less than 1μm, the device suffers from short channel effects and performance of the device is degraded [54], which includes: reduction in transconductance, g_m; shift in threshold voltage, V_T and increase in the device output conductance, g_d [6].

Additionally, in short channel devices, vertical electric field becomes stronger to an extent that even at smaller values of V_{ds}, the mobility, μ_0 of the carriers starts to reduce. Ho-Young et al. [55], in their study of transport characteristics of short channel SiC MESFETs, reported that υ_s and μ_0 of such devices are 1.7×10^7 cm/s and 300 $\text{cm}^2(\text{Vs})^{-1}$ respectively, which are smaller than those of earlier reported values.

Another important short channel effect is the drain induced barrier lowering (DIBL), causing less gate control on the channel current, I_{ds} thus, increasing g_d and decreasing g_m of the device. Further, at high V_{ds}, the flow of carriers can also divert towards the substrate resulting in large substrate current. Honda [6] and Manabu [2] in their investigation of short channel effects, demonstrated that when L_g is less than 1 μm, gate loses its effective control over I_{ds} due to DIBL. They also reported that f_T, power density, and g_m start to saturate at $L_g \sim 0.3\mu$m. f_T of a SiC MESFET is given by [85, 130]

$$f_T \approx \left[\frac{g_m}{2\pi(C_{gs}+C_{gd})}\right] , \tag{5.1}$$

where, C_{gs} is gate-to-source capacitance and C_{gd}, is gate-to-drain capacitance defined as [130]

$$C_{gs} \approx \left[\frac{\varepsilon_s W L_g}{h_0}\right]\left[1+\frac{X}{2L_g}-\frac{2h_0}{L_g+2X}\right] . \tag{5.2}$$

$$C_{gd} \approx \left[\frac{2\varepsilon_s W}{1+2X/L_g}\right] . \tag{5.3}$$

X represents extension of gate depletion layer towards the drain-side of the gate and is given by [130]

$$X \approx \sqrt{\left[\frac{2\varepsilon_s}{qN_d(-V_{gs}+V_{bi})}\right]}(V_{ds}-V_{gs}+V_{bi}) \ , \tag{5.4}$$

and h_0 of Eq. 5.2 is given by

$$h_0 = \sqrt{\frac{2\varepsilon_s(-V_{gs}+V_{bi})}{qN_d}} \ . \tag{5.5}$$

In above expressions, ε_s represents permittivity of SiC material, V_{gs} is gate-to-source biasing, V_{bi} is the built-in potential, W represents width of the device, q is the electronic charge and N_d channel doping density. Theoretical value of g_m, after considering the reduction in υ_s, because of the transverse electric field, is defined as [130]

$$g_m = \frac{\varepsilon_s \upsilon_s W}{3h_0} \ . \tag{5.6}$$

Transconductance delay, τ is given by

$$\tau \approx \frac{1}{\upsilon_s}\left[\frac{X}{2} - \frac{2h_0}{1+2X/L_g}\right] \ . \tag{5.7}$$

Channel resistance, R_i after the onset of current saturation is defined as

$$R_i = \left[\frac{\upsilon_s L_g}{\mu I_{ch}}\right] \ , \tag{5.8}$$

where I_{ch} is given by

$$I_{ch} = qN_d\upsilon_s[a-h(x)]W \ , \tag{5.9}$$

where a represents epi-layer thickness and $h(x)$ is given by

$$h(x) = \sqrt{\frac{2\varepsilon_s(V_{ds}-V_{gs}+V_{bi})}{qN_d}} \ . \tag{5.10}$$

Since there is non uniformity in $h(x)$ underneath the Schottky barrier gate caused by the applied voltage V_{ds}, which generates C_{ds} capacitor thus, by assuming that

the depletion layer involved in the definition of C_{ds} is $h(x)/2$ and also because of submicron geometry, the shape of depletion tends to become circular. And it can safely be assumed that one quarter of a circle under L_g is involved in defining C_{ds} thus, [39, 132]

$$C_{ds} \approx \left[\frac{W\varepsilon_s h(x)/2}{L_g/4}\right] . \tag{5.11}$$

And output conductance, g_d can be approximated as [130]

$$g_d \approx \frac{I_{ch}}{4V_{ds}} . \tag{5.12}$$

Eqns. 5.2 to 5.12 represent intrinsic small signal elements, here onward referred to as conventional technique to assess intrinsic small signal parameters of a SiC MESFET [130]. These parameters are, primarily, responsible for determining high frequency and high power characteristics of the device. As evident from Eqns. 5.2 to 5.12, intrinsic small signal parameters are material, biasing and device design dependent. Effects of source and drain parasitic resistances, R_S and R_D can be incorporated by using

$$R_S = \frac{L_{sg}}{qN\mu aW} + R_C \quad \text{and} \quad R_D = \frac{L_{dg}}{qN\mu aW} + R_C , \tag{5.13}$$

where L_{sg} and L_{dg} are the source-to-gate and gate-to-source separations, and R_C is ohmic contact resistance, typically 2Ω for microwave devices. Thus, effective V_{dse} is evaluated using either $V_{dse} = V_{ds} - I_{ch}(R_S + R_D)$, or $V_{dse} = V_{ds} - I_{ch}(R_S)$, whichever is applicable.

It is an established fact that SiC MESFETs are meant for high biasing and high temperature related applications where conventional approach to assess intrinsic small signal parameters may not be fully valid. At high biasing, there are considerable self-heating effects inside the device, which make the carriers hot and their scattering probability into the buffer and Schottky barrier layers increase. Expressions involved in the conventional technique are, primarily, dependent on gate depletion layer thus, any modification in depletion layer thickness because of high temperature/biasing is bound to generate errors in the assessed values of

these parameters.

In this chapter, a technique has been developed to assess the intrinsic small signal parameters of submicron SiC MESFETs by involving experimental $I-V$ characteristics. The developed technique takes into account possible depletion layer modification due to high temperature/biasing and is capable of predicting AC small signal parameters to an acceptable accuracy. The remaining part of the paper consists of development of a proposed technique for the assessment of small signal parameters for submicron SiC MESFETs. Followed by its comparison with experimental data and also with the conventional approach. The dependence of small signal parameters on the device biasing has been discussed at the end, using a MATLAB based simulation process.

5.2 Model Development

A crossectional view of a SiC MESFET is shown in Fig. 5.1. It has n-channel doping of $2.7\times10^{17}\text{cm}^{-3}$ grown on a buffer layer having a p-doping of $5\times10^{15}\text{cm}^{-3}$ as shown in Table 5.1. It is an interdigitated device having total gate periphery of $2\times200\mu$m [13]. Device to device isolation is achieved by mesa etching whereas, drain-source leakage is controlled by a fully depleted buffer grown on a semi-insulating substrate.

Fundamental difference in the proposed and the conventional technique is that I_{ch} of the conventional approach is changed with I_{ds}, which is evaluated using expression [39]

$$\begin{aligned} I_{ds} =& I_{dss}\left(1-\frac{\delta V_{gs}}{V_T+\Delta V_T+\gamma V_{ds}}\right)^2 \\ &\times\left(1+\lambda V_{ds}+\frac{\delta V_{gs}}{V_{ds(sat)}}\right)\tanh(\alpha V_{ds})\ , \end{aligned} \tag{5.14}$$

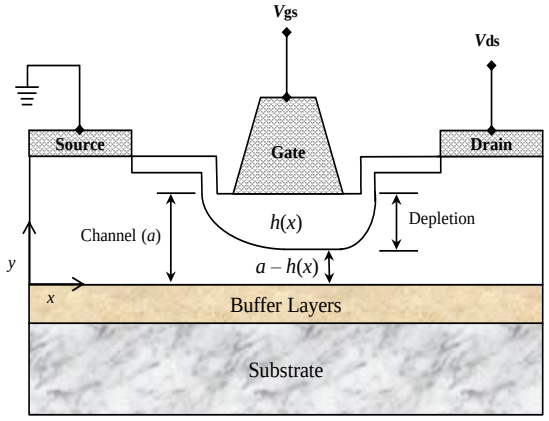


FIGURE 5.1: Crossectional view of a SiC MESFET.

where δ represents non-ideality in Schottky barrier of a SiC MESFET, ΔV_T corresponds to shift in V_T because of submicron geometry, γ simulates V_T dependence on V_{ds}, λ takes care of finite output conductance in the saturation region of operation, α defines the slope of the linear region, I_{dss} represents drain-to-source current at $V_{gs} = 0$V and saturation knee voltage is represented by $V_{ds(sat)}$. The output impedance of the MESFET has been taken care of by the term λV_{ds}. A relatively high value of λ would mean that the device has high output conductance as a function of V_{ds}, resultantly its output impedance will be relatively low. Differentiating Eq. 5.14 with respect to V_{gs} and V_{ds}, one will have

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds-const}} . \tag{5.15}$$

Also

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs-const}} . \tag{5.16}$$

Reason for changing I_{ch} with I_{ds} is that in short channel devices, especially at elevated temperatures and biasing, there could be a possible modification in the Schottky barrier depletion layer due to increased occupancy of high energy states by the energetic carriers. Such a modified depletion layer can be assessed to a reasonable accuracy by knowing I_{ds} having dependance on available channel crossection, i.e. $a - h(x)$ as shown in Fig. 5.1. Following this concept, expressions

based on $h(x)$ can be modified, such as gate-to-source capacitance, C_{gsm} can be redefined as [132]

$$C_{gsm} \approx (\varepsilon_s W L_g)\left[a - \frac{I_{ds}}{qN_d \upsilon_s W}\right]^{-1} . \tag{5.17}$$

While developing Eq. 5.17, it has been assumed that because of submicron geometry, carriers are attaining saturation velocity in a close vicinity of the source side of the gate electrode hence, saturation current has been used in Eq. 5.17. Extending the logic of parallel plate capacitor gate-to-drain capacitance, C_{gdm} follows an expression of the form defined by Eq. 5.18 [130]

$$C_{gdm} = \frac{\varepsilon_s W}{\left(1 + \frac{2X}{L_g}\right)} . \tag{5.18}$$

But in submicron devices, depletion underneath the Schottky barrier becomes circular and its extension in such cases towards the drain side can be assumed as identical in all directions thus, $X \approx h(x)$. Therefore, Eq. 5.18 can be written as

$$C_{gdm} = \frac{\varepsilon_s W}{\left(1 + \frac{2h(x)}{L_g}\right)} . \tag{5.19}$$

From Eq. 5.9

$$h(x) = \left[a - \frac{I_{ds}}{qN_d \upsilon_s W}\right] . \tag{5.20}$$

By combining Eq. 5.19 and 5.20 and rearranging, we get

$$C_{gdm} \approx \left[\frac{\varepsilon_s W}{1 + (2/L_g)\left[a - \left(I_{ds}/qN_d \upsilon_s W\right)\right]}\right] . \tag{5.21}$$

Drain-to-source capacitance, C_{dsm} of a SiC MESFET is defined by the non-uniform depletion layer distribution underneath the Schottky barrier gate of the device. Thus, separation between the two layers of charges defining C_{dsm} capacitor will be determined by length L_g of the device. Considering quarter circle approximation

because of the submission geometry [39], the capacitor C_{dsm} can be expressed as

$$C_{dsm} \approx \left[\frac{2W\varepsilon_s \left\{ a - \left(I_{ds}/qN_d\upsilon_s W \right) \right\}}{L_g/4} \right] . \tag{5.22}$$

Using Eqns. 5.21 and 5.22, modified unity gain frequency, f_T is defined as

$$f_{T1} \approx \left[\frac{g_{mm}}{2\pi(C_{gsm} + C_{gdm})} \right] , \tag{5.23}$$

where g_{mm} is given by

$$g_{mm} = (g_{m0})e^{-j\omega\tau_m} \tag{5.24}$$

such that g_{m0} can be attained by differentiating Eq. 5.14 with respect to V_{gs}, keeping V_{ds} constant [129]. Transconductance delay, τ_m is defined as

$$\tau_m \approx \left[\frac{C_{gsm} + C_{gd1}}{2g_{mm}} \right] . \tag{5.25}$$

In Eq. 5.25, a factor of two is used to adjust the depletion modification caused by high electric field. Since the device under discussion, by using its physical parameters given in Table 5.1, should pinch-off at V_{gs} = -5.6V by considering both V_T and $\triangle V_T$ [134]. Since the observed pinch-off, as evident from Fig. 5.2, is much higher than the calculated value because of self-heating effects, a factor of 2 is used to accommodate low g_m, which is a direct consequence of high V_T.

Channel resistance, R_{im} is given by Eq. 5.26

$$R_{im} = \left[\frac{\upsilon_s L_g}{\mu I_{ds}} \right] . \tag{5.26}$$

Since in a distributed network where a current path is modelled by a combination of multiple series resistors and parallel capacitors as offered by the MESFET channel with respect to its gate metal, the magnitude of the current decreases progressively while travelling through the channel hence, offering a non-uniform

resistance. Therefore, an AC resistance, in principle, would be less than its DC counterpart [130], which for a submicron device can be assumed as one half of the DC resistance, thus, output conductance, g_{dm} can be approximated as,

$$g_{dm} \approx \frac{1}{2}\frac{\partial I_{ds}}{\partial V_{ds}}\bigg|_{V_{gs(cont)}}, \tag{5.27}$$

where I_{ds} is given by Eq. 5.14. In summary, Eqs. 5.14 to 5.27 define a proposed set of expressions to estimate intrinsic small signal elements of microwave SiC MESFETs.

5.3 Measured and Simulated DC Characteristics

To check the validity of the proposed model and to compare it with experimental data, a MATLAB code has been developed involving swarm optimization technique wherein, Eq. 5.14 has been implemented [39]. A submicron SiC MESFET is chosen [13] whose details are given in Table 5.1. Wherein, buffer layer thickness is represented by, b and its doping density with variable, N_b. It is worth mentioning that buffer layer depletion, x_P, evaluated using Eq. 5.28, has the thickness of 0.48μm, which shows that entire buffer layer is depleted under built-in conditions [159].

$$x_P = \left[\left(\frac{2\epsilon_s V_{bi}}{q}\right)\left(\frac{N_d}{N_b}\right)\left(\frac{1}{N_d + N_b}\right)\right]^{1/2}. \tag{5.28}$$

Optimization was carried out using an objective function whose details are given elsewhere [39]. Optimized variables of Eq. 5.14 are listed in Table 5.2. RMS errors for experimental and simulated $I-V$ characteristics, as a function of biasing voltages, are given in Table 5.3. Whereas, observed and simulated $I-V$ characteristics are shown in Fig. 5.2.

Table 5.3 shows that average RMS error for the $I-V$ characteristics of Fig. 5.2 is 2.3341×10^{-3}. Such a small magnitude of error demonstrates the validity

TABLE 5.1: Shows physical parameters of a submicron SiC MESFET whose experimental $I-V$ characteristics given in Ref. [13] were used to validate the proposed model.

Variables	Values
$L_g(\mu\text{m})$	0.4
$W(\mu\text{m})$	4×100
$a(\mu\text{m})$	0.20
$N_d(\text{cm}^{-3})$	2.7×10^{17}
$b(\mu\text{m})$	0.34
$N_b(\text{cm}^{-3})$	5×10^{15}
$x_P(\mu\text{m})$	0.48
$x_n(\mu\text{m})$	0.06

TABLE 5.2: Shows values of different parameters of Eq. 5.14 for the device of Table 5.1, attained after optimization process to model $I-V$ characteristics of Figure 5.2.

Variables	Values
$\alpha(1/\text{V})$	0.1274
$\lambda(1/\text{V})$	0.0052
$I_{dss}(\text{mA})$	171.40
$V_T(\text{V})$	-20.00
γ	0.0631
Δ	-0.1926
δ	-0.2140
ξ	0.0342

TABLE 5.3: RMS error values of a 0.4μm SiC MESFET for the characteristics shown in Figure 5.2.

V_{gs}	-16V	-12V	-8V	-4V	0V	Average
RMSx10^{-3}	1.4389	2.2007	1.3606	3.1456	3.5249	2.3341

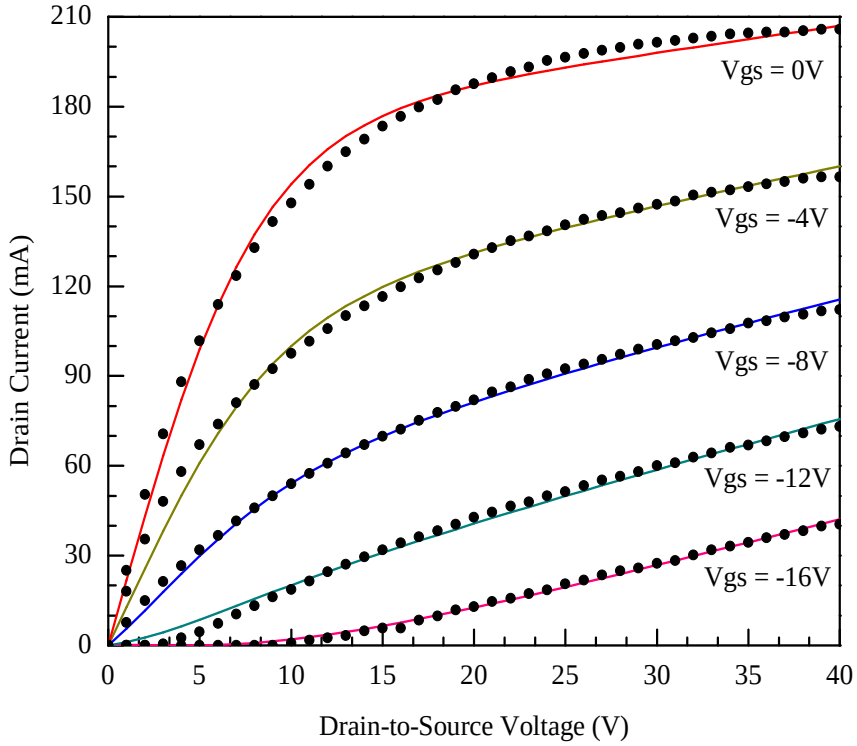


FIGURE 5.2: Simulated (−) using Eq. 5.14 and experimental (•) output characteristics of a 0.4μm SiC MESFET.

of Eq. 5.14. It can be seen from Fig. 5.2 that the device under discussion offers high resistance in its linear region of operation. This could be associated with relatively high values of R_S and R_D caused by the combination of contact resistance, R_C and bulk hesitance, R_B. Since R_B is a doping dependent variable and for a given doping, a relatively high value of R_S and R_D can then be associated with a high value of R_C, which is fabrication dependent and may vary from process to process. Since the chosen device has $L_g = 0.4\mu$m, it was therefore, obvious that this device will have short channel effects and the same are visible from the output characteristics shown in Fig. 5.2 wherein, the device is presenting a considerable high value of g_d and also the performance of Schottky barrier gate is deteriorating with increasing values of V_{ds} and V_{gs} [135, 144]. Such devices do not comply to standard square law expressions for their output characteristics, in the saturation region of operation, and therefore, a non-linear expression of the form shown by Eq. 5.14 is required to simulate $I - V$ characteristics of such devices.

By differentiating Eq. 5.14 with respect to V_{gs}, one gets g_m of the device as shown

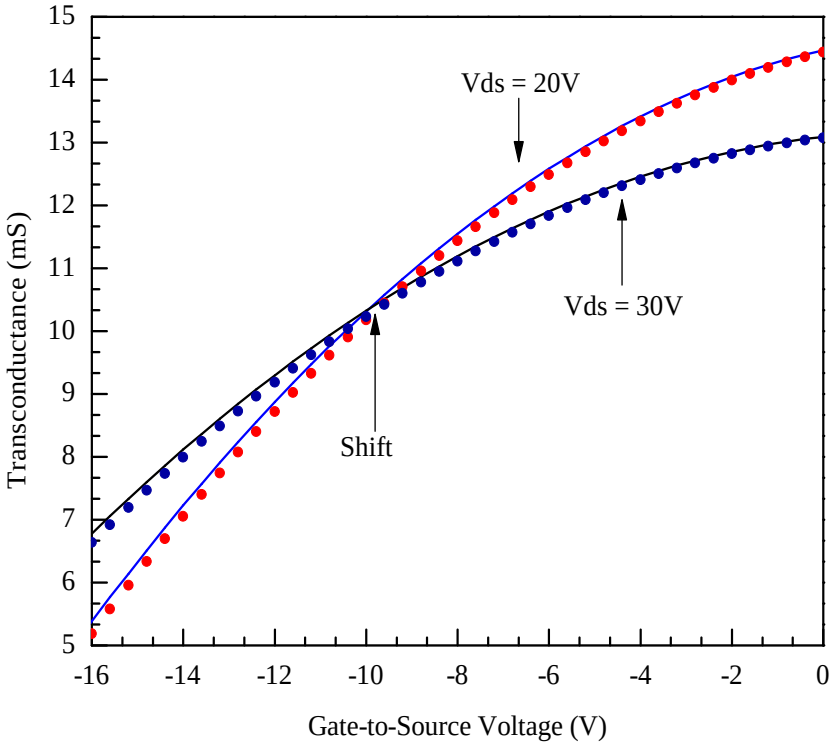


FIGURE 5.3: Transconductance of a submicron SiC MESFET. (−) represents a plot achieved using Eq. 5.15 and (•) represent differentiation of observed $I-V$ characteristics with repect to V_{gs}. Point 'shift' represents biasing voltage where the Schottky barrier gate starts performing relatively poor compared to lower biasing voltages.

by Eq. 5.15. The g_m of the device under discussion has been plotted in Fig. 5.3 where the symbols represent differentiation of experimental data of the $I-V$ characteristics of Fig. 5.2 and solid lines are plotted using Eq. 5.15. The plot of Fig. 5.3 clearly shows that at $V_{ds} = 30$V and at $V_{gs} \approx -10$V, Schottky barrier gate starts losing its grip on the channel, probably due to the self-heating effects and as a result, the slope of the curve changes at that biasing. This increases effective crossectional area available for the flow of current, i.e. $a-h(x)$, which results into an increase in g_d and decrease in g_m. The term $a-h(x)$ defines available channel crossection as shown in Fig. 5.2, and a decrease in $h(x)$ due to increased carriers scattering into the depletion region under intense electric field will reduce the the depletion height $h(x)$, which will eventually increase $a-h(x)$. So, the assessment of small signal parameters, under such conditions, using the conventional technique would be really hard. This requires a modification in the conventional approach to predict AC small signal parameters of a submicron SiC MESFET.

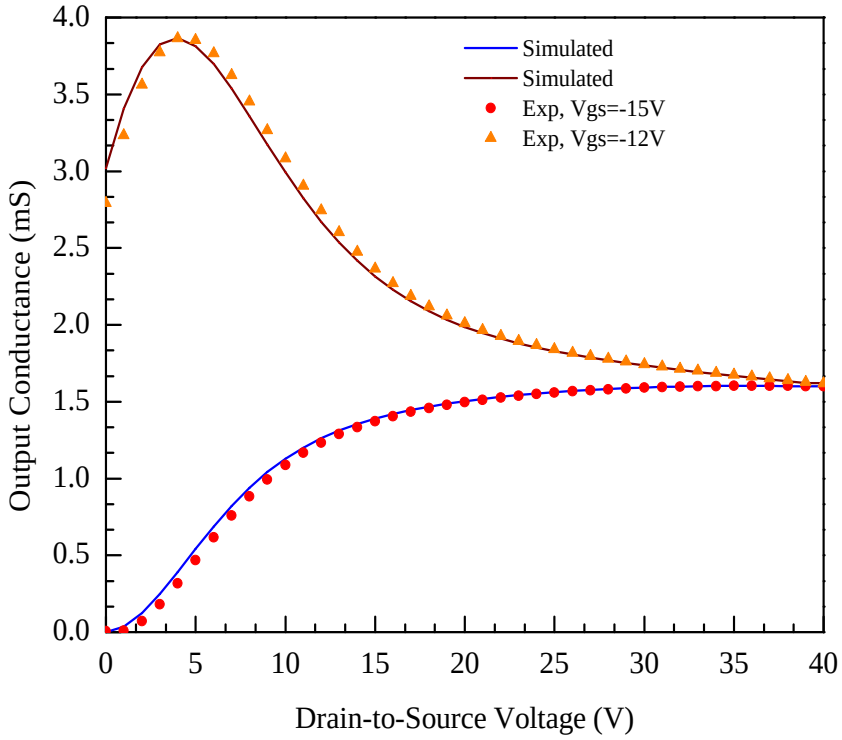


FIGURE 5.4: Output conductance of a submicron SiC MESFET. Plot exhibits that the output conductance which was concave upwards changed to concave downwards with changing gate biasing.

Figure 5.4 demonstrates changing behavior of g_d of a SiC MESFET with changing values of V_{gs} and V_{ds}. Solid lines are plotted using definition given in Eq. 5.16 whereas, symbols are achieved by differentiating the experimental $I-V$ characteristics with respect to V_{ds}. This figure clearly illustrates that the device, which was presenting negative profile for its g_d started showing positive profile for the same variable, when biasing conditions were further enhanced. For $V_{gs} = -12V$ curve of Fig. 5.4, the initial rise in g_d is due to the linear increase in the velocity of carriers under increasing values of V_{ds}. And when the velocity of carriers reaches υ_s, at this point of time any further increase will not be translated into an increase in I_{ds} thus, g_d starts decreasing and reaches to its saturation value at $V_{ds} = V_{ds(sat)}$. On the other hand, for $V_{gs} = -15V$ curve of Fig. 5.4, the carriers under high electric field become so hot that their scattering both into the depletion and buffer are the dominating factors in defining the device characteristics as a result, the magnitude of $g_d(V_{ds})$ though small but increasing; showing the broadening of the channel for a given V_{gs}. The magnitude of g_d then saturates for a biasing sufficient to attain

v_s. These results clearly demonstrate that at increased biasing, there is change in gate depletion layer and any element (e.g. C_{gs}, C_{gd}, etc.) associated with the gate depletion layer can only be assessed, with reasonable accuracy, if depletion layer modification has been taken into account [132].

5.4 Assessment of Intrinsic AC Parameters

Basic philosophy for assessing small signal parameters of a SiC MESFET is based on accurate DC modeling of the device as described in Section 5.2. Using swarm optimization technique, $I-V$ characteristics of a submicron device have been simulated. Once $I-V$ characteristics of an acceptable accuracy are achieved, the optimized variables, as shown in Table 5.2, are then used to simulate I_{ds} and then AC small signal parameters. In small signal parameter assessment, it is obvious from Eqs. 5.17 to 5.26 that variable $h(x)$ has been eliminated and it has been substituted with an I_{ds} based expression. Thus, any change in channel condition, if it is going to modify Schottky barrier depletion, will be directly translated into the available channel height, $a-h(x)$, which determines I_{ds}. Thus, the developed approach will incorporate carriers scattering into Schottky barrier depletion under self heating or intense transverse electric field.

Figure 5.5 represents variation in C_{gs} as a function of V_{ds} for chosen values of V_{gs}. An apparent view of the figure revealed that variation in capacitance profiles by varying V_{ds} are almost identical for both the models, except the initial points. At $V_{gs}=0$V, conventional model predicts a value of $\sim$ 50fF; whereas, the proposed model gives the value for the same variable about 3 times higher, i.e. $\sim$ 140fF. This clearly shows that in conventional approach, the Schottky barrier depletion layer is much thicker than the proposed approach; whereas, in reality, due to the intense channel conditions, Schottky barrier layer is thinner than its ideal value, which results in a much higher value of C_{gs}. In saturation region of operation ($V_{ds}=40$V and $V_{gs}=0$V), conventional model gives $C_{gs}=202$fF whereas, the value evaluated from the proposed technique is $C_{gsm}=165.6$fF. Experimental

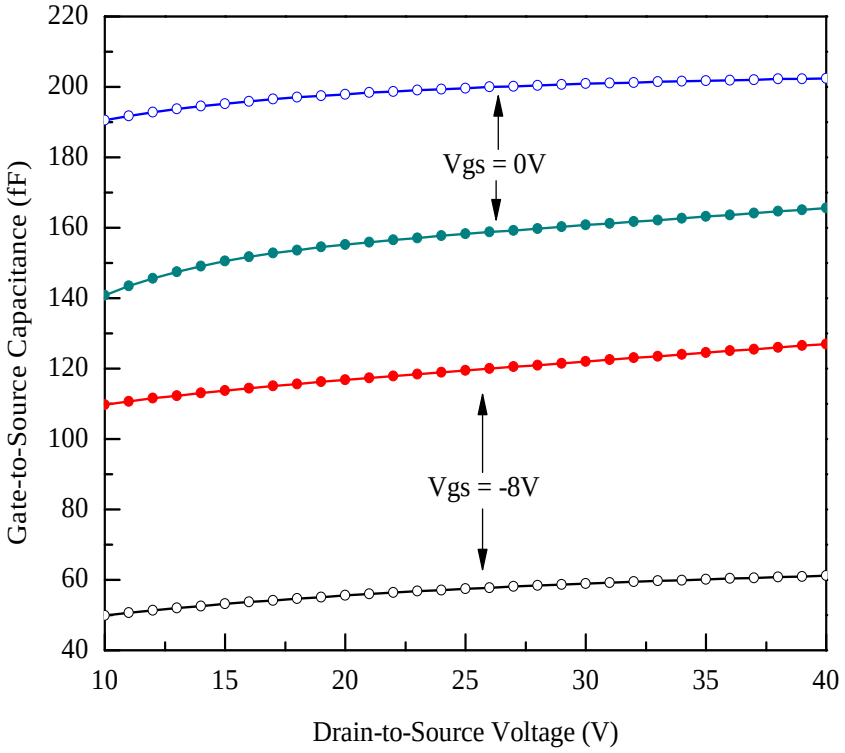


FIGURE 5.5: Gate-to-source capacitance, $C_{gs}(V_{ds}, V_{gs})$ of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of C_{gs} attained from the conventional approach whereas, solid circles ($\bullet$) show calculated C_{gs} from the proposed model.

value attained from AC measurement gave C_{gs} = 164fF [21]. A reasonably close match between the experimental value and the one calculated using the proposed technique confirms the validity of Eq. 5.17.

Figure 5.6 shows the behavior of C_{gd} capacitance as a function of applied biasing. An obvious contrast in the behavior of the conventional and the proposed models is observed. It is evident from the figure that with increasing magnitude of V_{ds}, the conventional model shows a parabolic decline in the values of C_{gd}; whereas, the proposed model representing Eq. 5.21 exhibits a slight upward trend with increasing values of V_{ds}.

Eq. 5.3, which represents the conventional model has X, a bias dependent variable, sitting in the denominator of the equation. With increasing drain biasing, the value of X also increases resulting into a decrease in the value of C_{gd}. But, this is an ideal scenario, usually observed in FET devices at low power and also at low biasing. Devices in which self heating and high electric field are the predominant

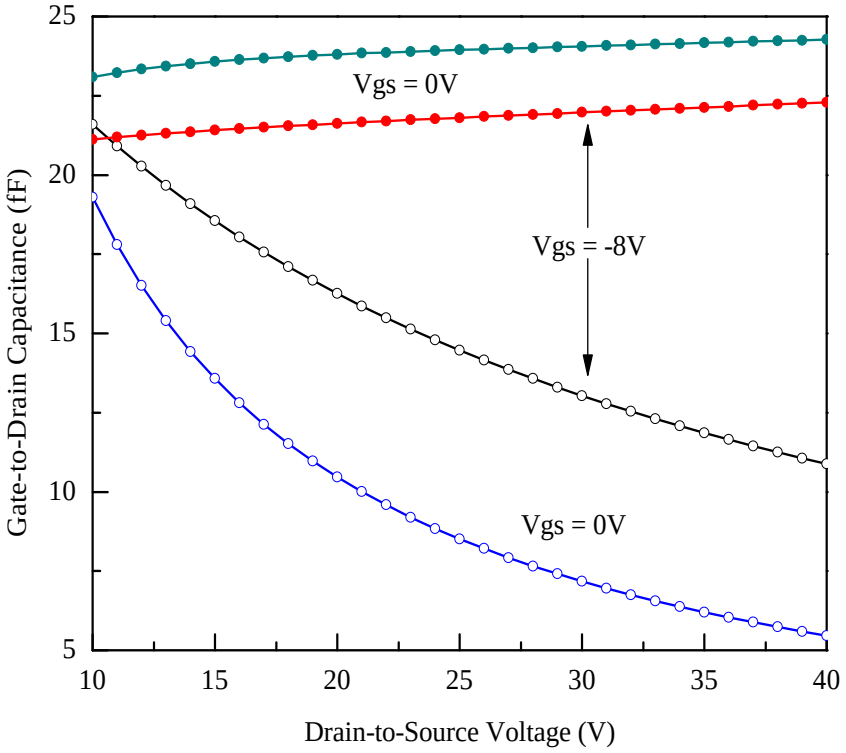


FIGURE 5.6: Gate-to-drain capacitance, $C_{gd}(V_{ds}, V_{gs})$ of a 0.4μm SiC MESFET. Open circles (○) represent values of C_{gd} attained from the conventional approach whereas, solid circles (●) show calculated C_{gd} from the proposed model.

phenomena, such a response is bound to fail because of Schottky barrier depletion layer modification. Extension in gate depletion layer caused by the increasing values of V_{ds} and its reduction due to self heating and vertical electric field are almost balancing each other. Rather, there is a slight reduction in the gate depletion layer, which is responsible for increase in C_{gd} with increasing V_{ds}, as evident from Fig. 5.6. These arguments are also supported by the experiment because, experimentally observed value of C_{gd} at $V_{ds} = 40$V and $V_{gs} = 0$V is 24.1fF [21], and the one calculated by using the proposed model is 24.27fF. On the other hand, the value of C_{gd} attained by using the conventional technique is 5.46fF, much lower than the actual one.

Figure 5.7 shows simulated results of C_{ds} as a function of V_{ds} with V_{gs} as a variable. The plot exhibits that by changing V_{gs}, there is a change (increase) in the magnitude of C_{ds} which is an understandable response, because increase in the magnitude of C_{gs} increases the depletion layer thickness, which results into an

increase in the crossectionl area of $h(x)$, a variable responsible to define C_{ds}. It is obvious from Fig. 5.7 that V_{gs} dependent response for both the cases, the conventional and the proposed, follow the same behavior that is, by increasing the magnitude of V_{gs}, the value of C_{ds} increases. But, C_{ds} variation with respect to V_{ds} exhibits opposite nature for the conventional and the proposed model as is evident from Fig. 5.7. The proposed model shows a decline in C_{ds} with increasing values of V_{ds}, while the conventional technique shows an upward trend for the same parameter. The response of the conventional model is understandable for the devices, which function at low biasing or at low temperature, where self heating is not a big consideration. In the proposed approach, the value of C_{ds} is decreasing with increasing values of V_{ds}, presumably due to the modification of gate depletion layer under intense channel conditions caused by high vertical electrical field or/and self heating effects, which have not been considered as variables in the convectional approach. These have been accommodated in the proposed approach by replacing $h(x)$ with an appropriate expression involving I_{ds}, which has a good accuracy, due to an optimized simulation process discussed hitherto.

Behavior of transit time, τ as a function of V_{ds} is shown in Fig. 5.8. The figure shows that the magnitude of τ is increasing almost linearly by increasing V_{ds}. However, the slope of the conventional and the the proposed model is different. Further, at $V_{gs} = 0$V, there is a significant difference in the starting value of τ. Primarily, τ represents time required by the depletion to readjust itself with changing values of potential at gate electrode. Therefore, to accommodate the entire gate depletion layer, both C_{gs} and C_{gd} are included in the definition of τ as given by Eq. 5.25. Since g_m is significantly lower because of the intense vertical electric field, therefore, to accommodate that a scaling factor of 2 has been used in Eq. 5.25. At $V_{gs} = 0$V and $V_{ds} = 40$V, the observed value is $\tau \approx 8.55$ps whereas, the evaluated value is $\tau \approx 7.98$ps. A reasonably good estimation of τ confirms the validity of Eq. 5.25. On the other hand, the value of τ attained from the conventional model, for the same biasing, is 5.25ps. Comparison of the data clearly shows that Eq. 5.25 provides a better assessment compared to that of Eq. 5.7. This is so because, Eq. 5.7 is based on υ_s whose value deteriorates due to intense

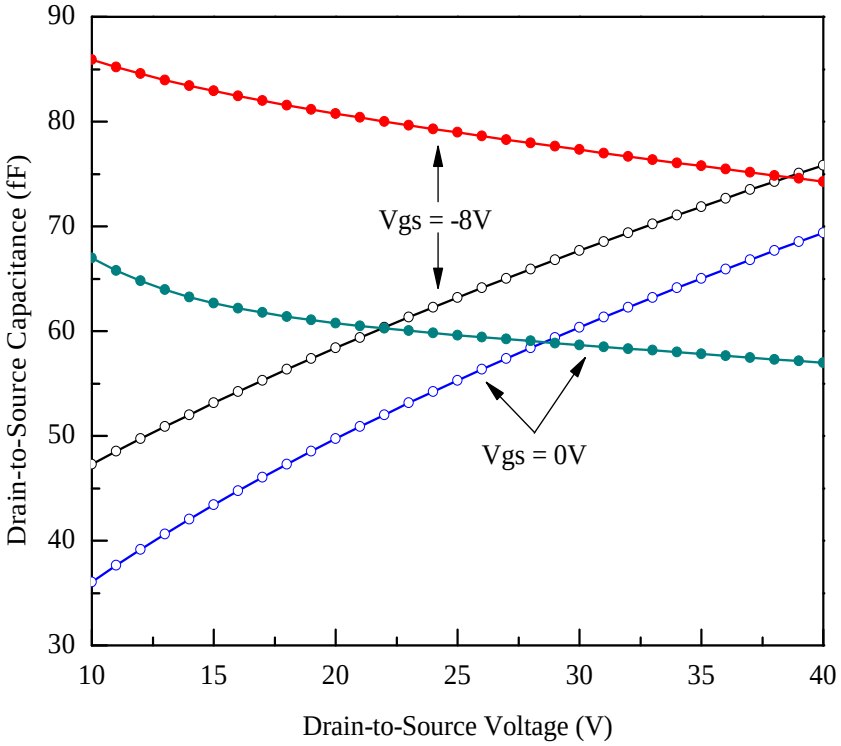


FIGURE 5.7: Drain-to-source capacitance, $C_{ds}(V_{ds}, V_{gs})$ of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of C_{ds} attained from the conventional approach whereas, solid circles ($\bullet$) show calculated C_{ds} from the proposed model.

vertical electric field, which has not been taken into account while developing this expression. Thus, a significant discrepancy is noticed in the observed and the evaluated values of τ using the conventional approach.

Figure 5.9 represents g_m of a submicron SiC MESFET. The plot is achieved using Eqns. 5.6 and 5.24. The conventional model exhibited much higher values of g_m compared to the proposed model. A basic reason, which could be associated with high values of g_m attained from the conventional model is, non consideration of self heating effects or/and high transverse electric field [162]. Both of these variables reduce the effectiveness of Schottky barrier gate action, which defines g_m. On the other hand, involving I_{ds} in g_m definition, as given by Eq. 5.24, implies that channel conditions, which eventually control the device g_m, are taken into consideration. Therefore, the proposed model response is more representative to that of the actual device response and the same is supported by the fact that at $V_{ds} = 40$V and $V_{gs} = 0$V, the observed response is 11.1mS whereas, the evaluated

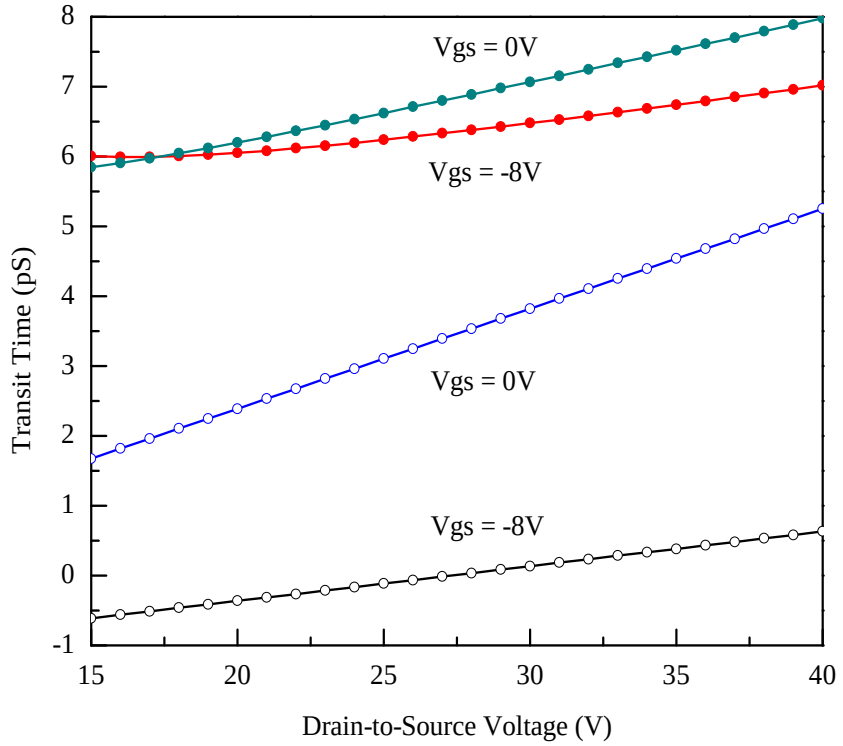


FIGURE 5.8: Transit time, τ of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of τ attained from the conventional approach whereas, solid circles ($\bullet$) show simulated values of τ using the proposed model.

response using the proposed and the conventional models are 11.9mS and 36.30mS, respectively. This clearly shows that the accuracy of the proposed model is much higher than the conventional model in predicting g_m of a submicron SiC MESFET.

Channel resistance, R_i and its variation as a function of V_{gs} and V_{ds} is shown in Fig. 5.10. Values of R_i given by the conventional model are negative indicating breakdown of Eq. 5.8. However, $R_i(V_{ds}, V_{gs})$ variation offered by the proposed model presents a quite convincing profile. The observed difference between two models can easily be figured out by comparing Eq. 5.8 and Eq. 5.26. In Eq. 5.8, I_{ch} is used in evaluating R_i while in the subsequent case, I_{ds} has been employed. Since I_{ch} is determined by $a - h(x)$ and $h(x)$, in the given situation, gives an over estimation as explained before therefore, the predicted values of R_i, are negative, which could not be possible. These results clearly demonstrate limitations pertaining to the conventional model applicability on SiC MESFETs.

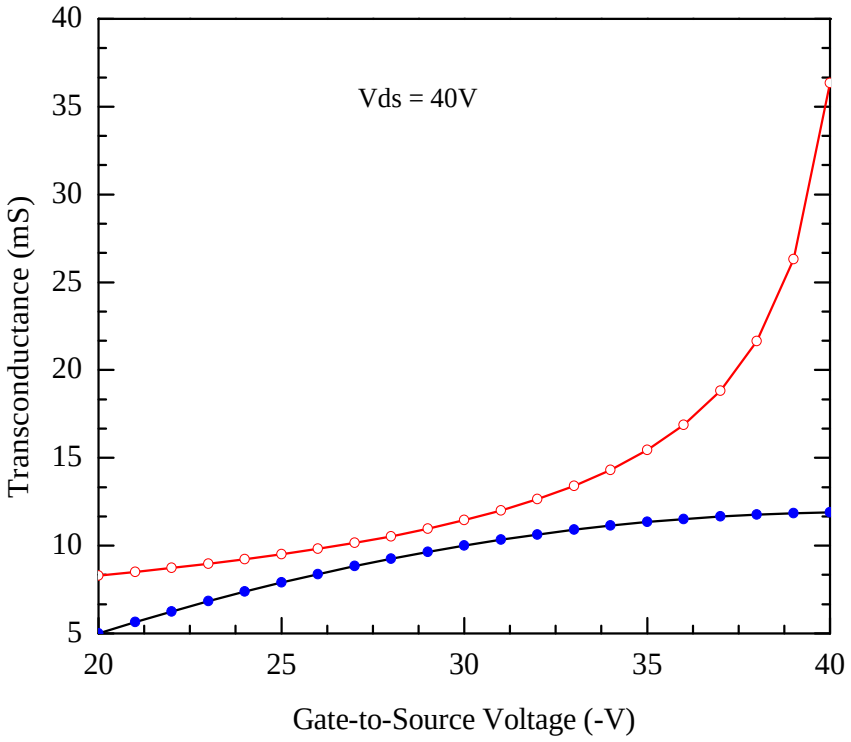


FIGURE 5.9: AC transconducatnce, g_m of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of g_m attained from the conventional approach whereas, solid circles ($\bullet$) show simulated values of g_m using the proposed model.

Unity gain frequency, f_T is an important feature, which determines the AC response of a SiC MESFET [105]. f_T of a submicron SiC MESFET as a function of V_{gs} and V_{ds} is shown in Fig. 5.11. Once again, the values predicted by the conventional model are substantially different than what is received from the proposed model especially, at higher gate biasing, i.e. $V_{gs} = -8$V. Experimentally achieved value of f_T at $V_{gs} = 0$V and $V_{ds} = 40$V is 10.2GHz and for the same biasing, the evaluated values of f_T are 13.63GHz and 9.97GHz for the conventional and the proposed models, respectively. An important feature observed from Fig. 5.11 is the change in the magnitude of f_T by changing V_{gs}. There is a nominal change in the values of f_T by changing $V_{gs} = 0$V to $V_{gs} = -8$V. This is so because, in the proposed model, the changed channel conditions caused by the self heating have been adjusted by I_{ds}, which is experimentally corrected to a reasonable accuracy.

Figure 5.12 represents variation in output resistance, r_0 as a function of V_{ds}. An interesting point, which is exhibited by the plot is that both the models are showing

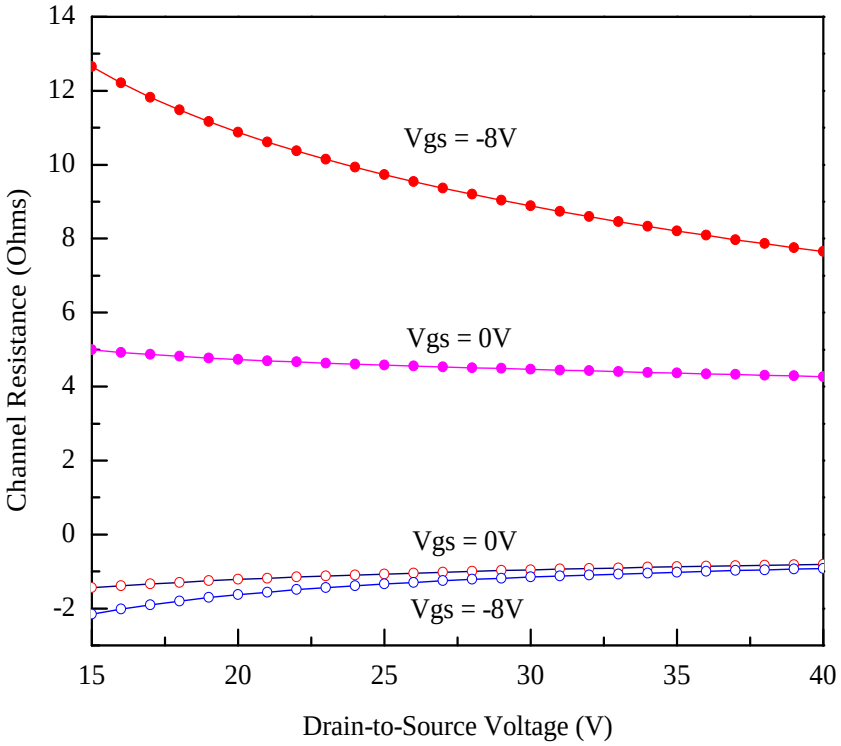


FIGURE 5.10: Channel resistance, R_i of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of R_i attained from the conventional approach whereas, solid circles ($\bullet$) show simulated values of R_i using the proposed model.

a similar increasing trend in r_0 values by increasing V_{ds}; however, the conventional model predicted a linear increase; whereas, the proposed model predicted a non-linear increase in the values of r_0. It is also worth noticing that the non-linear increase, as demonstrated by the proposed model, has two distinct regions. A region defined by $V_{ds} = 0$V to $V_{ds} \approx 17$V followed by a region from $V_{ds} \approx 17$V to $V_{ds} = 40$V. The 1st region is concaved upward whereas, 2nd region is concaved downward. If we assume that scattering of carriers to the buffer layer is nominal [64, 147], then magnitude of r_0 is primarily controlled by the Schottky barrier depletion layer. As is known that changing V_{ds} changes Schottky barrier depletion layer in a non-linear fashion which is precisely evident from ($\bullet$) plot of Fig. 5.12, which as expected, saturates at high V_{ds} potential. Thus, a non-linear increase with concave upward profile represents 1st region and then a non-linear saturation with concave downward profile represents 2nd region of operation. It is assumed that in 1st region of operation, horizonal electric field dominates whereas, in 2nd region of operation, transverse electric field dominates causing inversion of r_0 profile from

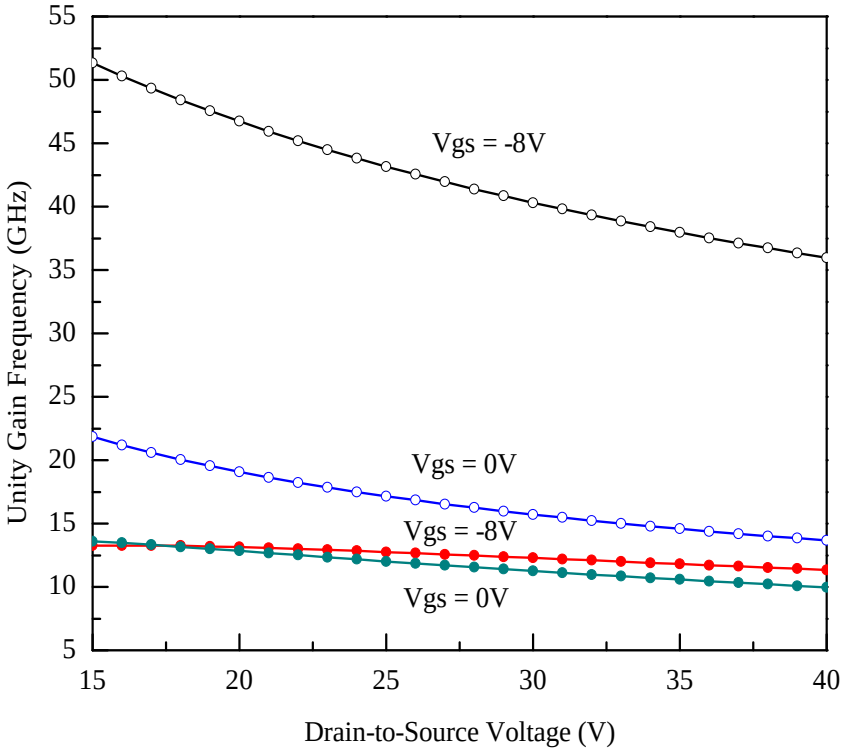


FIGURE 5.11: Unity gain frequency, f_T of a 0.4μm SiC MESFET. Open circles (○) represent values of f_T attained from the conventional approach whereas, solid circles (●) show simulated values of f_T using the proposed model.

concave upward to concave downward.

Table 5.4 summarises intrinsic small signal parameters of a submicron SiC MESFET evaluated using the conventional as well as the proposed models along with experimentally reported data [21]. Examination of the table clearly revealed that values of intrinsic small signal parameters assessed using the proposed model are far better and closer to experimentally achieved values than what is predicted by the conventional model. The fundamental reason of better accuracy of the proposed model is that the modification in Schottky barrier depletion layer caused by the vertical electric field and self heating has been incorporated in the proposed model by involving I_{ds} of the device, which has been experimentally corrected using Eq. 5.14 before assessing small signal elements.

AC equivalent circuit model of a SiC MESFET is shown in Fig. 5.13 [72]. The current source in Fig. 5.13 is dependent on V_{gse}, i.e. the gate voltage drop across C_{gs}

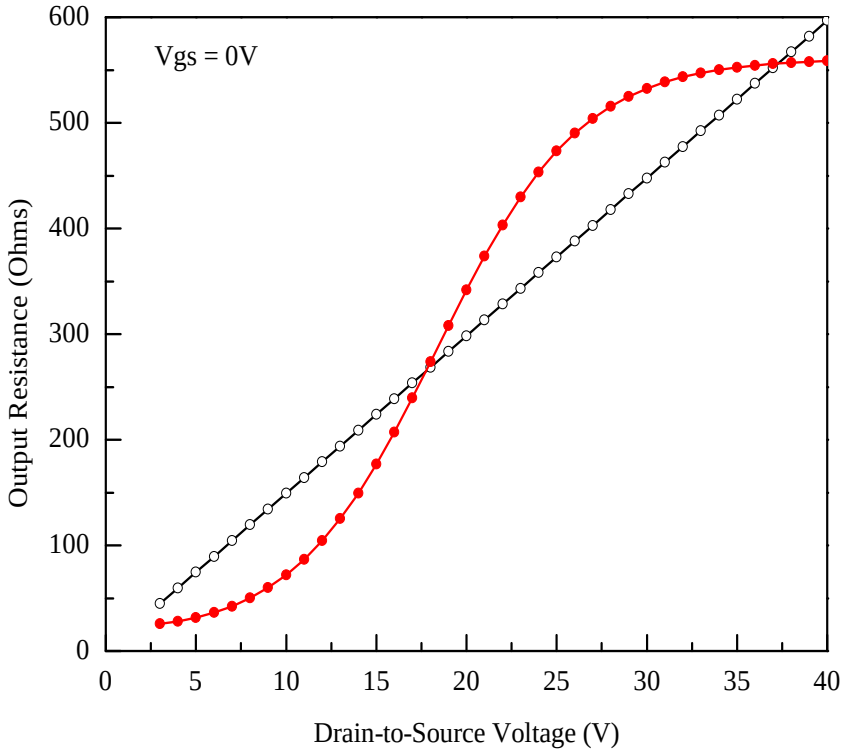


FIGURE 5.12: Output resistance, r_0 of a 0.4μm SiC MESFET. Open circles ($\circ$) represent values of r_0 attained from the conventional approach whereas, solid circles ($\bullet$) show simulated values of r_0 using the proposed model.

TABLE 5.4: Shows experimental and evaluated intrinsic small signal parameters of 0.4μm SiC MESFET.

Parameters	Experimental [21]	Conventional	Proposed
C_{gs}(fF)	164	202	165.6
C_{gd}(fF)	24.1	5.46	24.27
C_{ds}(fF)	62.3	69.39	56.96
g_m(mS)	11.1	36.30	11.90
g_d(mS)	2.0	1.676	1.790
τ(ps)	8.55	5.25	7.98
$R_i(\Omega)$	-	1.17	4.42
f_T(GHz)	10.2	13.63	9.97

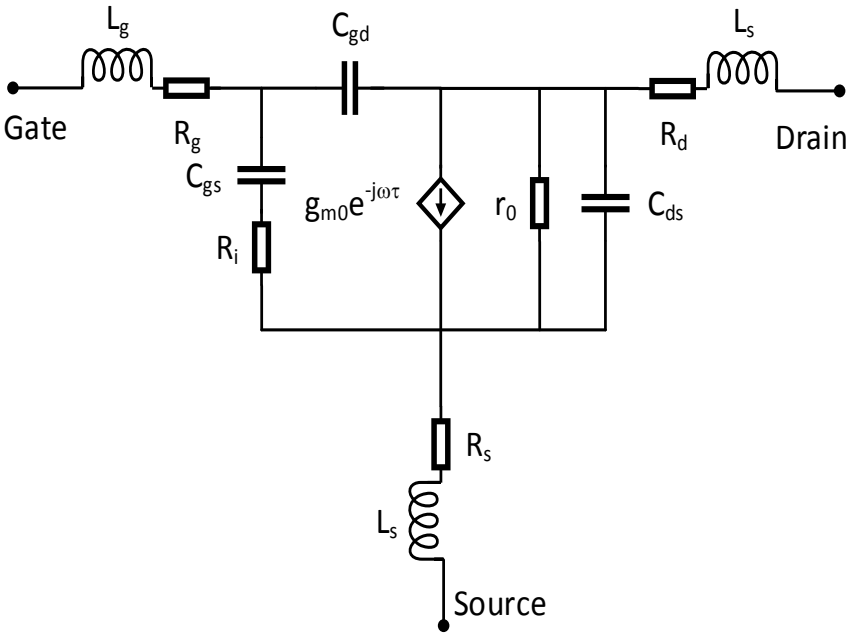


FIGURE 5.13: AC equivalent circuit of a SiC MESFET.

capacitor. It has been established before (Fig. 5.5) that C_{gs} capacitor is primarily dependent on V_{gs} but, it has variation, though small, because of V_{ds} biasing for a submicron device. Further, the conventional model gives poor estimation of C_{gs} thus, the voltage dependent source of the circuit (Fig. 5.13), when used for submicron SiC MESFET, requires a new definition, because of the Schottky barrier depletion layer modification due to intense transverse electric field and/or self-heating effects. It is proposed that the current source should have a combined dependence as $I_{ds} = g_m V_{gse}(\alpha V_{dse})$ where, α is an adjustment variable.

To accommodate V_{ds} dependence in the current source of the circuit shown in Fig. 5.13, it is proposed that variable h_0 of Eq. 5.6 should be replaced with $h(x)$, which is defined by Eq. 5.10. Considering the reduction in v_s as 1.4×10^7cm/s and replacing h_0 with $h(x)$, in Eq. 5.10, the value of g_m evaluated at $V_{ds} = 40$V and $V_{gs} = 0$V is found to be 12.0mS, which is very close to the the actual value given in Table 5.4.

5.5 Summary

In this chapter, a technique has been developed to assess intrinsic small signal parameters of submicron SiC MESFETs. Self heating effects coupled with a high transverse electric field cause depletion layer modification of Schottky barrier gate especially, when channel length is reduced to submicron regime. It has been shown that conventional expressions used to assess FET devices, meant for low voltage operation, lose their accuracy to predict small signal elements of a microwave SiC MESFET. It has been demonstrated that intense channel conditions of a SiC MESFET can be accommodated in a modeling process, if drain-to-source current, I_{ds}, which is determined by the available channel, $a - h(x)$ of the device is first modeled by using an appropriate I_{ds} expression. The accuracy of I_{ds} is achieved by comparing it with experimental data. Subsequently intrinsic small signal expressions are then developed by involving I_{ds} instead of Schottky barrier depletion layer expression, which is conventionally employed to assess the device small signal parameters. Following the same concept, a set of expressions has been developed and its validity for assessing small signal elements of SiC MESFETs has been demonstrated. It has been shown that the developed technique is considerably better in assessing small signal elements of a high voltage FET compared to the conventional technique.

Chapter 6

Conclusion and Future Work

6.1 Introduction

SiC is a wide band-gap material with large breakdown field, high saturation velocity, and high thermal conduction. Owing to these facts, SiC MESFETs are considered excellent candidates for high power microwave applications even in harsh thermal environments. Furthermore, SiC MESFETs offers thermally stable characteristics and under current state of technology, the maximum temperature range to which SiC MESFETs can operate is limited by the ceramic packaging. Of the three materials, Si, GaAs, and SiC, the last one offers highest absolute power density due to large breakdown voltage. Therefore, SiC MESFETs are very attractive for microwave applications such as transmitters and RADARs.

In order to allow these devices to operate at microwave frequencies, it is mandatory that gate length, L_g of the device should be in submicron regime. However, a submicron L_g device requires stringent fabrication constraints and, thus, non-uniformities in the device characteristics are commonly witnessed. Like other MESFETs, submicron SiC MESFETs also exhibit short channel effects.

Short channel effects are classified as second order effects in their nature, imposing additional challenges to engineers and scientists involved in the device modeling;

whereby, making the device's analytical modeling a more demanding and cumbersome task.

SiC MESFET current state of technology, its modeling techniques, especially for the devices having $L_g < 1\mu$m, potential distribution inside the channel under intense conditions and accurate assessment of intrinsic small signal parameters have been the focus of interest in this research. The intended research is accomplished in four parts and the details of which are elucidated in subsequent sections.

6.2 SiC MESFETs

An overview of SiC MESFETs, their characteristics and applications are presented in Chapter-2 of the thesis wherein, progress made so far in the device design to get improved performance is discussed. It is shown that the device has a great potential to be used in microwave communication systems. It is discussed that SiC MESFETs exhibit stable performance at high ambient temperature and also in radiation rich environment. The work reported by different research groups established the fact that SiC MESFETs could stand with high power requirement along with superior linearity characteristics in microwave amplifiers. Furthermore, owing to relatively better thermal conductivity, SiC MESFETs provide superior conduction of the heat generated by the high power operating conditions thus, maintaining their stable performance. The ultimate operating temperature of the device is determined by its packaging, so new packaging materials for the circuits containing SiC MESFETs should be searched to realize full benefits of the device.

Novel structures of SiC MESFETs are also discussed in Chapter-2, which are reported in the literature, to improve the device power handling capabilities and to increase its unity gain frequency, f_T and maximum frequency of operation, f_{max}. To improve transconductance, g_m of the device and to reduce its output conductance, g_0, in the saturation region of operation, different channel layers and recessed technologies are also discussed. It has been established that a thin heavily

doped channel with low drain side resistance would provide a relatively high g_m with improved break down voltage of the device.

To explore the device's fullest capacity and to know its physical behavior, simulation and modeling techniques are usually employed. Analytical, empirical and semi-empirical models developed for SiC MESFETs and their origins are discussed. While reviewing the literature, a need of a comprehensive model, which can predict DC characteristics of the device has been established. Moreover, it is discussed that an accurate AC model is needed to predict intrinsic small signal parameters of the devices designed for microwave power applications.

6.3 SiC MESFET's Analytical Modelling

In this part of the research, a detailed mathematical model describing $I-V$ characteristics of submicron SiC MESFETs has been developed. Poisson's equation with appropriate boundary conditions has been solved to determine potential distribution inside the channel. Location (L_1) of Schottky barrier gate with corresponding depletion layer width (u_1), where the carrier's velocity gets saturated has been identified. It has been demonstrated that, both L_1 and u_1 are biased dependent and their values are changing by changing drain biasing even after the onset of current saturation. This causes a modification in the depletion layer underneath the Schottky barrier gate and, thus, changes the available channel crossection for the flow of current. It has been established that finite output conductance in the saturation region of operation, which is usually observed in submicron devices, can be explained with Schottky barrier depletion layer modification.

$I-V$ characteristics of submicron SiC MESFET are modeled and compared with conventional velocity saturation technique, where the depletion layer after the onset of current saturation has been treated as constant. It has been shown that the proposed technique gave $\sim$15.9% improvement in the modeled output characteristics of a submicron SiC MESFET compared to the best technique reported in the literature.

6.4 SiC MESFET's Semiempirical Modelling

In this part, an improved model to simulate $I-V$ characteristics of submicron SiC MESFETs, designed for microwave power applications, has been developed. The proposed model adequately addresses a non-ideal Schottky behavior, commonly observed in submicron devices, by adjusting the device biasing through simulation variables. Swarm optimization technique has been applied to investigate L_g dependent performance of various SiC MESFETs models. It has been shown that the proposed model provides an improved accuracy, ranging from 7 % to 24 %, compared to the best models available in the literature. This enhanced performance is primarily associated with the extra control, provided by the proposed model to simulate the movement of the depletion region in the channel as a function of applied voltages. An attempt has been made to identify the location underneath the Schottky barrier gate, where the depletion region gets its maximum height and, thus, controls the saturation current of the channel. Physical and electrical parameters of various SiC MESFETs having L_g = 0.4 μm, 0.5 μm, 0.6 μm and 0.7 μm have also been assessed and compared with experimental data. An accurate assessment of the physical parameters of the devices exhibited the validity of the model for submicron SiC MESFETs.

6.5 SiC MESFET's Intrinsic Small Signal Parameters Assessment

In this section, a technique has been developed to assess intrinsic small signal parameters of submicron SiC MESFETs. Self heating effects coupled with a high transverse electric field cause depletion layer modification of Schottky barrier gate especially, when channel length is reduced to submicron regime. It has been shown that conventional expressions used to assess FET devices, meant for low voltage operation, lose their accuracy to predict small signal elements of a microwave SiC MESFET. Thus, there is a need to have a technique, which can predict small

signal elements of submicron SiC/GaN MEFETs, which are specially designed to operate under harsh environment and at high temperature.

It has been demonstrated that intense channel conditions of a SiC MESFET can be accommodated in a modeling process, if drain-to-source current, I_{ds}, which is determined by the available channel of the device is first modeled by using an appropriate I_{ds} expression. Once the accuracy of I_{ds} is achieved by comparing it with experimental data, intrinsic small signal expressions are then developed by involving I_{ds} instead of Schottky barrier depletion layer expression, which is conventionally employed to assess the device's small signal parameters. Following the same concept, a set of expressions has been developed and its validity for assessing small signal elements of SiC MESFETs has been demonstrated. Variation in the device small signal parameters as a function of applied biasing has been discussed in detail. It has been shown that the developed technique is considerably better in assessing small signal elements of a high voltage FET compared to the conventional technique.

6.6 Future Work

The research work carried-out in this thesis can be extended to accommodate the below mentioned topics which could not be covered due to the shortage of time.

1. Since SiC MESFETS are meant for high power applications, as a result, there are self heating effects which cause the channel carriers to become hot. Energetic carriers could potentially generate new carriers under impact ionization mechanism. The start of impact ionization in the channel could have a considerable impact on free carrier density resulting into a possible change in the device's I_{ds}. This behavior could be observed in SiC MESFET at a relatively high biasing, which would possibly modify the device's both output and transfer characteristics. This, as a result, would require a modification in the device modeling parameters and the same could be incorporated both

in semi-empirical and analytical models to make them more comprehensive and thorough for such type of devices.

2. Analytical model developed in Chapter-3, described SiC MESFETs DC characteristics by employing potential distribution inside the channel. The concept of potential distribution inside the channel could be extended further to determine the device's Miller's capacitors and hence, the device intrinsic small signal parameters. Additionally, device parameters, which are temperature dependent might be identified, which could then be incorporated in the model to predict temperature dependent device DC as well as AC characteristics.

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