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High Temperature Modeling of Wide Bandgap Field Effect Transistors

by

Saif ur Rehman

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High Temperature Modeling of Wide Bandgap Field Effect Transistors

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In the memory of my parents

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This is to certify that the research work presented in the thesis, entitled "**High Temperature Modelling of Wide Band Gap Field Effect Transistors**" was conducted under the supervision of **Dr. Muhammad Mansoor Ahmed**. No part of this thesis has been submitted anywhere else for any other degree. This thesis is submitted to the **Department of Electrical Engineering, Capital University of Science and Technology** in partial fulfillment of the requirements for the degree of Doctor in Philosophy in the field of **Electrical Engineering**. The open defence of the thesis was conducted on **June 24, 2019.**

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List of Publications

It is certified that following publication(s) have been made out of the research work that has been carried out for this thesis:-

1. **S. Rehman**, M. M. Ahmed, U. Rafique, and M. N. Khan, "A nonlinear model to assess DC/AC performance reliability of submicron SiC MESFETs," *Journal of Computational Electronics*, vol. 17, no. 3, pp 1199-1209, 2018.

2. **S. Rehman**, M. M. Ahmed, U. F. Ahmed, and M. N. Khan, "Temperature dependent analytical DC model for wide bandgap MESFETs," *IEEE Access*, vol. 7, pp. 49702-49711, 2019.

3. **S. Rehman**, U. F. Ahmed, M. M. Ahmed, and U. Rafique, "An improved space charge distribution analytical model to assess FET's intrinsic capacitors," *Submitted in Turkish Journal of Electrical Engineering and Computer Sciences*, 2019.

4. **S. Rehman**, U. Rafique, U. F. Ahmed, M. N. Khan, and M. M. Ahmed, "Effects of substrate on the AC performance of submicron GaN HEMTs," *Proceedings of 13th International Conference on Emerging Technologies (ICET)*, pp. 1-7, 2017. Retrieved from https://ieeexplore.ieee.org/iel7/8270720/8281648/08281750.pdf

Papers not included in this research

1. M. N. Khan, U. F. Ahmed, M. M. Ahmed, and **S. Rehman**, "An improved model to assess temperature-dependent DC characteristics of submicron GaN HEMTs," *Journal of Computational Electronics*, vol. 17, no. 2, pp. 653-662, 2018.

2. M. N. Khan, U. F. Ahmed, M. M. Ahmed, and **S. Rehman**, "Simulation and comparative analysis of the DC characteristics of submicron GaN HEMTs

for use in CAD software," *Journal of Computational Electronics*, vol. 18, no. 2, pp. 482-491, 2019.

3. M. N. Khan, U. F. Ahmed, M. M. Ahmed, and **S. Rehman**, "An improved temperature dependent analytical model to predict AlGaN/GaN HEMTs AC characteristics," *Accepted in International Journal of Numerical Modeling: Electronic Networks, Devices and Fields*, 2019.

4. **S. Rehman**, H. F. Usman, R. M. Asif, and H. M. Ashraf, "Performance evaluation of submicron SiC MESFET," *Proceedings of International Electrical Engineering Congress (iEECON)*, pp. 1-4, 2018. Retrieved from https://ieeexplore.ieee.org/document/8712187

5. U. F. Ahmed, **S. Rehman**, U. Rafique, and M. M. Ahmed, "AlGaN/GaN FinFET: A Comparative Study," *Proceedings of 14th International Conference on Emerging Technologies (ICET)*, pp. 1-6, 2018. Retrieved from https://ieeexplore.ieee.org/document/8603581.pdf

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Abstract

In 1st part of the thesis, an improved temperature dependent analytical model is presented for wide bandgap MESFETs output characteristics. The model involves self-heating effects, which is a common phenomenon in FETs meant to handle a relatively large current and exhibit negative conductance in their output characteristics. A comparative analysis of modeled and observed characteristics exhibited a significant improvement in the modeled data.

In 2nd part, an analytical model is presented to assess Miller capacitors of FETs. Based on four distinct regions underneath the Schottky barrier gate of the device, analytical expressions are developed to assess Miller capacitors for both linear, as well as, for saturation regions of operation. It is shown that, relative to earlier reported models, the proposed technique exhibited a significant improvement in assessing the device Miller capacitors.

In 3rd part, substrate effects on AC performance of wide bandgap FETs are discussed. A comparative analysis is established, which demonstrated that both Si and SiC substrates are equally good, and there is a nominal change in the AC performance of the device by changing the substrate from Si to SiC. Particle swarm optimization technique is used to achieve optimized intrinsic parameters by involving measured S-parameters. It is established that Si substrate, which is considerably cheaper than SiC, could comfortably be employed to fabricate submicron GaN HEMTs.

Finally, 4th part of the thesis presents a nonlinear model to simulate the $I - V$ characteristics of submicron SiC FETs. The region where the Schottky barrier gate loses its control on the channel current, because of the high biased, is successfully modeled for better understanding of the device operation. It is shown that the device performance drastically affected when transconductance to output conductance ratio is less than unity. By attaining accurate compliance between the observed and modeled output characteristics, even for those conditions where the channel is behaving erroneously, device AC parameters are extracted to predict the reliability of the device characteristics under intense operating conditions.

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Abbreviations

AC	Alternating current
AlN	Aluminium nitride
AlGaN	Aluminium gallium nitride
Al_2O_3	Aluminium oxide
ADS	Advanced design system
BFM	Baliga figure of merit
BHFFM	Baliga high frequency figure of merit
C-V	Capacitance-voltage
CAD	Computer aided design
DC	Direct current
DIBL	Drain induced barrier lowering
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
GSW	Gaussian standing wave
GA	Genetic algorithm
HEMT	High electron mobility transistor
I-V	Current-voltage
JFET	Junction field effect transistor
JFM	Johnson figure of merit
KFM	Keyes figure of merit
MESFET	Metal semiconductor field effect transistor
MMIC	Monolithic microwave integrated circuit
MAG, MSG	Maximum available and stable gain

NF	Noise figure
PAE	Power added efficiency
PD	Power density
PGA	Post gate anealing
PSO	Particle swarm optimization
QW-EBL	Quantum well electron blocking layer
RF	Radio frequency
RMSE	Root mean square error
Si, SiC	Silicon and silicon carbide
SiGe	Silicon germanium
SI	Semi-insulating
SPICE	Simulation program with integrated circuit emphasis
SSM	Small signal model
VNA	Vector network analyzer
2D	Two dimensional
2DEG	Two dimensional electron gas

Symbols

a	Channel epi-layer thickness
A	Area of the device
b	Buffer layer thickness
c	Speed of light
C_{DS}, C_{GS}, C_{GD}	Drain-to-source, gate-to-source and gate-to-drain capacitances
C_{PD}, C_{PG}	Drain and gate pad capacitances
C_{total}	Total capacitance
C_{sub}	Substrate capacitance
E	Applied electric field
E_s	Saturation field
E_g	Energy band-gap
f_T	Unity gain frequency
G_M, G_D	Transconductance and output conductance
G_{MT}, G_{DT}	Temperature dependent transconductance and output conductance
G_{ML}, G_{DL}	Linear region transconductance and output conductance
G_{MS}, G_{DS}	Saturation region transconductance and output conductance
G_{epi}, G_{sub}	Conductances of epi-layer and substrate
$h(x)$	Depletion layer height at any point x
h_0, h_d	Depletion layer height nearer to the source and drain
h_1	Depletion height where carriers attain υ_s
I_D	Drain current

I_{DS}, I_{DSS}	Drain-to-source current
$I_{DS(lin)}, I_{DS(sat)}$	Linear and saturation region I_{DS}
I_{DST}	Temperature dependent drain-to-source current
$I_{DS(exp)}, I_{DS(sim)}$	Experimental and simulated drain-to-source current
I_P	Pinch-off current
I_M	Current source
L_g	Gate length
L_{GD}	Gate-to-drain length
L_i	Channel length at specific location
L_s, L_d	Separation between source-gate and drain-gate
L_S, L_D, L_G	Source, drain and gate side inductances
N	Carrier concentration
N_b	Buffer layer doping density
N_D	Channel doping concentration
P_{out}	Output power
Q_i	Charge at specific location
q	Electron charge
R_S, R_D, R_G	Source, drain and gate side resistances
R_{DS}	Drain-to-source resistance
R_C	Contact resistance
R_I	Input resistance
R_{TH}	Thermal resistance
R_{CH}	Channel resistance
S_{ij}	Scattering parameters
T, T_{max}	Absolute and maximum temperature
u_0, u_d	Normalized depletion layer width near source and drain electrodes
u_1	Depletion width where carriers attain v_s
V_G	Gate voltages
V_{GS}	Gate-to-source voltages
V_D	Drain voltages

V_{DS}	Drain-to-source voltages
$V_{D(sat)}$	Saturation voltage
$V(L_i)$	Potential across the specific length
V_T	Threshold voltage
ΔV_T	Shift in threshold voltage
V_{bi}	Built-in potential
V_{Br}	Breakdown voltage
V_P	Pinch-off voltage
W	Gate width
x_p, x_n	Depletion thickness layer towards the buffer and the channel
Y_0	Admittance
$\alpha, \beta, \gamma, \psi, \xi, \lambda, \lambda_2, \delta$	Fitting parameters
μ	Electron mobility
μ_0	Low field mobility
ε_s	Relative permittivity of a semiconductor material
ε_0	Permittivity of free space
υ	Velocity
$\upsilon_s, \upsilon_{sat}$	Saturation velocity
κ	Thermal conductivity of material and Rollet's stability factor
τ	Transit delay time
ω	Angular frequency

Chapter 1

Introduction

1.1 Background

Great progress has been made in the field of electrical power systems after the invention of transistor and thyristor. The main purpose of these devices is to handle current and voltage at high power and frequency. Numerous semiconductor devices are currently being used in the industry, but none of them have achieved more popularity than transistor.

In 1925, an Austro-Hungarian Physicist Julius Edgar Lilienfield presented the idea of field effect transistor (FET) and was granted a patent in 1930 [1]. Oskar Heil also presented various patents on FETs and was one of the inventors of FETs [2]. In 1947, William Shockley and his team developed first practical junction field effect transistor (JFET) [3]. Shockley's efforts opened the new door for the development of commercialized FETs.

In 1966, Mead [4] developed a FET by replacing p-n junction with a Schottky junction beneath the gate, and used compound semiconductor material such as GaAs and named it metal semiconductor field effect transistor (MESFET). MESFETs can operate at high frequencies, and offer significant power efficiency and output power density (PD). FETs high frequency and power operations were further improved with the invention of high electron mobility transistors (HEMTs).

Both MESFETs and HEMTs are favorable devices for harsh environment due to their wide bandgaps, and they have relatively high thermal conduction allowing the device to function at elevated temperature.

1.2 Wide Bandgap Semiconductors

Silicon (Si) and Gallium Arsenide (GaAs) are the 1st and 2nd generation semiconductor materials, respectively; while Silicon Carbide (SiC) and Gallium Nitride (GaN) are known as the 3rd generation semiconductor materials [5]. Si/GaAS have narrow band gaps with values 1.12 eV and 1.4 eV, respectively; as given in Table 1.1, while SiC and GaN have wide bandgaps ($>$ 3 eV). Wide bandgap semiconductors are suitable for high power and high temperature devices, as they retain their fundamental characteristics at high operating temperature (500 °C). FETs fabricated using wide bandgap semiconductors have superior performance compared to GaAs and Si based FETs [6].

The superior electrical characteristics offered by SiC and GaN devices are primarily associated with the material's high thermal conductivity, radiation hardness and immunity to hot carriers degradation [7]. Table 1.1 shows the average properties of different semiconductor materials normally used in microelectronic industry [8]. Data of the table show that as compared to other materials, SiC and GaN have high υ_s and κ, which leads to high switching speed and operating voltages.

Generally, at high temperature and frequency, electrical properties of a device change rapidly. Electrical parameters such as υ and μ have strong dependence on temperature and play a significant role in determining the device performance. The magnitude of υ is inversely proportional to temperature and its variation with E is given by [9]

$$\upsilon(E) = E \times \mu(E) \tag{1.1}$$

TABLE 1.1: Average properties of semiconductor materials [8].

Material	E_g (eV)	ε_r	μ (cm^2/Vs)	υ_s (cm/s)	E (MV/cm)	κ (W/cm.K)	T_{max} (°C)
Si	1.12	11.7	1400	1×10^7	0.3	1.5	300
GaAs	1.4	12.8	8500	1×10^7	0.4	0.5	300
GaN	3.39	9.00	900	2.5×10^7	3.3	1.3	600
4H-SiC	3.26	9.66	1000	2.2×10^7	2.0	4.9	700

where

$$\mu(E) = \frac{\mu_0(T,N)}{\left[1+\left(\frac{\mu_0 E}{\upsilon_s}\right)^{\beta}\right]^{1/\beta}} \tag{1.2}$$

Here $\mu_0(T,N)$ represents low field mobility and it is a function of temperature and carrier concentration. Figure 1.1 shows υ vs. E plot with temperature as a variable [10]. Figure 1.1 shows that υ decreases as temperature increases, and it saturates at high values of E. At elevated temperature, the lattice vibrate with high amplitude, which offers more scattering to the drifting carriers resulting into reduced υ.

1.3 Figure of Merit

Figure of merit is the criteria by which one can judge the performance of semiconductor materials. In 1968, Johnnson et al. [11] defined a simple analysis that limits the performance of a device as a product of E and υ_s. Johnson's figure of merit (JFM) can be expressed as:

$$\text{JFM} = \sqrt{\frac{E\upsilon_s}{2\pi}} \tag{1.3}$$

Keyes [12] has also given a figure of merit known as Keyes figure of merit (KFM), which has been developed by using material's properties and their thermal effects.

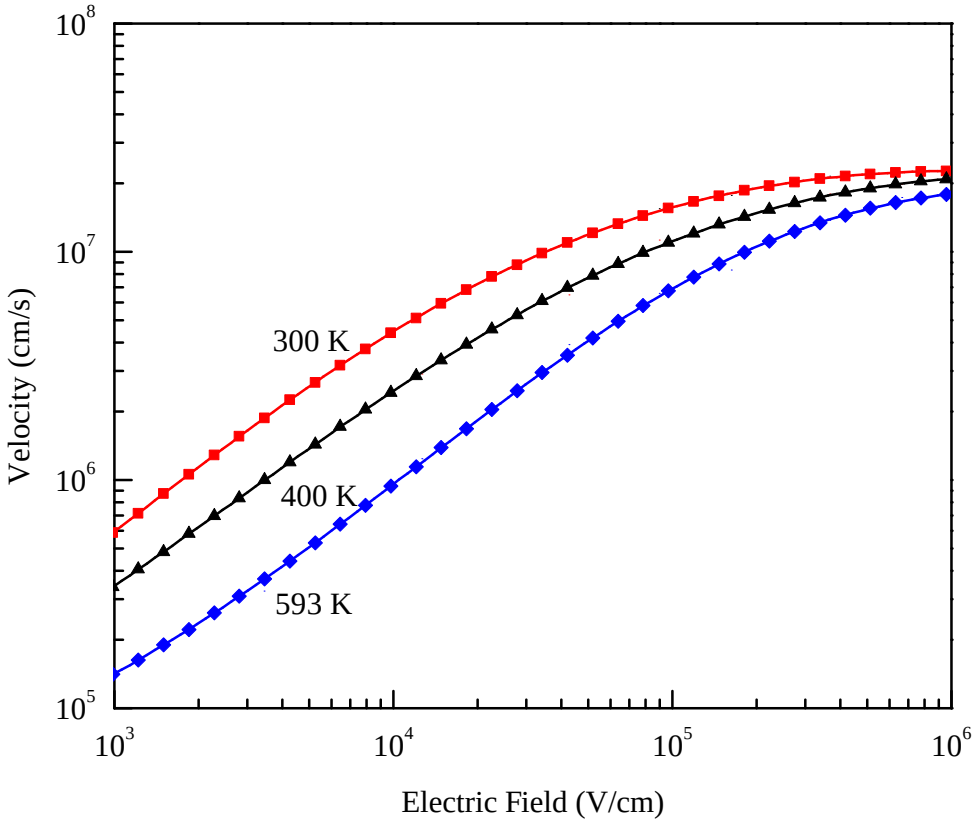

FIGURE 1.1: Electron drift velocity as a function of electrical field for different temperatures [10].

Equation (1.4) gives KFM wherein, material properties are represented by ε_s and thermal effects by κ.

$$\text{KFM} = \kappa\sqrt{\frac{c\upsilon_s}{4\pi\varepsilon_s}} \tag{1.4}$$

Baliga [13] also tried to quantify the operating capacity of a high power device and gave another figure of merit for such devices known as Baliga figure of merit (BFM), and it is given by

$$\text{BFM} = \varepsilon_s\mu_0 E_g^3 \tag{1.5}$$

For higher frequencies, switching loss occurs due to capacitance charging and discharging of a device. A good material should have a high critical field and large value of μ at higher frequencies for switching applications. Therefore, Baliga also presented an expression for high frequency applications, which is known as Baliga

TABLE 1.2: Figure-of-merits for different materials [15].

Material	JFM	KFM	BFM	BHFFM
Si	1	1	1	1
GaAs	11	0.45	28	16
4H-SiC	410	5.1	290	34
6H-SiC	260	5.11	90	13
GaN	790	1.8	910	100

higher frequency figure of merit (BHFFM) [14] and is given by

$$\text{BHFFM} = \frac{\mu_0 E_g^2}{2}\sqrt{\frac{V_G}{V_{bi}}} \tag{1.6}$$

where V_G is the gate voltage and V_{bi} is the built-in potential of the device. Table 1.2 shows a comparison of different figure of merits normalized with respect to Si. According to the data of the table, SiC and GaN are the materials of future for microwave and power devices.

1.4 Metal Semiconductor Field Effect Transistor (MESFET)

Figure 1.2 shows a crosssectional view of a MESFET. Gate is the main electrode, which controls the flow of current by controlling the thickness of the Schottky barrier layer. A MESFET device is biased by applying gate-to-source, V_{GS} and drain-to-source, V_{DS}, voltages. The drain-to-source current, I_{DS}, is dependent both on V_{DS} and V_{GS} [16]. In an n-channel MESFET, electrons flow from source to drain inside the channel, which is defined by the doped epitaxial layer grown on semi insulating (SI) substrate. Substrate, as shown in Fig. 1.2, offers high resistance and thus, confines the drifting carriers inside epitaxial layer, a. The gate length, L_g determines high frequency capabilities of the device, and a small value of L_g facilitates faster switching.

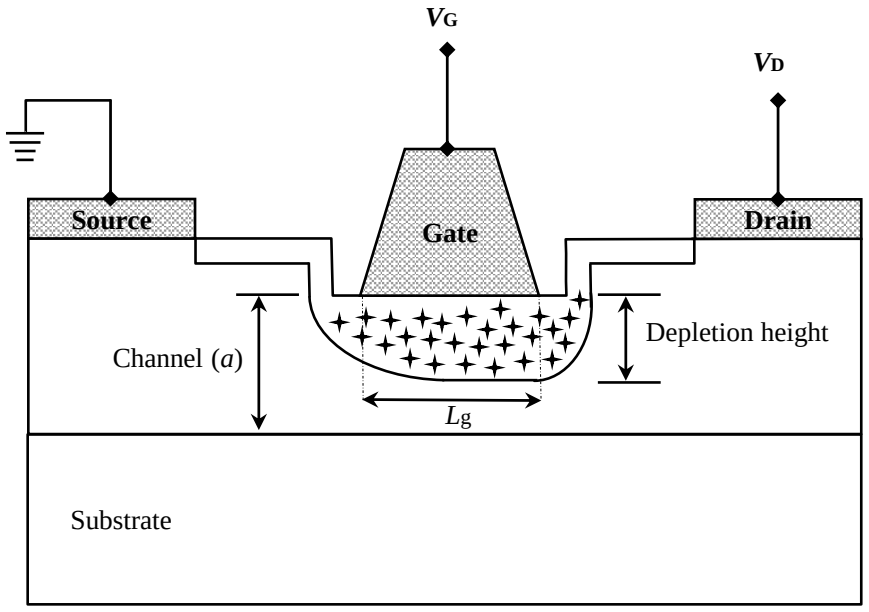

FIGURE 1.2: A crossectional view of an operating MESFET; illustrating recessed gate technology.

In Fig. 1.2, the gate of the MESFET is sitting in a recess, and the technology is therefore, known as recessed gate technology. Such a technology is employed to reduce gate-to-source resistance and to allow the gate metal to sit at relatively low doped ($\sim 10^{17}$) channel layer for the devices having heavily doped contact layer ($\sim 10^{18}$); normally employed to reduce the ohmic contact resistance of drain and source contacts [17].

Height of the variable a, as shown in Fig. 1.2, determines the target current of the device. At $V_{GS} = 0$ V, if $a - h(x)$ has value greater than zero; would mean that there is a finite channel thickness available for the conduction of current, and the device will be known as normally off device. Such devices need gate voltages to get the channel pinched and the magnitude of V_{GS}, where $I_{DS} \sim 0$ A, is referred to as pinched-off voltage, V_P [18].

Almost all types of MESFETs have similar behavior for output characteristics, i.e. cut-off, linear and saturation region of operation. At low biasing, they operate in linear region and at high biasing, output current saturates abruptly and cut-off region occurs for biasing higher than V_P.

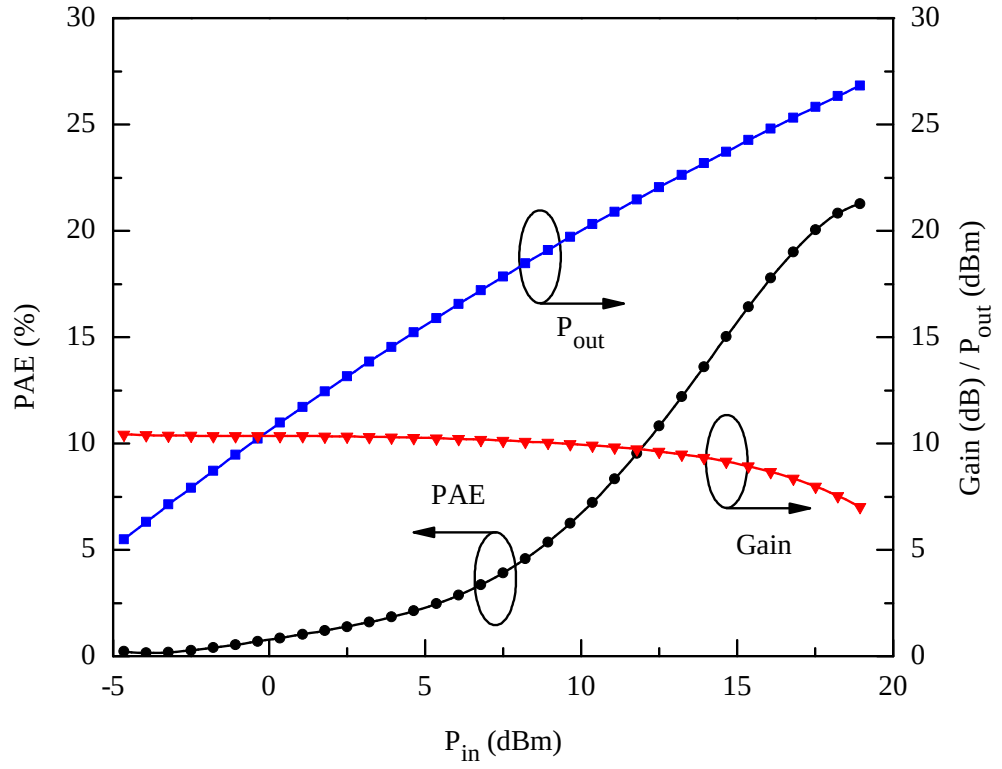

FIGURE 1.3: Input/output power characteristics of 4H-SiC MESFET [20].

Finally, the material chosen for the fabrication of a MESFET plays a crucial role in determining the characteristics of the device. SiC and GaN wide bandgap materials are very promising for microwave power MESFETs, and developing models to predict their DC and AC characteristics can play a role in the future growth of microelectronic industry.

PD and power added efficiency (PAE) are two important parameters for microwave power MESFETs. The reported power performance of SiC MESFETs is very promising and such devices can comfortably offer PAE = 70% and PD = 7.7 W/mm [19]. Figure 1.3 shows input-output power characteristics of a 4H-SiC MESFET with L_g = 0.5 μm and gate width, W = 100×2 μm at 2 GHz. At maximum input power, PAE = 21.1%, PD = 2.1 W/mm, and power gain = 10.6 dB [20].

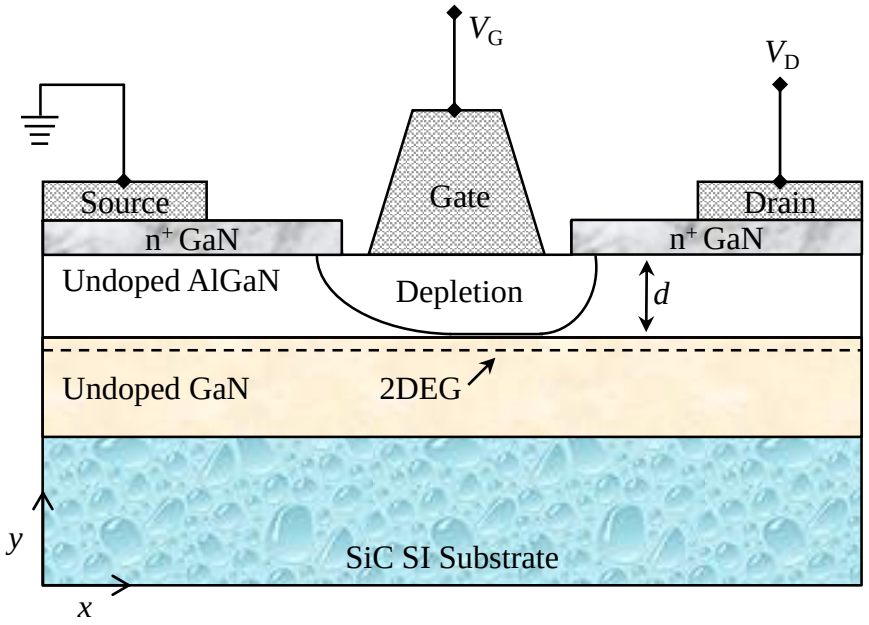

FIGURE 1.4: Crosssectional view of HEMT.

1.5 High Electron Mobility Transistor (HEMT)

An extension in the MESFET structure, for specific high frequency applications wherein, enhanced carriers mobility is needed, led to the invention of high electron mobility transistor called HEMT. In an HEMT, carriers are trapped in a quantum well defined by the combination of two layers having different E_g energies. This generates a discontinuity at the interface; leading to the generation of a quantum well, which at equilibrium trap carriers. These carriers define a two dimensional layer referred to as 2DEG, as shown in Fig. 1.4 [21], and they are responsible to define the device I_{DS}. Since these carriers are trapped in between two layers thus, they experience minimum lattice scattering and have high velocity. Concentration of these carriers is dependent upon the layers defining the heterostructure and in some materials; such as AlGaN/GaN, 2DEG can be created even without the donor layer, which further improves the device performance [22].

A simple HEMT structure is shown in Fig. 1.4, which consists of a thin undoped Aluminum Gallium Nitride (AlGaN) layer followed by an undoped GaN layer. On top of AlGaN layer, there is an n^+-GaN contact layer, which is used to minimize

TABLE 1.3: A relative performance of depletion type MESFET and HEMT of similar dimensions designed for microwave applications.

Parameter	**MESFET**	**HEMT**
Threshold voltage, V_T	∼-2 V	∼-1 V
Transconductance, G_M	∼150 mS/mm	∼200 mS/mm
Breakdown voltage, V_{Br}	Relatively Low	Relatively High
Capacitances C_{GS}, C_{GD}	Monotonically varies	Decrease rapidly
Power handling capacity	∼0.5 W/mm	∼0.8 W/mm
Power added efficiency	Relatively Low	Relatively High
Operating temperature	∼500 °C	∼700 °C
Operating frequency, f_T	∼100 GHz	∼150 GHz
Noise Figure, NF	∼0.5 dB	∼0.4 dB
Gain	∼8 dB	∼12 dB

contact resistance of drain-source ohmic contacts. Electrons defining 2DEG accumulate between AlGaN/GaN layers, where the potential well is created. μ of the 2DEG electrons will depend upon the channel temperature and the scattering they will experience. Since, in general, 2DEG electrons have relatively lower scattering therefore, HEMTs offer comparatively high gain and low noise figure (NF) even at elevated temperatures.

First wide bandgap HEMT was reported by Khan et al. in 1993 [24] with promising high power and frequency applications. Its growth continued and today, wide bandgap HEMTs are frequently employed in high power electronics. These devices, though expensive than MESFETs, are preferred because they have capabilities to operate below liquid nitrogen temperature to facilitate space applications and also at high temperature (∼700 °C) such as engine environment. Table 1.3 provides a performance comparison between MESFET and HEMT of similar dimensions designed for micro wave applications. It is evident from the data of the table that a HEMT device offers relatively improved performance when compared to a MESFET of similar dimensions and operating conditions.

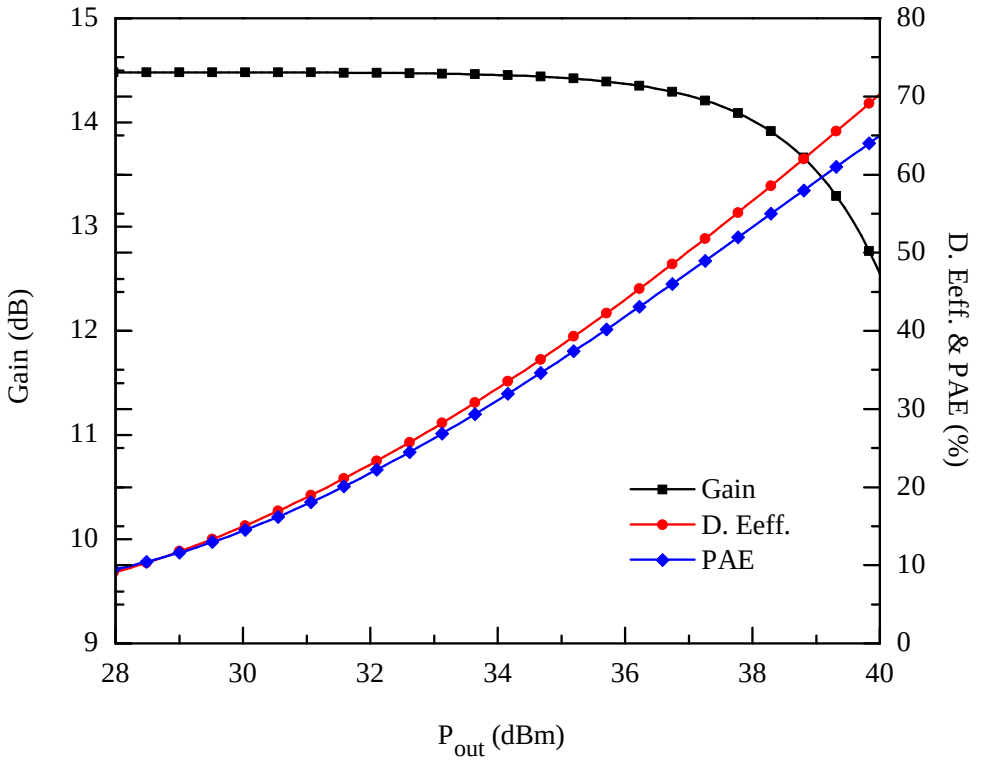

FIGURE 1.5: Gain, drain efficiency and PAE versus P_{out} of a HEMT device for $V_{DS} = 28$ V at 6 GHz [25].

HEMTs are usually not preferred for power amplifiers, as charge density in these devices is relatively low. However, normalized transconductance, G_M of these devices is normally better than MESFETs, which leads to high gain and cut-off frequency, f_T along with low NF. Due to these facts, HEMTs are preferred for low noise amplifiers and in frequency mixers. Figure 1.5 shows response of an HEMT at 6 GHz [25]. As a general trend, drain efficiency and PAE increase as output power increases, but gain of the device decreases at high output power. Performance of an HEMT primarily depends upon: a) the layers structure, which defines the heterostructure; b) the substrate used to hold the layers; c) the device geometry and d) the device physical dimensions. These parameters shall be explored, in detail, in this research to have a better understanding of the device for its possibly improved industrial utility.

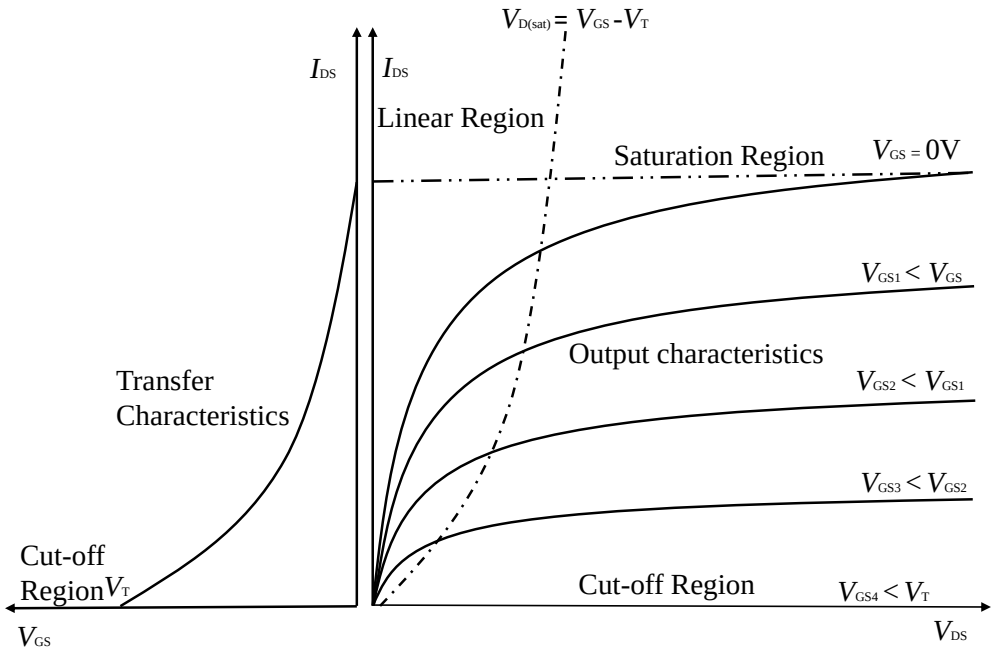

FIGURE 1.6: $I - V$ characteristics of an n-channel FET.

1.6 Output Characteristics of FETs

Figure 1.6 represents output (RHS) and transfer (LHS) characteristics of a FET. Both MESFET and HEMT devices exhibit same type of characteristics when observed as a function of V_{GS} and V_{DS}. The only difference is that in MESFETs, I_{DS} is controlled by the channel thickness $a - h(x)$, as shown in Fig. 1.2; whereas, in HEMT, it is the 2DEG, which controls I_{DS} of the device. At $V_{GS} = 0$ V and $V_{DS} > 0$ V, there is maximum channel available for the flow of current and assuming that υ is directly proportional to the applied field caused by the V_{DS}, then there would be a linear increase in the I_{DS} vs V_{DS} profile, as evident from the output characteristics of Fig. 1.6. This would be true for smaller values of V_{DS} that is $V_{DS} < V_{DS(\text{sat})}$, where $V_{DS(\text{sat})}$ is the voltage required to attain saturation velocity, υ_s. For higher magnitude of V_{GS}, there would be reduction in the corresponding values of $V_{DS(\text{sat})}$ and a combination of these points will generate a curve shown by the dotted lines in Fig. 1.6. Thus, the dotted curve separates linear region from the saturation region of operation as marked in the figure.

In the saturation region, carriers are drifting with the velocity referred to as υ_s;

resulting into, under ideal conditions, a constant I_{DS}. But, in an actual device, there could be many second order effects, which could lead to a non-ideal behavior of the device. In Fig. 1.6, there is a finite output conductance, G_D, causing a positive slope of the output characteristics in the saturation region of operation. The reasons and causes of this slope and how it could affect the performance of a MESFET/HEMT would be discussed in the later part of this thesis.

In Fig. 1.6, the LHS shows transfer characteristics of the device wherein, at a fixed V_{DS}, the response of the device is observed by sweeping V_{GS} values. The point where the curve touches the y-axis, is the point at $V_{GS} = 0$ V and the corresponding value of I_{DS} is known as I_{DSS}. At this condition, the Schottky barrier potential defines V_{bi}. On the other hand, the point where $I_{DS} = 0$ A, is the point where $a - h(x) = 0$ nm for MESFET, or in case of HEMT, carriers defining 2DEG = 0, represent that the device channel is fully pinched-off. The magnitude of V_{GS} required to attain this condition is referred to as $V_{GS} = V_P$ or V_T and is given by [26]

$$V_T = \frac{qNa^2}{2\epsilon_r\epsilon_0} - V_{bi} \tag{1.7}$$

where q is the electronic charge, N is the carrier concentration typically $\sim 3\times10^{17}$ cm^{-3} for n-channel, ϵ_r represents relative permittivity of the semiconductor involved and ϵ_0 denotes permittivity of free space.

1.6.1 Transconductance, G_M

Transconductance is one of the most important electrical parameters of the device, which describes the output current in terms of the change in gate swing voltage. It is also called mutual conductance of the device and denoted as G_M. Mathematically, one can write G_M as:

$$G_M = \frac{\partial I_{out}}{\partial V_{in}} = \frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{V_{DS}=\text{Cons}} \tag{1.8}$$

For FETs, it is the ratio of change in I_{DS} to the change in V_{GS} keeping V_{DS} constant. For high frequency applications, G_M plays an important role, as it controls the gain of the device that varies with frequency. Also, G_M is affected by the device topology, dimensions and the material engaged in the device fabrication. In general, it increases with the increase in W & N_D, and its variation as a function of L_g is nonlinear. A reduction in the device L_g increases G_M in first instance, but it saturates for $L_g < 0.1$ μm [27]. It is an established fact that for high G_M devices, N_D should be as high as possible and at the same time, a should be as thin as it could be [21]. Since, the upper value of N_D is limited by the device Schottky barrier leakage and a by the V_P it is, therefore, a trade-off should be made and their optimum values will be determined by the device specific applications.

Since the device performance is temperature dependent and the basic purpose of this research is to evaluate MESFET/HEMT reliabilities under intense operating conditions, a feel of G_M variation as a function of temperature is given in Fig. 1.7 [28]. The plot of the figure shows that G_M decreases with increasing values of temperature and hence, there could be a limit when the device characteristics might not be in conformity to the design requirements.

1.6.2 Output Conductance, G_D

Output conductance, G_D, when measured in the saturation region of operation represents a non-ideal behavior of the device. A positive G_D, after the onset of current saturation, indicates that the device is not a perfect current source in the saturation region of operation, and a finite conductance could then be associated either with buffer conductance or depletion layer modification caused by drain induced barrier lowering (DIBL). The value of G_D is the most unpredictable parameter in the device modeling and usually its value is estimated by involving the device second order effects in the device physics. Mathematically, G_D can be expressed as:

$$G_D = \frac{1}{R_I} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} \tag{1.9}$$

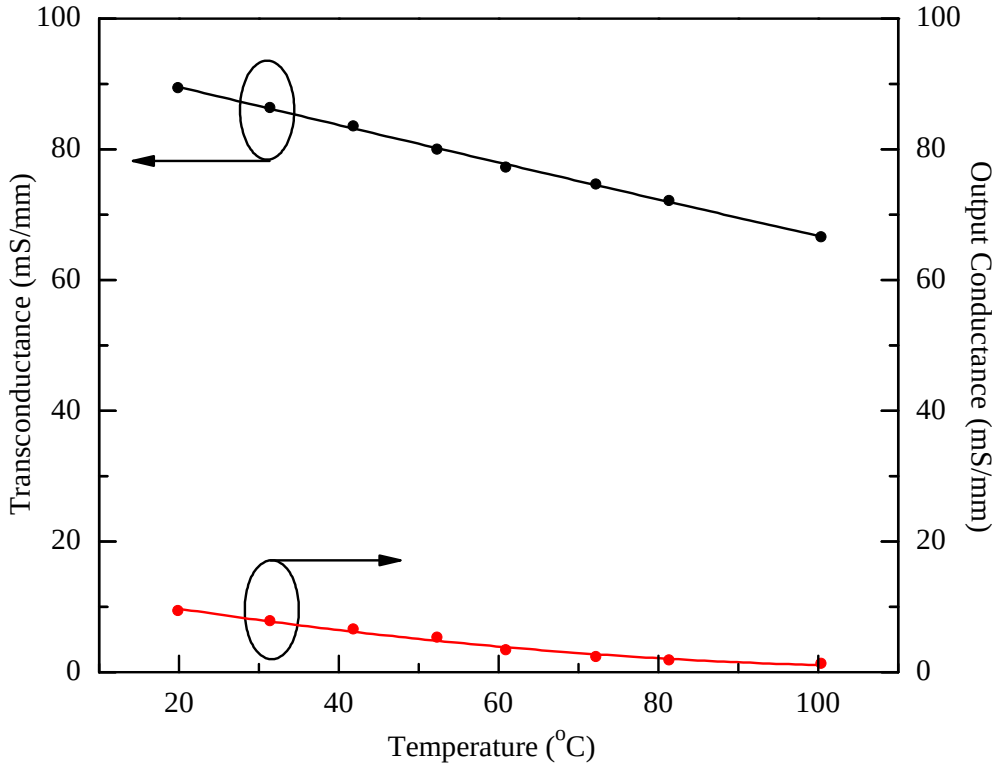

FIGURE 1.7: Temperature dependent variation in G_M and G_D of a MESFET [28].

where R_I is the channel resistance, which sits in parallel to the current generator defining the device behavior in the saturation region.

A negative value of G_D would mean that there is a reduction in the current magnitude with increasing values of V_{DS}. This aspect is observed, particularly in the devices, which are designed for power applications. In wide bandgap semiconductors, at relative high bias or at elevated temperatures, the channel of the device gets heated, and a simple definition of G_D, given by Eq. (1.9), might not be valid. Experimental data indicating dependence of G_D on the ambient temperature is given by Fig. 1.7. The figure once again represents a decreasing trend in G_D with increasing values of temperature as that of G_M [28]. However, the response of the device, in the saturation region of operation, especially, under intense operating conditions, cannot be explained by a simple space charge limited current model. This thesis, apart from other aspects, aims at developing a technique, which could possibly explain the behavior of wide bandgap MESFETs/HEMTs in

the saturation region of operation especially, the nature of G_D and its dependence on relatively high bias.

1.7 Intrinsic/AC Model Parameters of FETs

To cater high frequency needs, submicron MESFETs/HEMTs are fabricated and at the same time, to improve their power handling capability, the device width is enhanced by adopting interdigitated technology. The device AC performance is assessed through S-parameters measurement, which enables a design engineer to evaluate the device intrinsic and extrinsic parameters, and to sketch its AC equivalent circuit by using de-embedding techniques.

Normally, there is a discrepancy between the observed and evaluated AC parameters, which implies that the mathematical model used to describe the circuit behavior does not give good conformity with the observed AC characteristics for varying device conditions. These effects are prominent when the device size is reduced to submicron level, which causes shift in the device V_T, compression in G_M, and generate high G_D in the saturation region of operation.

Figure 1.8 illustrates all extrinsic and intrinsic elements of a FET equivalent circuit. Intrinsic parameters are bias dependent and are the function of the depletion underneath the Schottky barrier gate, while extrinsic parameters are bias independent [29], but they are dependent upon the device geometry, material used and the fabrication technology involved. Intrinsic parameters are gate-to-source capacitance, C_{GS}, gate-to-drain capacitance, C_{GD}, drain-to-source capacitance, C_{DS}, transit delay time, τ, G_M, drain-to-source resistance, R_{DS} and R_I.

In the extrinsic part of the circuit, shown in Fig. 1.8, R_D, R_S, and R_G represent drain, source and gate resistances, respectively; L_D, L_S, L_G are the inductances of drain, source and gate side, respectively; while C_{PG} and C_{PD} are the pad capacitors of gate and drain, respectively. These capacitances are also called stray capacitances or parasitic capacitances. Some parameters are linear, while others

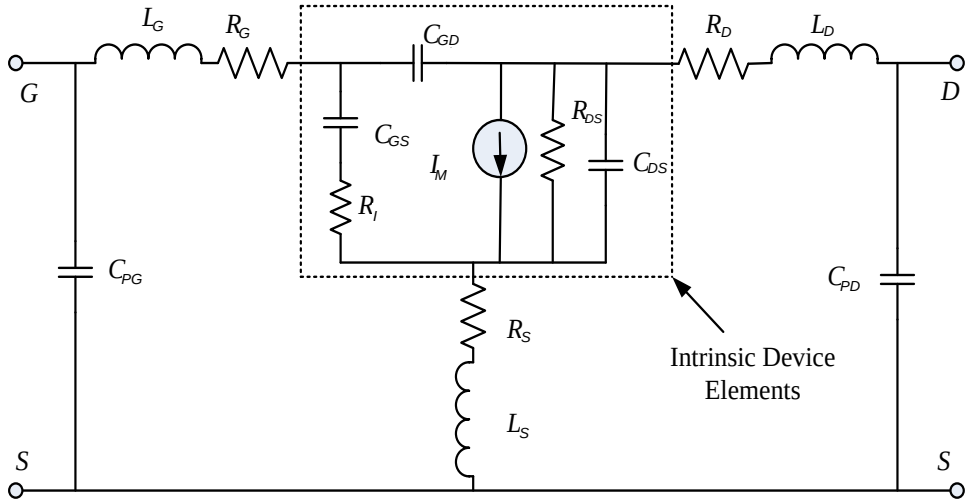

FIGURE 1.8: AC equivalent circuit model of a common source configuration MESFET.

have nonlinear behavior such as C_{GS}, C_{GD} and I_{DS}. Device onset current saturation is defined by I_M current source, which is sitting in parallel to R_{DS} resistor. Any non-ideality in the device behavior after the onset of current saturation will be accommodated by the R_{DS} resistor. Low frequency AC response is determined by C_{PG} and C_{PD}, whilst the high frequency response is primarily controlled by the Miller capacitors, i.e. C_{GS}, C_{GD} and C_{DS}.

1.7.1 Transit Time Delay, τ

Transit time delay, τ is the time in which the device conductance redirects itself by the change of V_{GS}. It is also the charging and discharging time of the gate depletion. It depends on G_M magnitude, and for high speed, frequency and gain, it is desirable that the value of τ should be as low as possible. Physically, it depends on L_g of the device and reduction in L_g results in less transit time delay ~ 1 psec. Mathematically, it can be expressed as:

$$\tau = \frac{L_g}{V_{GS}} \tag{1.10}$$

1.7.2 Channel Resistance, R_I

Channel resistance also called charging resistance, R_I is the intrinsic resistance under the gate between source and channel. For RF applications, R_I is used to determine the time required to charge that part of depletion where carriers are moving with υ_s.

1.7.3 Intrinsic Capacitances

C_{GS}, C_{DS} and C_{GD} play an important role in evaluating the AC behavior of the device. Total charge, Q, under the Schottky barrier gate, determines the values of these capacitors. A variation at the gate electrode caused by the input signal will create a change in Q, which will then be translated into new values of C_{GS} & C_{GD}. By differentiating Q with respect to V_{GS}, keeping V_{DS} constant, one can get C_{GS}, while C_{GD} can be attained by differentiating Q with respect to V_{DS}, keeping V_{GS} constant. Mathematically, C_{GS} and C_{GD} can be expressed as:

$$C_{GS} = \left.\frac{\partial Q}{\partial V_{GS}}\right|_{V_{DS}=\text{Cons}} \tag{1.11}$$

$$C_{GD} = \left.\frac{\partial Q}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} \tag{1.12}$$

C_{DS} lies between drain and source terminals of the device to accommodate the capacitances generated by the two extreme edges of the Schottky barrier depletion; one near to the source and another one near the drain edge along L_g. Under normal biased conditions, C_{DS} and C_{GD} capacitors have smaller values compared to C_{GS}. It is a valid assumption that C_{GD} has almost a constant value in saturation region of operation, but for large signal modeling, it increases inherently depending on bias voltages. Figure 1.9 shows the temperature effect on C_{GS} and C_{GD} of the device. As temperature increases, C_{GS} of the device decreases gradually while, C_{GD} has almost constant value.

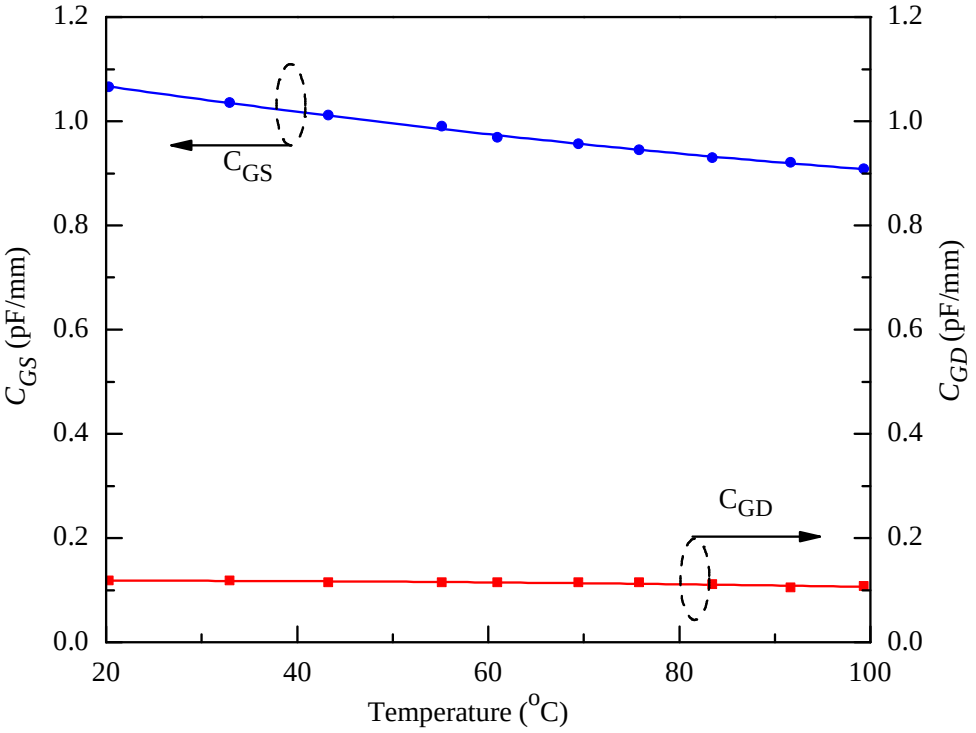

FIGURE 1.9: Temperature dependent variation in C_{GS} and C_{GD} capacitors of a MESFET [28].

1.7.4 Unity Gain Frequency, f_T

A figure of merit, which can fairly be applied to determine the AC performance of a MESFET/HEMT is its unity gain frequency, f_T. The capability of a FET to respond to the variations appeared at its Schottky barrier gate is determined by the charging and discharging of its Miller capacitors. If the τ of the device is smaller than the time needed by the signal to change at the gate, the device will respond and the signal will be translated by the channel current by adopting a new value of I_{DS}. Device f_T would therefore, be that frequency beyond that would not be able to translate the incoming signal into a new value of the channel current. Mathematically, it can be written as:

$$f_T = \frac{G_M}{2\pi(C_{GS} + C_{GD})} = \frac{\upsilon_s}{2\pi L_g} \tag{1.13}$$

Since, charging and discharging is defined by the dielectric relaxation time [30], which is a material dependent property therefore, f_T also depends on the chosen semiconductor. Si MESFET has three times smaller f_T compared to GaAs

MESFET while, SiGe/GaAs based HEMTs has 30% large f_T compared to GaAs MESFETs [31].

1.8 Research Questions

Keeping in view the future requirements of wide bandgap FETs, there is a need **to develop an analytical model, which can predict $I-V$ characteristics of wide bandgap MESFETs; especially those, which exhibit self-heating effects in their output characteristics.** This requires an accurate assessment of charge distribution inside the Schottky barrier depletion layer of the device. For this purpose, the depletion layer can be distributed into four different regions to assess accurate potential distribution inside the channel; leading to the development of an $I-V$ expression for the device output characteristics. Once an $I-V$ expression is established, it can then be extended to incorporate self and ambient heating effects to achieve wider applicability of the model.

In the 2$^{\text{nd}}$ part of the this research, it is aimed **to evaluate Miller capacitors of wide bandgap FETs for their improved AC performance analysis under intense operating conditions.** This is realized because in microwave FETs, $L_g \sim 0.4$ μm, and evaluation of charges inside the depletion layer becomes very challenging. Thus, a technique is needed to assess Miller capacitors with improved accuracy and their temperature dependence variation.

As the performance of wide bandgap FETs is greatly influenced by the substrate chosen for their fabrication it is, therefore, envisaged that as a 3$^{\text{rd}}$ part of this research, **substrate based performance analysis of wide bandgap FETs** should be carried out wherein, a comparison could be made by evaluating small signal equivalent circuit parameters of FETs fabricated on different substrates to observe their substrate dependent performance.

There are numerous models available, which can be employed in CAD, but there is none, which accommodates the device performance under harsh conditions. It

is, therefore, proposed that as a 4^{th} part of this research, a question should be addressed, which states **development of a nonlinear model to assess DC/AC performance reliability of submicron SiC MESFETs for CAD applications**.

1.9 Thesis Contributions

The major contributions of the thesis are given below.

1. In the first part, an analytical model has been developed, which can predict $I - V$ characteristics of wide bandgap MESFETs; especially those, which exhibit self-heating effects in their output characteristics.

2. In the second part, a mathematical model has been developed to evaluate Miller capacitors of wide bandgap FETs for their improved AC performance analysis under intense operating conditions.

3. In the third part, substrate based performance analysis of wide bandgap FETs has been carried out by evaluating small signal parameters of FETs.

4. Finally, as a fourth part of this research, a nonlinear model has been developed to assess DC/AC performance reliability of wide bandgap FETs for CAD related applications.

1.10 Thesis Outline

This chapter presented details pertaining to MESFETs and HEMTs as potential microwave power devices. Fundamental structure of these devices along with their DC and AC characteristics have been discussed. It is presented that 1^{st} and 2^{st} generation FETs deteriorate their performance at high bias and also at high temperatures and therefore, there is a need to have FETs, which can retain, by and large, their characteristics under harsh operating conditions. It is discussed that

wide bandgap FETs are potential candidates for high power and high frequency applications due to their abilities to withstand under intense operating conditions. It is, therefore, important to explore and explain the characteristics of these devices under extreme conditions. The remaining organization of the thesis is appended below:–

Chapter 2 presents a detailed overview of FETs (MESFETs and HEMTs). It is demonstrated that SiC and GaN FETs offer better performance relative to their Si/GaAs counterparts. SiC and GaN FETs have shown better stability and heat conduction at high biased conditions. Different numerical and analytical models reported in literature are critically reviewed. Various novel structures are reviewed to assess enhanced power handling capabilities of FETs along with f_T, f_{max}, G_M, and G_D. RF performance of the device rely upon small signal parameters so, in this respect, different parameters' extraction techniques reported in literature are critically reviewed. A detailed overview related to self-heating and its consequences on FETs characteristics is presented. Short channel and substrate effects on the device performance are also discussed in this chapter.

Chapter 3 gives an improved temperature dependent analytical model for wide bandgap MESFETs output characteristics. The model involves self-heating effects, which is a common phenomenon in FETs meant to handle a relatively large current and exhibit negative conductance in their output characteristics. A comparative analysis of modeled and observed characteristics exhibited a significant improvement in the modeled data.

Chapter 4 presents an analytical model to asses Miller capacitors of FETs. Based on four distinct regions underneath the Schottky barrier gate of the device, analytical expressions are developed to assess Miller capacitors for both linear, as well as, for saturation regions of operation. It is shown that relative to earlier reported models, the proposed technique exhibited a significant improvement in assessing the device Miller capacitors.

Chapter 5 discusses substrate effects on AC performance of wide bandgap FETs. A comparative analysis is established, which demonstrated that both Si and SiC

substrates are equally good, and there is a nominal change in the AC performance of the device by changing the substrate from Si to SiC. Particle swarm optimization technique is used to achieve optimized intrinsic parameters by involving measured S-parameters. It is established that Si substrate, which is considerably cheaper than SiC, could comfortably be employed to fabricate submicron GaN HEMTs.

Chapter 6 presents a nonlinear model to simulate $I - V$ characteristics of submicron SiC FETs. The region where the Schottky barrier gate loses its control on the channel current, because of the high biased, is successfully modeled for better understanding of the device operation. It is shown that the device performance drastically affected when transconductance to output conductance ratio is less than unity. By attaining accurate compliance between the observed and modeled output characteristics, even for those conditions where the channel is behaving erroneously, device AC parameters are extracted to predict the reliability of the device characteristics under intense operating conditions.

Chapter 7 discusses the conclusion drawn from this research and its extension as a future work.

Chapter 2

Literature Review

2.1 Introduction

The three terminal device referred to as metal semiconductor field effect transistor (MEFET) has revolutionized microwave and low noise electronic systems due to its excellent properties. MESFETs are employed in mixers, frequency multipliers and quasi-linear applications, as they have low noise figure (NF), excellent gain, good efficiency and high output power [32]. They are the building blocks for high frequency applications, particularly for monolithic microwave integrated circuits (MMICs).

Electrical performance of a MESFET rely on the material used for its fabrication. Different materials have been used to enhance the performance of a MESFET since its invention. Silicon (Si) is known as a first generation semiconductor material that can operate up to 200 °C [33]. Thus, devices fabricated using Si will deteriorate their performance when subjected to relatively higher temperature. Gallium Arsenide (GaAs) have some superior qualities compared to Si such as high electron saturation velocity, high energy band gap and critical electric field, and is treated as a second generation semiconductor. On the other hand, Silicon Carbide (SiC), a third generation semiconductor, is superior in material properties compared to both Si and GaAs, as it has wide bandgap in the range of ∼2.97 eV - 3.26 eV; high

TABLE 2.1: Electrical parameters of SiC and GaN [35].

Properties	4H-SiC	6H-SiC	3C-SiC	GaN
Band-gap (eV)	3.2	3.0	2.3	3.4
Intrinsic carrier concentration (cm^{-3})	5×10^{-9}	1.6×10^{-5}	1.5×10^{-1}	10^{10}
Hole mobility (cm^2/Vs)	115	90	40	30
Donor ionization energy (MeV)	45	85	40	28.5
Electron mobility (cm^2/Vs)	800	400	750	900

break down (V_{Br}) electric field ~2 MV/cm, which is almost 5 times of GaAs; high thermal conductivity ~4.75 W/cm K, i.e. 7 times of GaAs; low impact ionization and has high electron drift velocity ~2×10^7 cm/s; making it a potential candidate for high power microwave devices [34]. Another example of third generation semiconductor is Gallium Nitride (GaN), which offers electron mobility even better than SiC. A summary of SiC and GaN fundamental properties is listed in Table 2.1.

A small family of crystalline structures are known as polytypes. As SiC is a compound material, and it exists in different structures so, more than 300 polytypes of SiC are present in nature. Different polytypes such as 4H-SiC, 6H-SiC, 8H-SiC, etc. have different electrical properties. Some of polytypes are preferred because of their individual uniqueness, e.g. cubic 3C polytype can be grown on Si and thus, it can be used to fabricate cost effective devices [37]. Table 2.1 shows electrical properties of 4H, 6H and 3C-SiC polytypes. 3C-SiC has larger value of intrinsic carrier concentration. 4H-SiC has got more attention due to its attractive characteristics such as high electron and hole mobility compared to other polytypes. Also, energy bandgap of 4H-SiC is relatively high. Owing to these facts, 4H-SiC based devices are widely used in communication systems, cellular base stations, RADAR systems and high definition televisions (HDTVs), etc.

Wide bandgap MESFETs fabricated using SiC and GaN are capable of handling high power at microwave frequencies. Apart from high power applications, they

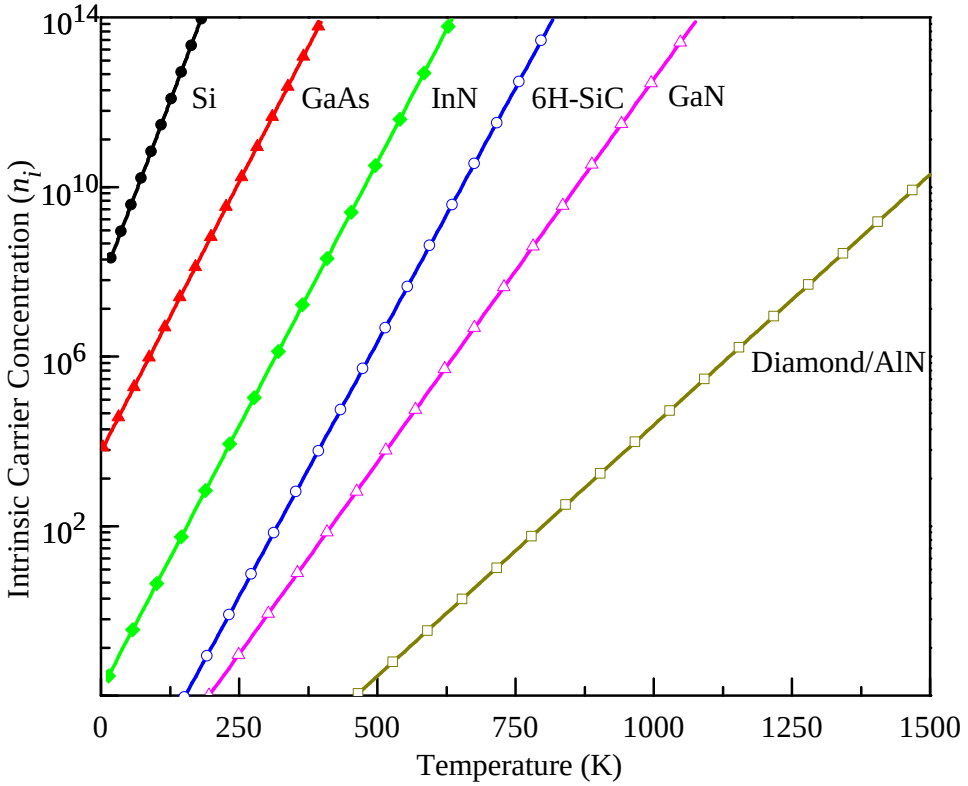

FIGURE 2.1: Intrinsic carrier concentration of different semiconductor materials as a function of temperature [36].

are potential candidates to be used in high temperature environments. These devices can comfortably handle ∼150 W power in mm-wavelength regime. Their operation is similar to that of GaAs MESFETs however; their performance, as power devices, is much superior compared to GaAs based devices [38]. The superior electrical characteristics offered by SiC and GaN MESFETs are primarily associated with the materials properties such as: high thermal conductivity; radiation hardness and immunity to hot carrier degradation [7]. Figure 2.1 shows intrinsic carrier concentration (n_i) of different semiconductor materials as a function of temperature [36]. A material releasing relatively less n_i with increasing temperature would mean that devices made by such materials would be more thermally stable.

For high power communication systems, microelectronic devices such as SiC and GaN MESFETs are highly suitable, as they have the ability to handle both high power and high frequency simultaneously [7]. SiC and GaN MESFETs can operate

comfortably up to a temperature of 500 °C [39] by maintaining their electrical performance, which made these devices a natural choice for electronic circuitries to be used in harsh environments. Also, due to higher V_B, SiC and GaN MESFETs have large power density than Si and GaAs that made them attractive for ultra high speed microwave circuitries [38].

A natural extension in third generation semiconductor FETs is SiC and GaN based high electron mobility transistors (HEMTs). Wide bandgap HEMTs have got a sizeable share in microelectronics high power industry. These devices are offering better gain and low *NF* compared to MESFTEs but, of course on the expense of sophisticated wafer and fabrication technology.

In this chapter, a review has been presented of wide bandgap FETs, which includes MESFETs and HEMTs. In the first part, a chronological growth of wide bandgap MESFETs is presented followed by wide bandgap HEMTs, and their potential use in microwave industry. The performance of high power devices is highly effected by self and ambient heating, and also by substrate properties. Therefore, a review in this respect is also presented to know the performance of these devices as a function of temperature and the quality of the substrate. To exploit the full potential of such devices, it is important to know relevant mathematical models, which can describe DC and AC performance of these devices both from their geometry and material perspectives. The chapter therefore, also gives a comprehensive review of various empirical and analytical models, which are developed so far to describe the electrical performance of wide bandgap FETs.

2.2 Wide Bandgap MESFETs

Keeping in view the needs of high temperature and harsh environment electronic circuitries, wide bandgap MESFET was introduced by Muench et al. in 1977 [40]. As discussed in the introductory section of this chapter that Si based devices failed to perform as per their electrical specifications beyond 200 °C therefore, there was a natural need to have the devices, which can function at high temperatures ambient

such as engine, mines, and power systems, etc. Wide bandgap semiconductors (SiC and GaN) can fulfill such needs because of their abilities to maintain their electrical properties at elevated temperatures caused by the device self-heating as well as by the external environment.

SiC and GaN MESFETs gained a significant attention both in microwave, as well as in power electronics, due to their abilities to operate simultaneously at high frequency and at high bias. Table 2.2 summarizes wide band MESFET's development history so far. In 1977, Muench et al. [40] fabricated first Schottky barrier MESFET from SiC. Their fabricated device exhibited G_M = 1.75 mS/mm. As obvious from the G_M value, the device response was fairly poor however, improvements in the MESFET design and quality of wafer have occurred periodically, which led to enhanced G_M values.

In 1984, Scott et al. [41] fabricated dual gate MESFETs and derived the expressions for both RF and $I-V$ characteristics. They extracted device parameters by using three port network and reported G_M = 24.3 mS. Aksun et al. [42] fabricated MESFETs of quarter micron L_g grown on Si substrate. Extrinsic G_M = 360 mS/mm was observed by measured S-parameters up to 20 GHz with f_T = 55 GHz and NF = 2.8 dB. Kelner et al. [43] evaluated $I-V$ characteristics of SiC MESFET structure grown on p-type Si substrate. They observed G_M = 2.3 mS/mm with L_g = 5 μm.

Asif et al. [44] fabricated MESFETs having L_g = 4 μm using single crystal GaN channel layer, which was deposited on a sapphire substrate. Drain/source ohmic contacts and Schottky barrier gate were fabricated using silver electrodes and TiAu metals, respectively. Their fabricated devices exhibited G_M as high as 23 mS/mm at V_G = -1 V.

In 1995, Weitzel [6] presented a comparative analysis of power densities for GaAs, Si and 4H-SiC MESFETs. It was reported that for low voltage applications, GaAs MESFETs offered high power densities due to their high electron mobilities and low channel resistances. On the other hand, 4H-SiC MESFETs have high absolute power densities for high voltage applications because of their higher V_B

compared to Si and GaAs. Allen et al. [45] presented SiC MESFETs analysis for RF applications for devices having different L_g. It was reported that for L_g = 0.45 μm, the device offered f_T = 22 GHz and f_{max} = 50 GHz with PAE of 54% at 2.1 GHz. Clarke et al. [46] investigated high power properties of 4H-SiC MESFETs. They observed a power density, PD = 5.6 W/mm with 36% PAE for S-band applications.

Henry et al. [47] fabricated SiC MESFETs of 48 mm gate periphery using buried channel structures. The buried channel structure was formed by using undoped spacer layer on top of the SiC MESFET. From this approach, they observed minimum RF dispersion and uniform G_M with P_{out} = 4.4 W/mm, PAE = 62%, and a power gain of 10.6 dB at 3 GHz. For continuous wave applications, they observed P_{out} = 2 W/mm, PAE = 40%, and 7 dB associated gain. Rorsman et al. [48] in 2004 investigated scalability of 4H-SiC MESFETs for high frequency applications. Different L_g devices with different gate structures were processed on a thin highly doped p-buffer layer. From this process, they observed an improvement in output conductance, G_D and a reduction in short channel effects. Also, 20% and 25% improvement in extrinsic f_T and f_{max} was observed, respectively, with 12% increase in PD.

In 2006, Andersson et al. [19] fabricated SiC MESFETs using field-plated technique combined with a buried-gate. A relatively higher V_B and lower G_D were observed. Furthermore, their fabricated MESFETs offered PAE = 70% and PD = 7.8 W/mm at 3 GHz. Gang et al. [49] presented DC and RF characteristics of 4H-SiC MESFETs fabricated on high purity semi-insulating (SI) substrates. They observed PD = 7.8 W/mm, gain of 11.9 dB and PAE = 48% at 2 GHz for continuous wave applications.

In 2013, Chuan et al. [50] fabricated high power SiC MESFETs using p-buffer layer and multi-recessed gate for S-band applications. Their fabricated MESFETs demonstrated pulsed wave output power of 94 W, a linear gain of 11.7 dB and 24.3% PAE at 3.4 GHz. On the other hand, for continuous wave applications,

TABLE 2.2: Development history of wide bandgap MESFETs .

Author	Year	Development	Ref.
Muench et al.	1977	First wide bandgap MESFET fabricated using SiC.	[40]
Scott et al.	1984	Wide band MESFET's model using dual gate.	[41]
Aksun et al.	1986	Quater micron MESFETs with G_M = 360 mS/mm, f_T = 55 GHz and NF = 2.8 dB.	[42]
Kelner et al.	1987	SiC MESFETs structure using p-type Si substrate with G_M = 2.3 mS/mm	[43]
Asif et al.	1993	GaN MESFETs having L_g = 4 μm and W = 100 μm with G_M = 23 mS/mm, V_B = 120 V and υ_s = 5×10^6 cm/s.	[44]
Weitzel et al.	1995	SiC MESFETs with G_M, f_{max}, f_T, PD, and PAE of 42 mS/mm, 12.9 GHz, 6.7 GHz, 2.8 W/mm and 12.7%, respectively.	[6]
Allen et al.	1997	SiC MESFETs having L_g = 0.45 μm for high power S-band applications with f_T = 22 GHz and f_{max} = 50 GHz.	[45]
Clarke et al.	2002	Development of 4H-SiC MESFETs for S-band applications with PD = 5.6 W/mm and PAE = 36%.	[46]
Henry et al.	2004	SiC power MESFETs for S-band operations with 20 W output power, PD = 4.4 W/mm, and PAE = 60%.	[47]
Rorsman et al.	2004	Effects of L_g on f_T, f_{max} and PD.	[48]
Andersson et al.	2006	MESFETs fabrication using field plated buried-channel with PD = 7.8 W/mm and PAE = 70%.	[19]
Gang et al.	2010	MESFETs fabrication using home-grown epi structures with PD = 7.8 W/mm and PAE = 40%.	[49]
Chuan et al.	2013	Dual p-buffer layer and multi-recessed gate MESFET.	[50]
Jia et al.	2015	MESFET fabrication using multi-recessed source/drain drift regions.	[51]

their fabricated transistors offered output power greater than 4.7 W/mm, which confirmed their potential use for high power solid state amplifiers.

Jia et al. [51] presented an improved structure of 4H-SiC MESFETs with multi-recessed source/drain drift regions. The presented process was utilized to improve V_B, and capacitance characteristics of SiC MESFETs; to obtain better power RF characteristics. Simulation results showed 19% increase in PD compared to single-recessed SiC MESFETs. The presented design also improved f_T and f_{max} having values 17 GHz and 68 GHz, respectively.

2.3 Wide Bandgap HEMTs

Development in wide bandgap FETs technology was phenomenal in 1990s, and it was witnessed simultaneously both in MESFETs as well as in HEMTs. A MESFET is a relatively cheaper device, because it requires a simple wafer for its fabrication compared to a HEMT wafer. However, wide bandgap HEMTs offer excellent microwave characteristics and they are far superior when compared with wide bandgap MESFETs [52]. Resultantly, along with the wide bandgap MESFETs, there was a growth side by side in wide bandgap HEMTs and currently, wide bandgap HEMTs are frequently employed in microwave power circuitries. Efforts made so far in wide bandgap HEMT's development are summarized in Table 2.3.

In 1994, Asif et al. [53] fabricated a 0.25 μm gate length AIGaN/GaN HEMT with nominal G_D and a relatively high G_M. This was a first wide bandgap semiconductor based HEMT with superior RF characteristics. They observed $G_M = 27$ mS/mm, $f_T = 11$ GHz and $f_{max} = 35$ GHz at room temperature. Gaska et al. [54] described characteristics of AlGaN/GaN HEMTs grown on 6H-SiC and sapphire substrates. They demonstrated that SiC HEMTs have better electron transport properties compared to sapphire based HEMTs, especially, for high power applications.

TABLE 2.3: Development history of wide bandgap HEMTs.

Author	Year	Development	Ref.
Asif et al.	1994	First AIGaN/GaN HEMT fabrication.	[53]
Gaska et al.	1998	Self-heating effects in AlGaN/GaN HEMTs.	[54]
kuzmik	2001	InAlN/(In)GaN quantum well HEMT structure with 205% increased power capabilities.	[55]
Arulkumaran et al.	2002	Effects of substrates and temperature on G_M of the device.	[56]
Liu et al.	2005	Temperature dependent NF with post gate annealing.	[57]
Micovic et al.	2006	P_{out} = 2.1 W/m with power gain of 17.5 dB at 80.5 GHz.	[58]
Donoval et al.	2008	Performance comparison of MOS-HEMT and HEMT.	[59]
Thorsell et al.	2011	Electro-thermal model valid up to 100 kV/cm, for high temperature and bias.	[60]
Sadi et al.	2013	$C-V$ and $I-V$ characteristics of HEMTs and LD-MOSFETs with inter-modulation effects.	[61]
Iacopi et al.	2015	Wide bandgap devices for high power and temperature.	[62]
Aliakbari et al.	2015	Based on active transmission line theory, multi-finger p-HEMTs time domain modeling.	[63]

Kuzmík [55] compared physical parameters of a novel structure InAlN/(In)GaN quantum well HEMT to the conventional approach and found three times larger polarization induced charge which contributed in defining 2-DEG. He observed I_D = 3.3 A/mm and G_M = 300 mS/mm, i.e. 205% increased power capabilities, which can be considered a record power performance with the proposed structure. Arulkumaran et al. [56] examined $I-V$ characteristics of HEMTs grown on sapphire and SI-SiC substrates for the temperature range of 25 °C to 500 °C. They demonstrated that both, sapphire and SI-SiC HEMTs have similar $I-V$ characteristics at 300 °C but, SI-SiC HEMTs have better performance at 500 °C.

Effects of post gate annealing (PGA) on the $I-V$ characteristics of AIGaN/GaN HEMTs were reported by Liu et al. [57]. They observed a significant decrease in the device gate leakage current, f_T and f_{max} at high temperature. On the other hand, annealed devices performed superiorly with $NF_{\min} = 3.94$ dB, and gain = 7.02 dB in harsh environment.

Micovic et al. [58] fabricated MMIC for high frequency applications using GaN HEMTs. Compared to InP and GaAs HEMTs, 8 times higher P_D in W-band established the superiority of the proposed design. Donoval et al. [59] reported static and transfer characteristics of AlGaN/GaN HEMTs and Al_2O_3/AlGaN/GaN MOS-HEMTs up to 425 °C. At higher temperature, these devices exhibited a 30% improvement in their $I_{\mathrm{D(sat)}}$ and G_M. Thorsell et al. [60] discussed thermal effects of HEMT device for high bias and temperature. Sadi et al. [61] proposed an empirical nonlinear model of IIIV HEMTs incorporating intermodulation distortion. Iacopi et al. [62] developed temperature dependent model of wide bandgap devices for high power applications. Based on active transmission line theory, Aliakbari et al. [63] modeled multi-finger p-HEMTs and found good results for high frequency analysis.

2.4 Self-Heating Effects

As compared to other semiconductor materials, SiC is a wide bandgap semiconductor with good thermal conduction properties and thus, it is a preferred choice for harsh environment applications [39]. But at the same time, SiC FET's temperature rises inherently at increased V_{DS}, which causes self-heating of the device. Thus, self-heating effects occur due to high operating current and voltages, which directly effects electron mobility, causing degradation in DC and RF performance of the device [64]. Also, power dissipation, which is related to the thermal resistance, is effected by the self-heating and hence, the power handling capabilities of the device [65]. Thus, one can say that both dynamic and static properties of the device are dependent on ambient temperature self-heating.

TABLE 2.4: Effects of self-heating on FETs characteristics.

Author	Year	Development	Ref.
Anholt	1995	Change in device static and dynamic properties due to self-heating effects.	[66]
Royet et al.	2000	Negative differential G_M found at low frequencies.	[67]
Villard et al.	2003	Thermal limitation mechanisms for both DC and RF performance in MESFETs .	[68]
Islam et al.	2004	Physics based model for GaN MESFETs incorporating thermal and trapping effects.	[69]
Yuk et al.	2008	Temperature dependent $I-V$ characteristics with third order intermodulation distortion.	[70]
Hongliang et al.	2009	Self-heating and trapping effects for both positive and negative frequency dispersions.	[71]
Wen et al.	2017	Electro-thermal model for GaN HEMTs, self-heating effects expressed in term of E_c as a function of T and V_G.	[72]

Anholt [66] showed that for better performance of the device, self-heating effects must be taken in to account. Yuk et al. [70] presented self-heating and temperature dependent large signal model of MESFETs. They predicted S-parameters, small-signal parameters, as well as reflected input/output power with third order intermodulation distortion. Royet et al. [67] demonstrated that self-heating effects lead to temperature increment and power dissipation in the device. They showed that at low frequencies, self-heating caused negative differential G_M in the $I-V$ characteristics. By using temperature dependent trapping and transport properties, Islam et al. [69] reported that trapping and self-heating both effect RF performance of GaN MESFETs. They reported that significant change occurred in the device P_D, gain and PAE due to self-heating effects. Villard et al. [68] observed thermal limitation mechanisms for both DC and AC performance in MESFETs.

Output power of the device is effected by trapping and self-heating effects. Device

simulation, under these circumstances, becomes more crucial and complicated. Temperature dependent models with electron mobility at low and high fields are essential to solve this problem. Hongliang et al. [71] reported a comprehensive model describing self-heating and trapping effects for 4H-SiC MESFETs. They simulated effects of some trapping parameters, i.e. time constant and trapping concentration on G_M of the device for both positive and negative frequency dispersions. Wen et al.[72] reported self-heating effects of GaN HEMT as a function of temperature and gate bias. Table 2.4 presents a summary of self-heating effects on FETs electrical performance.

2.5 Short Channel and Substrate Effects

MESFET devices can be categorized into two parts

i) short channel devices, and

ii) long channel devices.

Devices with $L_g < 1$ μm (submicron) are usually called short channel or microwave devices whereas, devices having $L_g > 1$ μm are called long channel or low frequency devices [73]. In short channel devices, current saturates by increasing V_{DS}, and this happens due to the velocity saturation of carriers present in the channel, while in long channel devices, the current saturation is caused by the channel pinch-off [30].

In 1979, Wada et al. [74] numerically analyzed MESFET devices of three different materials; Si, GaAs and InP. In their work, they described thoroughly the effects of electric field on the electron drift velocity, Schottky barrier height underneath the gate and substrate conduction. They observed that pinch-off channel has small effect on short gate devices due to the substrate conduction and gate-to-source capacitance, C_{GS} of the device.

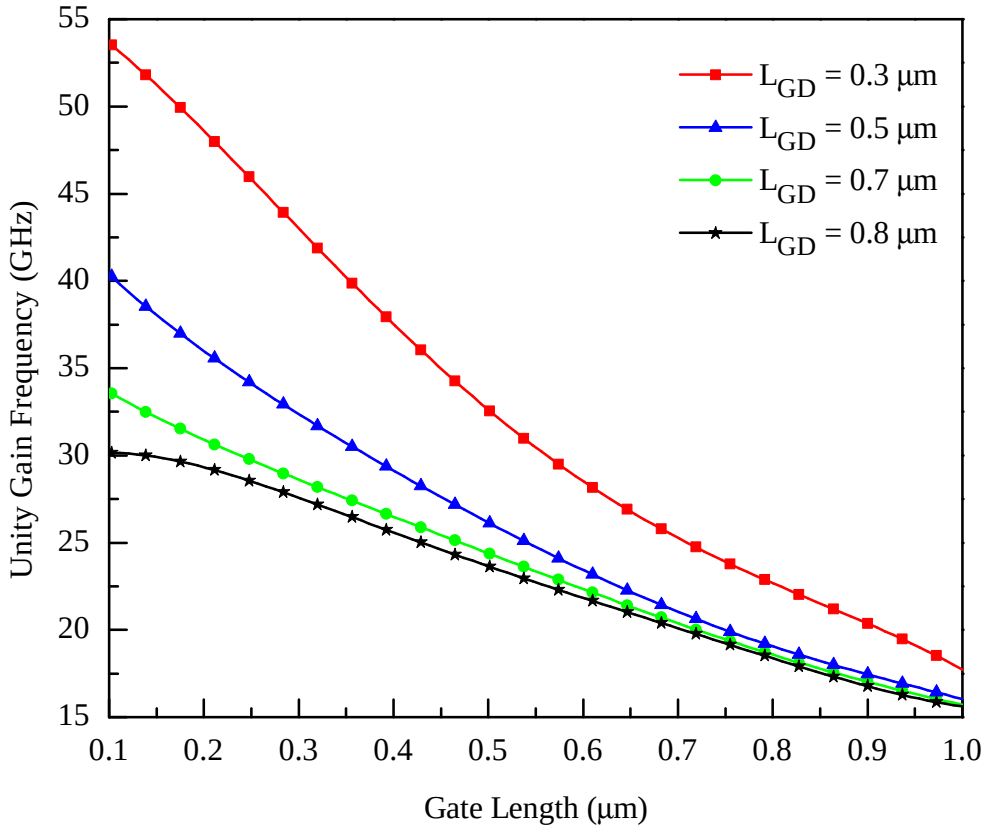

FIGURE 2.2: Unity gain frequency versus gate length for four different gate-to-drain spacing [75].

In MESFETs, RF performance depends on device material, L_g and electric field in the channel. Although f_T is inversely proportional to L_g, RF performance of the device cannot be enhanced by simply reducing L_g, as saturation occurs in f_T for $L_g < 1$ μm [27]. Additionally, reduction in L_g causes short channel effects, which deteriorates the device performance [76]. Honda et al. [77] showed that the RF performance of the device degrades due to the short channel effects. Figure 2.2 shows the behavior of f_T as a function of L_g and gate-to-drain length, L_{GD} [75]. The plot shows that f_T increases as L_{GD} decreases, and for short L_g, maximum f_T is observed.

In short channel devices, Schottky barrier depletion layer gets modified and the resultant electric field inside the channel effects carrier mobility, device leakage and charge accumulation in the channel [31]. Drain induced barrier lowering (DIBL) is also an important parameter of short channel effects. As the drain voltages of the

TABLE 2.5: Short channel and substrate effects on FETs characteristics.

Author	Year	Development	Ref.
Wada et al.	1979	Pinch-off channel has small effect on short gate devices.	[74]
Huang et al.	2000	For small L_g, maximum f_T is observed.	[75]
Arai et al.	2003	RF performance cannot be enhanced by simply reducing L_g.	[76]
Yang et al.	2005	p-buffer layer effects on DC and RF performance of MESFETs.	[78]
Na et al.	2005	Substrate effects with $G_M = 41$ mS/mm, $f_T = 9.3$ GHz, $f_{max} = 34$ GHz, PD = 1.5 W/mm and PAE = 14.6%.	[79]
Hjelmgren et al.	2007	DC and RF performance of MESFETs with high purity semi-insulating substrate.	[80]
Yim et al.	2011	RF performance degrades due to short channel effects.	[81]

device increases in the saturation region, Schottky barrier height of the channel decreases, and this decreases the effect of V_{GS} on the device.

Problem of current instability in 4H-SiC MESFETs occurs due to the trapping of electrons in the substrate [82]. A conducting p-layer between channel and substrate can reduce this problem and improve the performance of the device. In 2005, Aggarwal et al. [34] proposed a model for buried p-layer 4H-SiC MESFETs. They showed that $C-V$ characteristics and f_T of the device are effected by p-layer. Yang et al. [78] studied p-buffer layer effects on $I-V$ and RF characteristics. Trapping effects in the channel and in the buffer layer were also investigated.

Na et al. [79] fabricated 4H-SiC planar MESFETs by using ion implantation and showed good DC and RF performance of tier fabricated devices. They observed $G_M = 41$ mS/mm, $I_{\mathrm{DS(sat)}} = 500$ mA/mm at $V_{DS} = 40$ V of the devices having $L_g = 0.5$ μm and gate width, $W = 100$ μm. RF characteristics with $f_T = 9.3$ GHz, $f_{max} = 34$ GHz, PD = 1.5 W/mm and PAE = 14.6% at 2 GHz were also

obtained. In [80], the authors investigated DC and RF characteristics of 4H-SiC MESFETs with high purity SI substrate. Their study was based on TCAD, focusing on thermal heat, substrate trapping effects and electron transport of the device. Yim et al. [81] proposed a model incorporating short channel effects and observed performance degradation. In nut shell short channel effects are important for accurate assessment of device characteristics and cannot be overloaded while designing a microwave MESFET/HEMT. Table 2.5 summarizes short channel and substrate effects on FETs characteristics.

2.6 Modeling Techniques

An expression that can generate the response of a system, process or a device is known as a mathematical model. There is a strong relationship between parameter extraction techniques, device measurements and the device mathematical model [83]. The validity of a model depends on its parameters, features, form and also the accuracy of the technique, which is employed in the development of the model [84]. Accurate and exact device characterization are required for reliable determination of the device parameters. Generally, device models are categorized on the basis of employed techniques and these techniques are known as:

i) physical modeling technique, and

ii) numerical modeling technique.

In a physical model, device physical parameters are employed, e.g. channel height, a, W, L_g and channel doping, N_D, etc. These parameters are linked with each other by involving device physics and expressions, referred to as closed form expressions. Compared to numerical model, these parameters are more logical to handle and device characteristics can be predicted appropriately by using these physical parameters; when compared with bias potential, therefore, physical models are preferred for the better understanding of the device.

A numerical modeling of a FET concerns with carrier's motion inside the channel as a function of applied bias. Since, electric field distribution inside the channel is not uniform; therefore, it is quite difficult to assess its effect on the motion of carriers that ultimately limits channel current. In addition, it is quite complex for a design engineer to tackle the parameters of the device, which directly effects the field inside the channel. Therefore, numerical techniques, usually give device response by involving expressions, which can generate the device characteristics by engaging the device physical and bias parameters. Such an expression may not be arrived at using physics of the device.

Numerous researchers have developed models for FET's characterization. Some models are based on the device behavior and are used quite often to predict FET's characteristics, while, others employ numerical techniques to generate the behavior of the device. The detail of this development is elaborated in the following sections.

2.6.1 MESFET Models

A number of models elaborating $I - V$ characteristics of MESFETs have been developed by the researchers working in the field. In 1969, Grebene et al. [85] developed a general theory to describe the pinch-off operation for the gate junction of a FET. On the basis of device structure, they described the current conduction over a wide range of operation. Also, by incorporating Poisson's equation, they developed an expression for potential distribution inside the channel with the consideration of carrier drift velocity under a relatively high electric field.

Shur et al. in 1978 [86] presented an analytical model for GaAs MESFETs. They assumed that the pinch-off condition under the gate is not responsible for the saturation current, as it is a function of Gunn effect [87] near the drain side. By using two-dimensional computer analysis and experimental data on a $L_g = 1$ μm device, they calculated saturation current, G_M and total charge under the gate. They also performed small signal analysis of the device by calculating transit delay, τ, f_T and intrinsic capacitances of the device.

In 1978, Willing et al. [88] presented a method to predict large signal, as well as small signal parameters of GaAs MESFETs. Using the device geometry and material parameters, they derived analytical expressions for both DC and RF characteristics, and validated it for different devices. They measured the active channel properties by considering the device parasitic resistances and derived expressions for maximum output power and minimum NF from DC characteristics of the device.

In 1979, Fukui et al. [89] presented a detailed method to assess device physical DC characteristics of MESFETs. They derived simple analytical expressions by using material and geometrical parameters of the device, and calculated L_g, a and N_D, etc. A wide range of devices, e.g. 11 MESFETs were used to demonstrate their theory, and a good agreement with the experimental data was demonstrated. Five devices were used for high power applications, while, the remaining were used for low noise applications. They claimed that maximum output power and minimum NF can be predicted by using DC parameters. They also derived the expressions for parasitic resistances and G_M of the device.

In 1989, Chang et al. [90] solved 2-D Poisson's equation for potential and electric field distribution in the saturation region of an operating MESFET. By using Chang-Fetteman equation, they estimated $I-V$ characteristics, electron saturation velocity, υ_s. electric field, hot electron energy, and V_B. The beauty of the developed technique was that it can be employed to variety of FETs involving different materials.

Effect of field dependent mobility on the performance of a SiC FET was presented by Tsap [91]. He developed an analytical two region model for saturated electron drift velocity in the presence of strong electric field and calculated f_T and output power of the device. He showed that f_T of the device is directly affected by the field mobility, which is dependent on L_g and it reduces more than 1.5 times by increasing $L_g = 0.9$ to 1.5 μm.

Huang et al. [92] developed a 2-D simulator by using Scharfetter-Gummel-type discretization method for 4H-SiC MESFET. They predicted different parameters

TABLE 2.6: Historical perspective of MESFET's mathematical models.

Author	Year	Development	Ref.
Grebene et al.	1969	Potential distribution using current conduction mechanism, presence of finite drain resistance.	[85]
Shur et al.	1978	I_{sat}, G_M, G_D, f_T, Q, C_{GD}, C_{GS}, τ and V_B are calculated for 2-D CAD simulations.	[86]
Willing et al.	1978	RF and DC analysis, Harmonic power level with 6 dB gain compression.	[88]
Fukui et al.	1979	Basic channel parameters are determined from DC characteristics, NF and P_D also predicted from the DC parameters.	[89]
Chang et al.	1989	Field and potential distribution analysis for saturation region by using 2-D Poisson equation.	[90]
Tsap	1995	Nonlinear dependence of υ_s on E, channel parameters effects on f_T and P_D.	[91]
Huang et al.	1998	2-D simulator for 4H-SiC MESFET developed, impact ionization effect on high V_B.	[92]
Mnatsakanov et al.	2002	Low field mobility model for 4H, 6H and 3C SiC MESFETs by considering temperature and doping concentration.	[93]
Mukherjee et al.	2003	Analytical model with trapping and substrate effects.	[94]
Garcia et al.	2011	13 parameters model to predict $I-V$ expressions for large V_{DS}.	[95]
Khemissi et al.	2012	2-D physics based model for linear, non-linear and saturated regime of MESFETs.	[96]
Rao et al.	2015	An improved $I-V$ model, incorporates thermal and substrate effects.	[97]
Ahmed et al.	2017	Evaluation of potential distribution inside the channel for SiC MESFETs.	[98]
Li et al.	2018	Based on metal-semiconductor interface state of the Schottky junction developed GaN MESFET model for static performance.	[99]

of the device, i.e. threshold voltage, V_T; mobility, μ; Schottky barrier hight, ϕ_b and υ_s, etc.

Mnatsakanov et al. [93] proposed temperature and concentration dependent mobility model for SiC polytypes. They derived analytical expressions and tested them on 4H, 6H and 3C polytypes MESFETs over a wide range of temperature and doping concentration. Mukherjee et al. [94] reported a physics based model for SiC MESFET. In their study, they focused on trapping and self-heating effects of the device performance. Additionally, surface and buffer layer dependent performance were also investigated and results showed that thicker buffer layer reduces the trapping based degradation significantly.

In 2012, Khemissi et al. [96] proposed a 2-D model for $I-V$ characteristics of MESFETs. Output current expression was found for three regions of operation (linear, saturation and breakdown) at different bias by incorporating field dependent mobility and channel distribution underneath the gate. Their results showed that the developed model was useful for power and pre-amplifier devices. Rao et al. [97] developed an improved $I-V$ model for SiC MESFETs by incorporating substrate and thermal effects of the device and observed current degradation. Ahmed et al. [98] reported an $I-V$ model for submicron SiC MESFETs by evaluating channel potential using Poisson's equation with appropriate boundary conditions. They observed that finite G_D in the saturation region of operation is caused by the Schottky barrier depletion layer modification.

2.6.2 HEMT Models

In the last decade, GaN-based HEMTs have received a great attention as an active device for high frequency power electronics [73, 100]. High V_B and low intrinsic carrier generation at high temperature made GaN-based HEMTs suitable for high power and high temperature systems. GaN HEMTs offer a relatively large value of μ due to two-dimensional electron gas (2-DEG) transport mechanism, which is formed by the heterojunction of two distinct semiconductors; a prerequisite for

a HEMT. In an HEMT channel, charges are confined in a 2-D space instead of 3-D as is the case in MESFET. This fundamental difference is the reason that a MESFET model cannot be used to predict the characteristics of a HEMT and the device requires all together a different approach to model its characteristics. A number of analytical models have been presented in literature to predict the performance of an HEMT.

In 1987, Loret et al. [101] presented a 2-D numerical model for HEMTs. Poisson's and macroscopic transport equations were used to model simulation and their results were compared with the experimental data. Chang et al. [102] developed an analytical model for DC and RF characteristics of HEMTs. Gaussian Standing Wave (GSW) [103] was used to simulate electron drift velocity behavior as a function of electric field for DC characteristics. 2-D Poisson's equation was used to find the behavior of the channel under saturation condition and the effect of parasitic resistance of donor layer on channel current was also investigated. Furthermore, small signal parameters such as G_M, gate capacitance, C_G and channel conductance, etc. were also derived for microwave performance.

In 1989, Shey et al. [104] presented an analytical model based on non linear charge control formulation for HEMTs. They developed simple analytical expressions for device DC characteristics and compared the device characteristics with the measured data. Angelov et al. [105] proposed a nonlinear model to simulate frequency dispersion, heat and breakdown effects for HEMTs and MESFETs. To validate their theory, DC characteristics, frequency dispersion, and S-parameters measurements were carried out over a wide range of commercial HEMTs and compared with the experimental data. Lai et al. [106] proposed a model of 50 nm InP-HEMT with $f_{max} > 1$ THz.

A large signal model describing the effects of self-heating and charge trapping for GaN HEMTs was presented by Yuk et al. [107]. They used the expression of drain current to find G_M of the device and by using G_M, output power, gain and PAE of 13.09 W, 10 dB and 38%, respectively were calculated. To validate the RF characteristics predicted by their model, they used ADS software to predict

TABLE 2.7: HEMT analytical models.

Author	Year	Development	Ref.
Loret et al.	1987	2-D numerical model based on Poisson's and macroscopic transport equations.	[101]
Chang et al.	1987	Field and potential distribution analysis by using Gaussian Standing Wave (GSW).	[102]
Shey et al.	1989	Non-linear charge control formulation for HEMTs.	[104]
Angelov et al.	1996	A nonlinear model to simulate frequency dispersion, heat and breakdown effects for HEMTs.	[105]
Lai et al.	2007	50 nm InP-HEMT with $f_{max} > 1$ THz.	[106]
Yuk et al.	2009	Large signal model with PD = 13.09 W and PAE = 38%.	[107]
Long et al.	2012	Performance analysis of GaN HEMT and GaAs *p*-HEMT at 4 GHz.	[109]
Sahoo et al.	2016	Small signal modeling for AlN/GaN/AlGaN HEMT using both Si and SiC substrates.	[110]

S-parameters in the frequency range of 0.2-10 GHz and compared the results with those obtained from their expressions. A good degree of agreement between modeled and simulated results showed the validity of their model. Liu et al. [108] proposed models for self-heating, charge conversion and frequency behavior of III-V FETs. *p*-HEMT devices having 4×75 μm^2 and 2×100 μm^2 dimensions were used to verify the validity of their proposed model. Measured S-parameters from 100 MHz to 3 GHz at 25 °C were also compared with the modeled data, and small signal parameters were calculated and compared with Angelov model.

Long et al. [109] investigated GaAs *p*-HEMT and GaN HEMT devices for DC and RF applications. They extracted intrinsic device parameters by using Taylor series expansion of Y-parameters. For large signal modeling, non-quasi-static charge control was used to formulate device current expressions. They tested their model on two devices: 4×70 μm^2 GaN HEMT with input power of 9 dBm and 4×75 μm^2 GaAs *p*-HEMT with the same input power at 4 GHz. They observed that the model predicted the characteristics of GaN HEMT with better accuracy than

GaAs p-HEMT.

Sahoo et al. [110] proposed a small signal model for AlN/GaN/AlGaN HEMT using both Si and SiC substrates. They described that SiC is more suitable and has better performance for GaN HEMTs compared to Si. A summary of model development history of HEMT, discussed in the preceding paragraphs, is presented in Table 2.7.

2.6.3 Nonlinear Compact Models

Nonlinear compact models are used to predict the device characteristics without involving in detail the inner workings of the device. Such models are suitable to be employed in Computer Aided Design (CAD), where the internal conditions of the device are ignored and the only focus is on the output characteristics and their dependence on the device geometry and bias. Thus, nonlinear models allow a design engineer to analyze the effect of the device dimensions and material on the output characteristics before its fabrication. There are numerous nonlinear models available in literature which can simulate $I-V$ characteristics of MESFETs [70, 111–120].

In 1978, Willing et al. [88] presented a method to predict the nonlinear behavior of GaAs MESFETs. They also calculated small signal parameters, e.g. active channel resistance, feedback capacitance, output resistance and G_M. Taki [121] proposed an empirical model to analyze the nonlinear behavior of FETs. Irrespective of material and device parameters, his $I-V$ expression was valid for both pinch-off and saturation regions. Kacprzak et al. [122] presented a compact FET model for large signal measurements. They derived a modified four parameters based $I-V$ expression from Taki hyperbolic tangent function [121], which was valid for any size of FETs. The presented model was derived mathematically with little physical justification.

Curtice et al. [119] developed a nonlinear model for large signal as well as for RF applications. On the basis of harmonic balance technique, they analyzed the

device behavior in both time and frequency domain. Tellez [123] also developed a five parameter nonlinear MESFET model, which was based on Curtice model [124]. He compared the results with Schichman-Hodges model [125] and found 16% improvement for low current operation of MESFET.

Statz [118] also developed an $I-V$ expression for FETs, which was suitable for SPICE simulations. Total gate charge was calculated leading to C_{GS} and C_{GD} assessment at given V_{DS} and V_{GS}. Ahmed [126] also reported a model wherein he introduced effects of a on the device performance. By employing his previous work [127], he developed an algorithm to simulate I_{DS}, G_M and G_D of submicron MESFETs. He showed that with the increase in a, G_D increases, while G_M decreases, and the performance could be enhanced keeping $a < L_g$. Islam et al. [128] extended the work of Ahmed et al. [17] and presented a seven parameter nonlinear model for submicron MESFETs. They compared their model with Ahmed model, by using mean square error (MSE) and reported improved results.

In [78], the authors developed a compact model for 4H-SiC MESFETs that showed the effects of p-buffer layer and doping on pinch-off voltage and G_D. DC characteristics were compared with the experimental data by incorporating pinch-off voltage and G_D simulations. Memon et al. [129] also presented a nonlinear model and compared their work with other models reported in literature. Their work was based on Ahmed model [130], and has the ability to simulate the nonideal Shockley response of the device. For high saturation and pinch-off voltage of 4H-SiC MESFETs, Quanjun et al. [111] presented a compact model and compared it with other similiar models. Their model was useful for MMICs and RF circuits, and can be employed in CAD simulations.

Riaz et al. [26] presented an improved model for SiC MESFETs, especially for microwave power applications. They accommodated nonideal Schottky behavior of the device as a function of device bias, and applied their model, using Particle Swarm Optimization (PSO) technique on devices having different L_g. They demonstrated 24% improved accuracy even for the devices, which exhibit second

order effects in their $I-V$ characteristics. Table 2.8 gives $I-V$ expressions for various nonlinear models, which are routinely employed to predict DC characteristics of Schottky barrier.

TABLE 2.8: $I_{DS}(V_{GS},V_{DS})$ expressions of various nonlinear MESFETs models.

Model	Equations	Ref.
Quanjun	$I_{DS} = I_{Dsso} \times \left(1 - \frac{V_{GS}}{V_T}\right)^2 \times [1 + \lambda V_{GS} V_{DS}] \times \tanh[\alpha V_{GS} V_{DS}]$	[111]
Angelov	$I_{DS} = I_{pk}(1 + \tanh(\psi))(1 + \lambda V_{DS}) \tanh(\alpha V_{DS})$ $\psi = P_1(V_{GS} - V_{pk}) + P_2(V_{GS} - V_{pk})^2 + P_3(V_{GS} - V_{pk})^3 + ...$ $P_1 = P_{sat}\left(1 + \frac{B_1}{\cosh^2(B_2 V_{DS})}\right)$	[115]
TOM3	$I_{DS} = \beta(V_G)^Q(1 + \lambda V_{DS})\frac{\alpha V_{DS}}{(1 + (\alpha V_{DS})^k)^{\frac{1}{k}}}$ $V_G = QV_{st}ln(1 + e^u),\ u = \frac{V_{GS} - V_{th} + \gamma V_{DS}}{QV_{st}}$	[116]
McCamant	$I_{DS} = \frac{I_{dso}}{1 + \delta V_{DS} I_{DSO}}$ $I_{DSO} = \begin{cases} \beta\left(V_{GS} - V_T - \delta V_{DS}\right)^\eta \left[1 - \left(1 - \frac{\alpha V_{DS}}{3}\right)^3\right] & 0 \le V_{DS} \le \frac{3}{\alpha} \\ \beta\left(V_{GS} - V_T - \delta V_{DS}\right)^\eta & V_{DS} \ge \frac{3}{\alpha} \end{cases}$	[117]
Curtice	$I_{DS} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \tanh(\gamma_2 V_{DS})$ $V_1 = V_f\left(1 + \beta_2(V_{DSO} - V_{DS})\right)$	[124]
Riaz	$I_{DS} = \beta\left(1 - \frac{\delta V_{GS}}{V_T + \Delta V_T + \gamma V_{DS}}\right)^2 \left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right) \tanh(\alpha V_{DS})$	[26]

2.6.4 Capacitor Models

Miller capacitors (C_{GS} and C_{GD}) play an important role in determining the RF performance of a FET. An accurate assessment of Miller capacitors is therefore, important to guage f_T and f_{max} of a given FET. Experimentally determined S-parameters are used to evaluate C_{GS} and C_{GD}, which are primarily defined by the source and drain side depletion layer of Schottky barrier gate, respectively. The same can be assessed theoretically by knowing L_g, W, N_D, and dimensions of depletion layers on either side of the gate.

Takada et al. [131] and Shur et al. [132] presented a detailed physical capacitor models to calculate the capacitance of MESFETs. At different bias, they derived analytical expressions for C_{GS} and C_{GD}, and found good agreement with the experimental data. Scheinberg et al. [133], reported a model to simulate $C-V$ characteristics of MESFETs. Different simulators were used, e.g. SPICE and CAD for real time implementation of their work.

By employing Poisson's equation, Chang et al. [145], Bose et al. [136] and Murray et al. [137] developed models to calculate the total charge distribution underneath the gate. They developed expressions for C_{GS} and C_{GD} on the basis of charge distribution. Zhu et al. [139] presented a comprehensive model by extending Murray et al. [146] work. They claimed that the charge distribution near the drain side is not negligible due to the charge extension, and demonstrated comparatively better results than Murray model.

Avolio et al. [141] developed a charge model for microwave transistor. They derived charge equations extracted from both small signal and large signal measurements, which were available in CAD simulator. Kobayashi et al. [142] experimentally investigated the negative capacitance in FETs. They claimed that their newly time dependent model is suitable for ultra low power applications and can work at $>$ MHz. Dong et al. [143] also presented a negative capacitance model

TABLE 2.9: Various models developed so far for assessment of FET's Miller capacitors.

Author	Year	Development	Ref.
Takada et al.	1982	Analytical expressions of variable-capacitance model developed for three regions; before and after pinch-off, and transition region.	[131]
Chen et al.	1985	Low and high pinch-off regions, taking into account feedback capacitance, sidewall capacitance and C_{GS}, designed for CAD.	[132]
Scheinberg et al.	1991	Trans-capacitance term used in Y-matrix for SPICE, empirical equations as a function of bias voltages.	[133]
D'Agostino et al.	1994	Non linear model for MESFET capacitances.	[134]
Nawaz et al .	1997	Quasi-static approximation, 3×3 matrix representing 9 elements for trans-capacitance in CAD applications.	[135]
Bose et al.	2001	Miller capacitances as function of L_g by considering three regions Poisson's equation.	[136]
Murray et al.	2002	Two region charge model for linear and saturation regions, and for C_{GS} and C_{GD} expressions.	[137]
Ahmed et al.	2003	Quarter circle assumption of potential at the drain and source side, device geometry and depletion hight are incorporated.	[138]
Zhu et al.	2006	Consideration of charge distribution near the drain side.	[139]
Jia et al.	2013	L-gate 4H-SiC MESFET with 26% reduction in C_{GS} and C_{GD}.	[140]
Avolio et al.	2014	Developed charge equations from both small signal and large signal measurements.	[141]
Kobayashi et al.	2016	Negative capacitance of FET experimentally investigated first time.	[142]
Dong et al.	2017	A negative capacitance model incorporating reverse DIBL and negative output differential conductance effects	[143]
Lu et al.	2018	Analytical capacitor and charge model for hetero gate dielectric tunneling FETs.	[144]

for FETs. They reported that reverse DIBL and negative output differential conductance can cause these effects in the device. Table 2.9 shows a summary of capacitor models developed in the last decades.

2.7 RF/AC Analysis

As discussed earlier, RF performance of the device depends collectively on channel properties, device geometry and the material chosen for its fabrication. Channel doping effects G_M, f_T and f_{max} of the device. Figure 2.3 shows that both G_M and f_T increases as channel doping increases but, f_{max} decreases with the increase in channel doping level [75]. High doping causes a reduction in the magnitude of μ due to ionized scattering but, on the other hand, this increases I_{DS}, which is a positive factor resulting into an increase in G_M as evident from Fig. 2.3.

SiC Schottky barrier FETs having $L_g = 10$ μm and $W = 400$ μm were investigated in Ref. [147] and a maximum value of $G_M = 0.7$ mA/V was reported. Weitzel et al. [6] measured the output power, S-parameters and DC characteristics of MESFETs having $L_g = 0.7$ μm and $W = 332$ μm. They observed $G_M = 42$ mS/mm, gain = 9.3 dB, $f_{max} = 12.9$ GHz, $f_T = 6.7$ GHz, PD = 2.8 W/mm and PAE = 12.7%.

Huang et al. [75] proposed numerical simulations for 4H-SiC MESFET. RF characteristics were derived using 2-D numerical drift diffusion model and it was found that f_T and f_{max} can be increased by reducing L_g up to 0.1 μm. Sayed et al. [148] designed a 5 W ultra wideband power amplifier by using SiC MESFET. For a given frequency range, i.e. 10 MHz−2.4 GHz, using shunt feedback and input/output matching topology, they measured the power performance of the amplifier, i.e. gain of 8 dB, output power of 37 dBm and PAE of 35%.

Hossein [149] proposed a 4H-SiC high power RF MESFET with a combination of L-gate source field plate (LSFP-MESFET). The device produced 91% larger V_B and 4 times higher PD compared to conventional MESFET. Also, f_T and f_{max} of the device were found to be 23.1 GHz and 85.3 GHz, respectively, and maximum

TABLE 2.10: RF power performance of different MESFETs.

L_g (μm)	W (μm)	PD (W/mm)	f_T (GHz)	f_{max} (GHz)	PAE (%)	Ref.
0.4	1000	4.1	-	15.9	63	[150]
0.45	250	0.8	18	50	63	[45]
0.5	200	2.1	9.1	26.2	21.1	[20]
0.7	500	1	9	25	54	[45]
0.8	250	8.9	-	-	30	[151]

stable gain (MSG) of 22.7 dB was achieved at 3.1 GHz. For S-band power amplifier, Xiao et al. [50] proposed p-buffer layer doped SiC MESFETs and observed that it improved PD and linear gain when compared with the conventional SiC MESFET. RF performance of different MESFETs as a function of L_g and W is presented in Table 2.10.

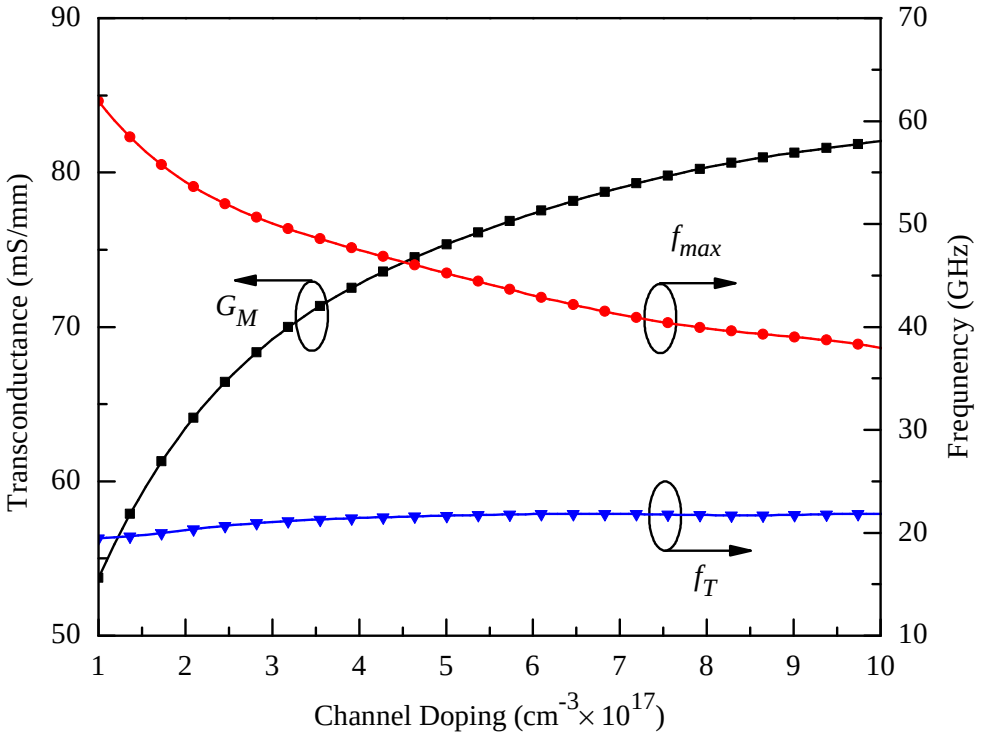

FIGURE 2.3: Effect of channel doping on small-signal parameters of 4H-SiC MESFET [75].

2.8 Intrinsic Parameter Extraction Techniques

For intrinsic parameters extraction of the device, usually two methods are used: analytical method [152, 153] and optimization [154].

The first approach is robust and comprehensive, and many researchers have opted this technique wherein, circuit is reduced to intrinsic part to get Y-parameters of the device. To check the device behavior for high power and frequency, these Y-parameters are then converted into S-parameters. On the basis of analytical solution, Berroth [155] proposed an improved model for small signal modeling of FETs that can work for wide range of frequencies. Minasian et al. [156] by removing extrinsic parameters of the device, evaluated intrinsic part up to a frequency range of 10 GHz. Diamand at el. [157] presented a method for the assessment of parasitic impedances of the device in terms of Z-parameters. At different gate bias, real part of Z-parameters were used to calculate parasitic resistances, while inductances were determined from the imaginary part.

For diagnostic and design purpose, Curtice et al. [158] presented a procedure to extract device parameters by using S-parameters, as well as DC characteristics. In 1989, Giovanni et al. [159] proposed a detailed model for both small and large signal parameters of MESFETs that linked CAD and the device circuit design. They first extracted intrinsic parameters in terms of reverse Y-parameters, and then on the basis of these intrinsic parameters, they extracted extrinsic parameters for large signal model. Golio et al. [160] reported device behavior at low frequency incorporating G_M and output resistance.

In 1992, Angelov et al. [161] extracted small signal parameters from DC characteristics and its derivatives. At different bias points, S-parameters were observed by using Vector Network Analyzer (VNA) up to 62.5 GHz. At $V_{DS} = 0$ V, Angelov model gave accurate parasitic parameters by operating the device in normal mode. In 1993, Eskandarian et al. [162] developed expressions for parasitic inductances of FET by using "HOT-COLD" measurement technique. These expressions were used when the device parasitic capacitances had significant effect on biased gate.

All intrinsic parameters were in good agreement except internal resistance R_I and τ.

Lin and Kompa [163] presented 15 elements based small signal FET model. On the basis of an efficient and fast objective function, they applied multi biased data fitting for a set of measured S-parameters up to 40 GHz. Their method was highly sensitive in error measurement. Their work showed that high variations in incremental resistance has minimum effect on the calculation of intrinsic parameters, i.e. G_M, C_{GS} and C_{GD}. Shirakawa et al. [164] presented a simple small signal model of a HEMT by using an analytical parameter transformation technique. Using 100 different bias points, they measured S-parameters up to 62.5 GHz iteratively to minimize the variance of intrinsic parameters.

In 1994, Schoon [173] performed both small and large signal modeling on dual-gate FET. For a wide range of biased voltages, a detailed process was used to measure intrinsic parameters of the device. In 1995, Gonzalez et al. [165] used Monte Carlo technique to extract intrinsic parameters of FET. Their proposed model showed that at low I_{DS}, intrinsic elements were frequency independent. On the other hand, for large values of I_{DS}, C_{GD} and G_D were frequency dependent due to the charge dynamic process in the channel of the device.

In 1996, Van et al. [166] presented 13 elements based small signal model of GaAs FET by using decomposition bases an optimization process. For each element, they used an error function in order to reduce uniqueness problem in parasitic resistances. Rorsman et al. [174] discussed HEMTs small signal modeling by using iterative method. Measured S-parameters were used to extract the device parameters up to 50 GHz.

Dambrine et al. [152] proposed a fast and systematic method to extract all parasitic parameters by incorporating pad capacitances of the device. Berroth et al. [155] extended Dambrine et al. work and extracted small signal parameters with parasitic resistances and C_{GD} without frequency limitations. A brief summary of small signal model development so far are described in Table 2.11.

TABLE 2.11: Small signal model characteristics of FETs.

Author	Year	Development	Ref.
Minasian et al.	1977	Extrinsic elements removed, simplified model for L_g=1 μm up to 10 GHz.	[156]
Ghione et al.	1989	Intrinsic parameters in term of Y-parameters for CAD simulations.	[159]
Golio et al.	1990	G_M and output resistance behavior at low frequency. Mechanism of trapping described by using three equivalent circuit elements.	[160]
Angelov et al.	1992	S-parameters observed by using Vector network Analyzer (VNA) up to 62.5 GHz with L_g = 0.35 μm and W = 200 μm.	[161]
Eskandarian et al.	1993	"HOT-COLD" measurement technique used for extraction. R_I and τ found not in good agreement, as C_{GS} appears in series.	[162]
Lin et al.	1994	15 element FET model, S-parameters up to 40 GHz for L_g = 0.5 μm.	[163]
Gonzalez et al.	1995	Monte Carlo technique was used, C_{GD} and G_S were evaluated.	[165]
Van et al.	1996	13 elements FET model, optimization process used, R_G has great impact on small signal properties.	[166, 167]
King et al.	1998	Mathematical model for unstable parameters. ~1% error in $\|S_{11}\|$ causes ~98% error in R_I.	[168]
Sabat et al.	2009	Different optimization techniques were used for 16 elements SSM over 0.5 to 25 GHz.	[169, 170]
Liu et al.	2010	Improved small signal model for SiC MESFETs, optimized intrinsic parameters over 0.5 to 20 GHz.	[171]
Riaz et al.	2017	SSM developed using I_{DS}, instead of Schottky barrier. All intrinsic parameters found in good agreement with conventional and experimental data.	[172]

2.9 Novel Structures

Wide bandgap semiconductor devices have been developed for high power applications and have shown great potential in comparison with Si and GaAs based

devices. Semiconductor devices fabricated using SiC, GaN, etc. offer better saturation velocity along with high operating voltages due to their high band gap. Researchers are trying to improve further the performance of wide bandgap MESFETs by suggesting novel structures in addition to improved material properties.

In [175], the authors presented a modified SiC MESFET structure with a gate-buffer layer combined with a p-type spacer. For a thickness of 75 nm of p-type spacer and gate buffer with doping $1{\times}10^{16}$ cm^{-3} and $5{\times}10^{15}$ cm^{-3}, respectively, SiC MESFETs exhibited maximum performance significantly higher than the conventional structure.

To improve voltage breakdown region, numerous device structures for SiC MESFETs have been reported such as: field plate structure that produced almost two times the normal V_B [176]; recessed source-drain drift region having metal plate termination method (DRMPR-MESFET) [177]; narrowly recessed gate [178], fully depleted Si-on-insulator (FD-SOI MESFET) [179] and triple recessed MESFET (TRG-SOI MESFET) [180] structures.

Orouji et al. [181] compared double-recessed 4H-SiC MESFET with undoped space region (DRUS-MESFET) and conventional double-recessed MESFET (DR-MESFET). After placing the undoped space region in the channel, V_B increased due to low doping concentration and modified electric field. Output PD increased by a factor of 25.4% compared to DR-MESFET. Also, f_T and f_{max} increased by a factor of 13.07% and 95.6%, respectively. In their previous work [182], they investigated drain side double-recessed gate (DS-DRG) and showed its impact near the drain side, and compared this with source side double recessed gate (SS-DRG). V_{Br} of 170 V was observed with DS-DRG, while it was 130 V with SS-DRG. Similarly, drain current for DS-DRG had a large value compared to SS-DRG.

Lakhdar et al. [183] presented a 2-D analytical model describing the sub-threshold behavior of double gate GaN (DG-GaN) MESFETs. Short channel and DIBL effects were improved compared to single gate GaN (SG-GaN) MESFETs because, double gate technology enhanced the channel potential variation. Also, threshold voltage roll-off as a function of L_g and channel potential as a function of channel

TABLE 2.12: Novel structures development for FETs.

Author	Year	Development	Ref.
Song et al.	2004	Enhanced gate structure with p-type spacer.	[175]
Cha et al.	2005	Field plate structure produced almost double V_{Br}.	[176]
Orouji et al.	2011	Performance comparison of DRUS-MESFET and DR-MESFET. P_D, f_T and f_{max} increased by factor of 25.4%, 13.07% and 95.6%, respectively, with DRUS-MESFET.	[182]
Lakhdar et al.	2011	Comparative analysis of DG-GaN MESFET with SG-GaN MESFET. DG-GaN MESFET showed good potential.	[183]
Moghadam et al .	2011	PD increases by three times using CB-MESFET structure compared to CSOI-MESFET.	[184]
Lee et al.	2014	Quantum well electron blocking layer (QW-EBL) was used in AlGaN/GaN/AlGaN HEMTs.	[185]
Ramezani et al.	2016	Symmetrical structure for 4H-SiC MESFET, V_B increased.	[186]

length showed enhanced results for DG-GaN MESFETs compared to SG-GaN MESFETs.

An insulator region also effects V_B of the device. In [184], the authors showed that silicon-on-insulator in insulator region (ISOI) structure was more suitable than conventional bulk (CB-MESFET) and 4H-SiC SOI MESFETs. They observed that RF performance of the device increases due to the depletion region extension and the device PD also increases by three times using CB-MESFET structure.

Lee et al. [185] presented a novel concept to increase V_B of HEMTs by using quantum well electron blocking layer (QW-EBL) of AlGaN/GaN/AlGaN. A good confinement in 2-DEG was observed due to high electric field produced due to QW-EBL, which led to reduction in drain current spreading into the substrate. By modifying electric field near the gate in symmetrical structure for 4H-SiC MESFET, improvement in the V_B was observed by Ramazani et al. [186]. A summary of MESFET's novel structures is presented in Table 2.12.

2.10 Summary

In this chapter, a detailed overview of FETs (MESFETs and HEMTs) is given. Device performance with different aspects is reported. The performance of a FET depends upon the material used for its fabrication. It has been observed that devices fabricated using SiC and GaN have superior performance, both in DC and RF domain compared to GaAs MESFETs. SiC MESFETs have excellent heat conduction in high power applications and shows maximum stability in performance. By using work done by different researchers, it is shown that SiC MESFETs have a great potential to be used in harsh environments.

Device characteristics can be predicted by using analytical or numerical models. Numerical models are easy to conceive, as they deal with the device parameters, which can be manipulated effectively and efficiently through a nonlinear expression. On the other hand, analytical models require the electric field distribution inside the channel and can be quite complex as the field distribution inside the channel is non-uniform.

The RF performance of FETs rely mainly upon the device intrinsic parameters. Parameter extraction techniques play a crucial role in determining the accuracy of the predicted intrinsic parameters. For accurate small signal modeling, a suitable capacitor model is needed. Such a model could help the design engineer to assess the reliability of the device under changing conditions.

SiC and GaN based devices can be operated at higher drain-to-source voltages compared to GaAs, which causes self-heating effects in the device. Self-heating effects are directly proportional to the power handled by the device. Under high bias, characteristics of the device may degrade, and a simple model may not be accurate enough to predict the device performance. So, there is a need to develop a model for SiC MESFETs that incorporates self-heating effects.

It is also discussed that in heterostructure devices, properties of the chosen substrate play an important role in device modeling. GaN HEMTs fabricated on

Si and SiC substrates have shown efficient power performance. By varying the structure of a FET, its performance can be improved.

Chapter 3

Temperature Dependent FET's Analytical Model

3.1 Introduction

In this chapter, an attempt has been made to develop a model to predict $I-V$ characteristics of wide bandgap MESFETs; especially those, which exhibit self-heating effects in their output characteristics. This requires an accurate assessment of charge distribution inside the Schottky barrier depletion layer of the device. For this purpose, the depletion layer was distributed into four distinct regions, which facilitated an improved potential assessment inside the channel; leading to the development of an $I-V$ expression for the device output characteristics.

Due to high power applications and high switching speeds, SiC and GaN MESFETs suffer from self-heating effects because of the variation in the channel conditions [187, 188]. As the drain current (I_{DS}) increases, the temperature in the channel also increases and this in turn decreases mobility of carriers [189]. This leads to an overall reduction in the performance of a MESFET [190]. This degradation is further enhanced if the device is subjected to higher ambient temperature. However, in SiC and GaN MESFETs, these effects are relatively lower compared to other commercially used materials such as Si and GaAs [191]. Hence, SiC and

GaN based devices can operate at a relative wider temperature range compared to Si/GaAs devices.

Self-heating effects should be taken into consideration while developing an analytical model; especially for wide bandgap semiconductor MESFETs, because they are primarily meant to operate at high bias and also at high switching speeds. Royet et al. in 2000 [187] developed an analytical model, incorporating self-heating effects, for long channel SiC MESFETs by dividing the gate depletion, underneath the Schottky barrier gate, into two regios: a region representing the depletion before the velocity saturation and the 2^{nd} region of the depletion after the onset of velocity saturation. They proposed temperature dependent drift velocity using optical phonon coupling, which is difficult for a design engineer to handle.

In 2001, Bose et al. [136] developed an analytical model for GaN MESFETs DC characteristics. In their work, they used Poisson's equation to find the potential distribution across the depletion layer. Using this concept, they calculated the length after which the channel current saturates and eventually they developed an I_{DS} expression for the current flowing through the channel. However, their model did not consider variation in I_{DS} caused by self-heating effects which leads to limited applicability of the model.

Murray et al. [137] in 2002 developed a DC model for SiC MESFETs, wherein they divided the Schottky barrier depletion layer into two regions. They hypothesized that in each of the two regions, depletion height has its own distinct boundary conditions and these remain constant throughout the boundary. They calculated the potential distribution inside the channel and proposed an expression for the DC characteristics of the device. Murray et al. however, have not considered variation in the channel conditions associated with self-heating effects; thus, the model is bound to create discrepancy when the device is subjected to harsh operating conditions.

Zhu et al. [139] in 2006 extended the model proposed by Murray et al. by considering the extension of the depletion towards the drain side of the Schottky barrier gate. With the addition of the charges accumulated towards the drain side of the

gate, they re-assessed potential distribution inside the channel and found that by ignoring the charge extension towards the un-gated drain side, it is not possible to model the characteristics of the device accurately; especially in the linear region of operation. Although, it is demonstrated that Zhu model is significantly better than Murray model in predicting the DC characteristics of a submicron SiC MESFET but, it is silent as far as self-heating or ambient temperature is concern.

Ahmed et al. [98] in 2017 re-evaluated the potential distribution inside the channel of submicron MESFETs by taking into account three distinct regions of the depletion layer underneath the Schottky barrier gate. They reported that the extension of the depletion layer towards the drain side, for submicron devices, is approximately one forth of the gate length, L_g of the device. They demonstrated an improved accuracy of the modeled DC characteristics of submicron SiC MESFETs in comparison to Zhu model. Since, the model does not accommodate self-heating effects explicitly in its very definition, it would, therefore, bound to generate discrepancy for the devices having negative output conductance because of self-heating effects.

3.2 Model Development

An operating MESFET is shown in Fig. 3.1. In this figure, Region-I is the extension of the depletion towards the source side of the gate, whilst Region-II describes that part of the gate depletion where carriers are moving below the saturation velocity. The start of Region-III defines a location where channel carriers velocity gets saturated, and this region terminates at the end of the Schottky metal towards the drain side of the gate. And finally, Region-IV represents extension of the depletion towards the drain side caused by both the potentials i.e. V_D and V_G.

The device output characteristics depend upon I_{DS} flowing through the channel under the influence of E, and assuming that a is the epi-layer of the device as shown in Fig. 3.1, and $h(x)$ represents height of the depletion layer at any point

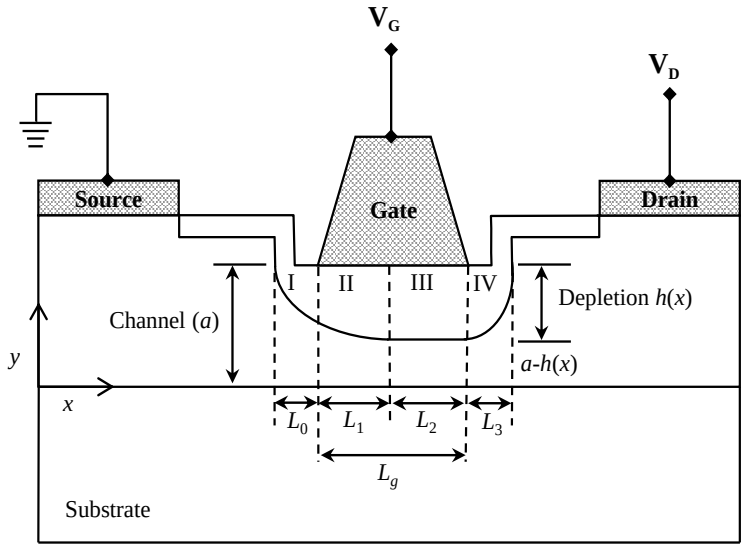

FIGURE 3.1: A crossselectional view of a submicron MESFET.

x under the Schottky barrier gate; such that the available channel for the flow of I_{DS} is $[a - h(x)]$, then one can write [192]

$$I_{DS} = qWN_D\mu(E)E(x)\,[a - h(x)] \tag{3.1}$$

where q is the electronic charge, W is the width of the device, N_D is the channel doping density and $\mu(E)$ represents field dependent mobility of the channel carriers. An empirical relation, which defines $\mu(E)$ is given as [10, 193]

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\dfrac{\mu_0 E}{v_s}\right)^{\beta}\right]^{1/\beta}} \tag{3.2}$$

where μ_0 represents low field mobility of carriers, v_s is the carriers velocity after the onset of current saturation and β is a fitting variable.

In the linear region of operation, I_{DS} of the device increases linearly and its magnitude is dependent upon the bias potentials V_D and V_G. If we represent the linear region current by $I_{DS(\text{lin})}$, then it can be expressed as [137]

$$I_{DS(\text{lin})} = I_P \left[\frac{3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3)}{1 + Z(u_d^2 - u_0^2)}\right] \tag{3.3}$$

In the above expression, u_d and u_0 are unit less quantities, which represent normalized depletion heights towards drain and source side of the device, respectively; and are given by

$$u_d(V_G, V_D) = \frac{h_d}{a} = \sqrt{\frac{V_D + V_G + V_B}{V_P}}$$
$$u_0(V_G) = \frac{h_0}{a} = \sqrt{\frac{V_G + V_B}{V_P}} \tag{3.4}$$

where V_B is the built-in potential of the device; variables h_d and h_0 represent depletion layer heights towards drain and source side of the Schottky barrier gate, respectively. Device pinch-off voltage, V_P and other variables of above mentioned equations are given as

$$I_P = \frac{q^2 N_D^2 \mu_0 W a^3}{6\epsilon_s L_g}, \quad V_P = \frac{qN_D a^2}{2\epsilon_s}, \quad Z = \frac{qN_D a^2 \mu_0}{2\epsilon_s L_g v_s} \tag{3.5}$$

where ϵ_s is the relative permittivity of the semiconductor.

On the other hand, assuming that the current saturation in SiC and GaN MESFETs are caused by the velocity saturation of the channel carriers, then the saturation current, $I_{DS(\text{sat})}$ can be expressed as [194]

$$I_{DS(\text{sat})} = qWN_D\gamma v_s a\,(1 - u_1) \tag{3.6}$$

where γ provides a smooth shift form the linear to the saturation region, and u_1 defines the depletion layer where carriers velocity gets saturated and is expressed as

$$u_1(V_G, V_D) = \sqrt{\frac{V(L_1) + V_G + V_B}{V_P}} \tag{3.7}$$

In Eq. (3.7), the variable $V(L_1)$ defines the potential across the length L_1 underneath the Schottky barrier gate as shown in Fig. 3.1 and is given by

$$V(L_1) = V_P\left(u_1^2 - u_0^2\right) \tag{3.8}$$

By using Eqs. (3.3) and (3.6), the channel length, L_1 can be evaluated in terms of device and bias parameters as given below [98]

$$L_1 = L_g Z \left[\frac{(u_1^2 - u_0^2) - (2/3)(u_1^3 - u_0^3)}{\gamma(1 - u_1)} - (u_1^2 - u_0^2) \right] \tag{3.9}$$

To evaluate the two dimensional potential distribution of the Schottky barrier depletion as shown in Fig. 3.1, Poisson's equation, as given below, can be employed

$$\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = -\frac{qN_D}{\varepsilon_s} \tag{3.10}$$

By changing co-ordinate system as shown in Fig. 3.1, i.e. $x^{'} = x - L_g$, Eq. (3.10) can be rewritten as the sum of $W(x', y) = \xi(y) + V(x', y)$, where

$$\frac{d^2\xi}{dy^2} = \frac{qN_D}{\varepsilon_s} \tag{3.11}$$

and

$$\frac{\partial^2 W(x',y)}{\partial x^2} + \frac{\partial^2 W(x',y)}{\partial y^2} = 0 \tag{3.12}$$

such that

$$W(x', y) = V(x', y) + \frac{qN_D}{2\varepsilon_s} y^2 \tag{3.13}$$

Equation (3.13) can be solved by employing the separation of variables technique and the device boundary conditions to get the potential distribution inside the channel as given below [98]

$$V(L_g, h_1) = V_P\left(u_1^2 - u_o^2\right) + \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi(L_g - L_1)}{2au_1}\right] \tag{3.14}$$

First term of Eq. (3.14) represents the potential of Region-I and II; whereas, second term of Eq. (3.14) represents potential drop in Region-III. From Fig. 3.1, it is obvious that $L_2 = L_g - L_1$, therefore, the 2$^{\text{nd}}$ part of Eq. (3.14) is reduced to

$$V(L_2) = \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_2}{2au_1}\right] \tag{3.15}$$

One can see from Fig. 3.1 that there is no Schottky barrier gate covering Region-IV; resultantly V_G will decay exponentially, causing the depletion layer to diminish quickly. Ahmed et al. [98] proposed that the length of Region-IV can be approximated as $L_3 \approx L_g/4$, resulting into

$$V(L_3) \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_3}{2a u_1}\right] \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_g}{8a u_1}\right] \tag{3.16}$$

In transverse direction, the total potential drop across the Schottky barrier gate will then be equal to the applied potential V_D, which can be written as

$$V(L_0) + V(L_1) + V(L_2) + V(L_3) = V_D \tag{3.17}$$

The combination of Eqs. (3.8), (3.15) and (3.16) forms the following equation

$$V_P\left(u_0^2\right) + V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi\left(L_g - L_1\right)}{2a u_1}\right] + \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_g}{8a u_1}\right] = V_D \tag{3.18}$$

Equation (3.18) gives potential distribution for all the four regions shown in Fig. 3.1. The first term $V_P\left(u_0^2\right)$ of Eq. (3.18), which is ignored in Ref. [98] has been included in this evaluation. Moreover, in Ref. [98] self-heating and temperature effects on the device $I-V$ characteristics have not been taken into consideration, which could lead to a discrepancy in the modeled $I-V$ characteristics. In order to incorporate self and ambient heating effects, assume that R_S and R_D represent source and drain side resistances of the device, respectively; then drain to source voltage, V_{DS} can be written as

$$V_{DS} = V_D + I_{DS}(R_S + R_D) \tag{3.19}$$

such that

$$R_S = \frac{L_s}{N_D q \mu a W} + R_C$$
$$R_D = \frac{(L_d - L_3)}{N_D q \mu a W} + R_C \tag{3.20}$$

where R_C is the contact resistance and L_s and L_d provide separation between source-gate and drain-gate, respectively.

At a given temperature, T, the thermal resistance, R_{TH} of a MESFET channel is defined as [195]

$$R_{TH} = \frac{1}{\pi\kappa} ln\left(\frac{8T}{\pi L_g}\right) \tag{3.21}$$

where κ represents thermal conductivity of the material involved. R_{TH} defined by Eq. (3.21) will change the response of the device based on power handled by it. Therefore, it is proposed that the channel resistance, R_{CH} can be written as

$$R_{CH} = R_{TH}\left(1 + \lambda\left[e^P - 1\right]\right) \tag{3.22}$$

where power, P is defined as $P = V_{DS}I_{DS}$ and λ will adjust the device channel geometry. Now, the temperature dependent drain-to-source current, I_{DST} will be the current generated by the device by taking into account self and ambient heating, and it can be represented by the following expression

$$I_{DST} = I_{DS} - I_{DS}\left(1 - \frac{R_{TH}}{R_{CH}}\right) \tag{3.23}$$

Output conductance, G_{DT} can be obtained by differentiating Eq. (3.23), as given below

$$G_{DT} = \left.\frac{\partial I_{DST}}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} = \left.\frac{\partial\left[I_{DS} - I_{DS}\left(1 - R_{TH}/R_{CH}\right)\right]}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} \tag{3.24}$$

After making substitution for R_{CH} and differentiating, we have

$$\left.\frac{\partial I_{DST}}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} = \frac{\partial I_{DS}}{\partial V_{DS}}\left(\frac{1}{1 + \lambda\left[e^P - 1\right]}\right) + I_{DS}\frac{\partial}{\partial V_{DS}}\left(\frac{1}{1 + \lambda\left[e^P - 1\right]}\right) \tag{3.25}$$

If $\partial I_{DS}/\partial V_{DS} = G_D$, then Eq. (3.25) is reduced to

$$G_{DT} = \frac{G_D}{1 + \lambda\left[e^P - 1\right]} - I_{DS}\left(\frac{\lambda e^P\left(V_{DS}G_D + I_{DS}\right)}{\left(1 + \lambda\left[e^P - 1\right]\right)^2}\right) \tag{3.26}$$

Equation (3.26) can also be written as

$$G_{DT} = \frac{G_D}{(1+\lambda\left[e^P-1\right])^2}\left[\lambda e^P\left(1-I_{DS}\right)-\lambda+1-\frac{I_{DS}^2}{G_D}\right] \tag{3.27}$$

When $V_{DS} < V_{DS(\text{sat})}$, under these conditions, $I_{DS} = I_{DS(\text{lin})}$ and $G_D = G_{DL}$; such that

$$G_{DL} = \frac{I_P}{V_P}\left[\frac{3(1-u_d)-3Zu_d(u_d^2-u_o^2)+2Z(u_d^3-u_o^3)}{\left(1+Z(u_d^2-u_o^2)\right)^2}\right] \tag{3.28}$$

where use of Eqs. (3.3) and (3.4) is made to write Eq. (3.28). On the other hand, in the saturation region of operation, $V_{DS} \geq V_{DS(\text{sat})}$, under such circumstances, $I_{DS} = I_{DS(\text{sat})}$ and $G_D = G_{DS}$; such that

$$G_{DS} = \frac{-3\gamma I_P}{2Zu_1V_P} \times \left.\frac{\partial V(L_1)}{\partial V_{DS}}\right|_{V_{GS}=\text{Cons}} = \frac{-3\gamma I_P}{2Zu_1V_P}\Gamma(V_{GS},V_{DS}) \tag{3.29}$$

To achieve above mentioned expression, Eqs. (3.5), (3.6) and (3.7) are used. By differentiating Eq. (3.18) w.r.t V_{DS} at constant V_{GS}, and incorporating Eqs. (3.7) and (3.9), one can write function $\Gamma(V_{GS},V_{DS})$ as

$$\begin{aligned}\Gamma(V_{GS},V_{DS}) = \Bigg[1+\frac{E_s a}{\pi u_1 V_P}\Bigg\{&\sinh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)-\frac{\pi}{2a}\cosh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)\\ &\Bigg\{L_gZ\left(\frac{(u_1^2-u_o^2)-\frac{2}{3}(u_1^3-u_o^3)}{\gamma(1-u_1)^2}+2u_1\frac{1-\gamma}{\gamma}\right)+\frac{L_g-L_1}{u_1}\Bigg\}\\ &+\sinh\left(\frac{\pi L_g}{8au_1}\right)-\frac{\pi L_g}{8au_1}\cosh\left(\frac{\pi L_g}{8au_1}\right)\Bigg\}\Bigg]^{-1}\end{aligned} \tag{3.30}$$

Transconductance, G_{MT} can be expressed in a similar way as that of G_{DT} and the same is given below

$$G_{MT} = \left.\frac{\partial I_{DST}}{\partial V_{GS}}\right|_{V_{DS}=\text{Cons}} = \left.\frac{\partial\left[I_{DS}-I_{DS}\left(1-R_{TH}/R_{CH}\right)\right]}{\partial V_{GS}}\right|_{V_{DS}=\text{Cons}} \tag{3.31}$$

By substituting R_{CH} and differentiating with respect to V_{GS}, we get

$$\left.\frac{\partial I_{DST}}{\partial V_{GS}}\right|_{V_{DS=\text{Cons}}} = \frac{\partial I_{DS}}{\partial V_{GS}}\left(\frac{1}{1+\lambda\left[e^{P}-1\right]}\right) + I_{DS}\frac{\partial}{\partial V_{GS}}\left(\frac{1}{1+\lambda\left[e^{P}-1\right]}\right) \tag{3.32}$$

Considering $\partial I_{DS}/\partial V_{GS} = G_M$, Eq. (3.32) is transformed to

$$G_{MT} = \frac{G_M}{1+\lambda\left[e^{P}-1\right]} - I_{DS}\left(\frac{\lambda e^{P} V_{DS} G_M}{\left(1+\lambda\left[e^{P}-1\right]\right)^{2}}\right) \tag{3.33}$$

Above expression can also be written as

$$G_{MT} = \frac{G_M}{\left(1+\lambda\left[e^{P}-1\right]\right)^{2}}\left[\lambda e^{P}\left(1-P\right)-\lambda+1\right] \tag{3.34}$$

When $V_{DS} < V_{DS(\text{sat})}$, under these conditions, $I_{DS} = I_{DS(\text{lin})}$ and $G_M = G_{ML}$; such that

$$G_{ML} = \frac{3I_P}{V_P}\left[\frac{(u_o-u_d)+Zu_ou_d(u_d+u_o)-Z(u_d^3-u_o^3)}{\left(1+Z(u_d^2-u_o^2)\right)^{2}}\right] \tag{3.35}$$

On the other hand, when $V_{DS} \geq V_{DS(\text{sat})}$, this resulted into $I_{DS} = I_{DS(\text{sat})}$ and $G_M = G_{MS}$; such that

$$G_{MS} = \frac{3\gamma I_P}{2Zu_1V_P}\left[\frac{L_gZE_s}{V_P}\left\{\frac{(1-u_0)-\gamma(1-u_1)}{\gamma(1-u_1)}\right\}\cosh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)\right]\Gamma(V_{GS},V_{DS}) \tag{3.36}$$

In writing the above expression, use of Eqs. (3.6), (3.18) and (3.30) is made.

3.3 Modeled Characteristics

To ensure the validity of the developed technique, MESFETs of varying L_g and W were selected and their DC characteristics were modeled and compared with the experimental data. Table 3.1 represents physical parameters of the selected devices. The chosen GaN MESFET was fabricated by [196] on a 200 nm thick n-GaN active layer grown using metal organic chemical vapor deposition upon a

sapphire substrate. Prior to active layer formation, a 3.6 μm thick undoped buffer layer along with a 25 nm thick nucleation layer was also deposited to improve the quality of the active layer. Devices were fabricated using standard lithography and lift-off processes and the finished device physical dimensions are given in Table 3.1. On the other hand, the detail of chosen SiC MESFET are given in [197], wherein recessed type devices were realized using heavily doped contact layer upon a moderately doped channel layer. The layer structure including the buffer layers were grown by chemical vapor deposition technique upon a semi-insulating SiC substrate. Devices were fabricated using lift-off process and the physical dimensions of a finished SiC MESSFET along with its electrical parameters are elaborated in Table 3.1. Room and high temperature measurements of the finished but unpacked devices were carried out using on-wafer direct measurements.

TABLE 3.1: Physical parameters of GaN/SiC MESFETs.

Parameters	**GaN**	**4H-SiC**
gate Length, L_g (μm)	0.3	1.0
Gate Width, W (μm)	100	500
Epi-layer thickness, a (μm)	0.2	0.3
Doping Density, N_D ($\times 10^{17}$ cm^{-3})	2.7	1.1
Gate-Source Separation, L_s (μm)	1.0	0.5
Gate-Drain Separation, L_d (μm)	2.3	2.0
Thermal Conductivity, κ (W/m-K)	160	490
Electron Mobility, μ (cm^2/Vs)	330	700
Built-in Potential, V_{bi} (V)	1.3	1.1
Band-Gap, E_g (eV)	3.49	3.26
Saturation Velocity, v_s ($\times 10^7$cms^{-1})	2.5	2.2
Breakdown Voltage, $V_{\rm Br}$ ($\times 10^6$ Vcm^{-1})	3.0	3.0

By using Eq. (3.23), the device output characteristics can be plotted, which incorporate both the self-heating as well as the ambient temperature effects on the device performance. The expression does not include the effect of temperature

which could be caused by the devices mutual conductance for an integrated circuit. Figure 3.2 shows measured [196] and modeled output characteristics of a GaN MESFET. Dotted lines, as shown in the figure, represent a significant deviation from the experimental data, especially in the saturation region of operation. Moreover, this deviation is more pronounced at higher drain current. Since at higher drain current, self-heating effects are also higher and the model presented in [98] does not consider the self-heating effects in its very development; resultantly there is deviation from the experimental data. It is pertinent to mention here that the performance of the model presented in [98] improves when output conductance of the device, in the saturation region of operation, is either zero or positive. As the model is not designed for negative conductance of the device; thus, it is bound to generate relatively higher errors if the device exhibits negative conductance after the onset of current saturation.

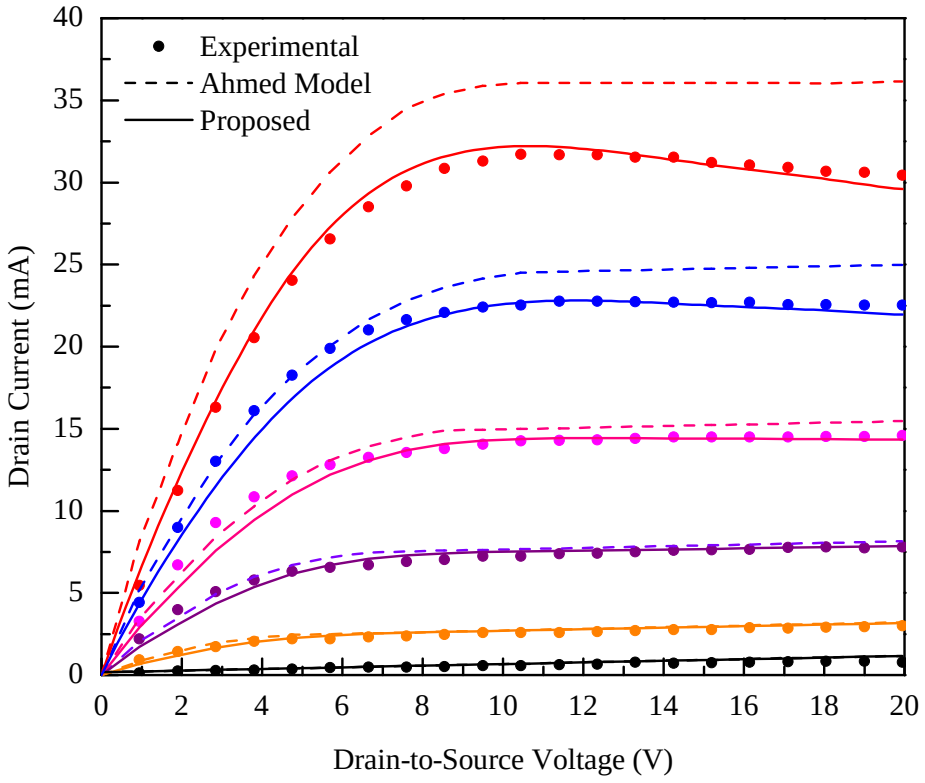

FIGURE 3.2: Modeled and experimental [196] DC characteristics at $T = 300$ K of a 0.3 μm GaN MESFET for $V_{GS} = 1$ V to -9 V with a step of 2 V.

In Fig. 3.2, solid lines show characteristics drawn with the proposed modified model. A significant improvement can be seen when compared with model presented in [98]. The observed improvement is both in the linear as well as in the saturation region of operation, which is primarily due to the inclusion of self-heating term in the model expression. Table 3.2 shows bias dependent root mean square (RMS) errors for the proposed model relative to the experimental data. For comparison purposes, errors obtained from the model presented in [98] are also listed. Examining the data of the table, it is obvious that the proposed model has outperformed [98] in all reported values of V_{GS}. And on the average, the proposed model exhibited $\sim 53\%$ improvement in predicting the DC characteristics of a GaN MESFET.

TABLE 3.2: Bias dependent RMS error values between the modeled and the experimental output characteristics of a 0.3 μm GaN MESFET. Bold faces show lowest observed values.

Model	V_{GS}						**Avg.**
	1 V	**−1** V	**−3** V	**−5** V	**−7** V	**−9** V	
Ahmed	0.8620	0.3736	0.2116	0.1583	0.1272	0.2236	0.3261
Proposed	**0.1132**	**0.1591**	**0.1829**	**0.1337**	**0.1051**	**0.2203**	**0.1524**

Figure 3.3 shows measured [189] and modeled output characteristics of a 1 μm SiC MESFET at $T = 300$ K. Once again, it is obvious from the figure that the proposed model performance is significantly better than the model presented in [98]. It is pertinent to mention here that at $V_{GS} = 0$ V, there is maximum current flowing from the channel; resulting into larger heat dissipation thus, higher negative conductance in the saturation region of operation is seen in Fig. 3.3. In conformity to Fig. 3.2, there is more discrepancy in this case between the model presented in [98] and the experimental data. This effect is subsequently improved for the cases where less magnitude of I_{DS} is flowing from the channel. Contrary to this, the proposed model provides, in general, improved performance irrespective of the gate bias thus, indicating its ability to predict $I - V$ characteristics of wide bandgap MESFETs designed for power and harsh environment applications,

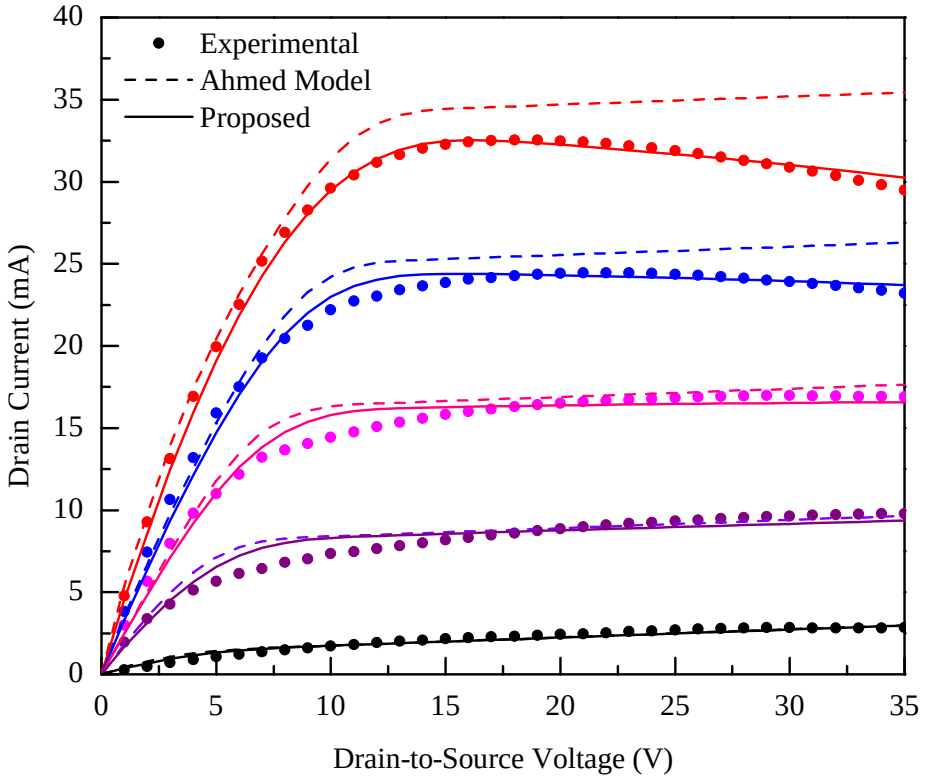

FIGURE 3.3: Modeled and experimental [189] DC characteristics at $T = 300$ K of a 1 μm SiC MESFET for $V_{GS} = 0$ V to -16 V with a step of 4 V.

independent of their fabrication material. Furthermore, it is also noted that the model is capable to predict $I-V$ characteristics for the long channel ($L_g = 1$ μm) as well as for the short channel ($L_g = 0.3$ μm) devices, fabricated using wide bandgap material, exhibiting its wider applicability, provided the material properties remain intact. On the other hand, this model may not be fully valid for MESFETs having different physical structure then the one chosen in this research. Because, in that case Poisson's equation solution could be different; leading to a changed potential distribution inside the channel and hence a changed response.

Table 3.3 shows V_{GS} dependent RMS error values, at $T = 300$ K, for the proposed and Ahmed model for a SiC MESFET whose characteristics are shown in Fig. 3.3. It is obvious from the data of the table that the proposed model performance is relatively better than Ahmed model for values of V_{GS} considered for error evaluation. On average, the proposed model achieved $\sim 54\%$ improved performance

relative to Ahmed model.

TABLE 3.3: Bias and temperature dependent RMS error values in modeled output characteristics. Bold faces show lowest observed values.

Temp.	**Model**	V_{GS}					**Avg.**
		0 V	**−4** V	**−8** V	**−12** V	**−16** V	
$T = 300$ K	**Ahmed**	0.5576	0.3612	0.2379	0.2525	0.1319	0.3082
	Proposed	**0.0798**	**0.1229**	**0.1635**	**0.2122**	**0.1163**	**0.1390**
$T = 500$ K	**Ahmed**	0.2652	0.1865	0.0869	0.0889	**0.1435**	0.1542
	Proposed	**0.1035**	**0.1004**	**0.0605**	**0.0771**	0.1443	**0.0972**

Figure 3.4 shows measured and modeled output characteristics, once again, for the device of Fig. 3.3 but, at $T = 500$ K. It is an established fact that at elevated temperature the channel offers increased scattering; resulting into reduced I_{DS}, which is evident from the $I-V$ characteristics of Fig. 3.4. Examining the plots of Figs. 3.3 and 3.4 simultaneously, it is evident that by increasing the temperature from $T = 300$ K to $T = 500$ K, the magnitude of I_{DS} reduces to almost 50%. Since the device current is reduced, the negative conductance in the saturation region of operation, as discussed before, also reduces. It has been observed earlier that at relatively lower current, there is an improvement in the performance of Ahmed model and the same is reflected by the characteristics shown in Fig. 3.4. An improved performance by Ahmed model at $T = 500$ K relative to $T = 300$ K cannot be associated with the model expression, because the model expression does not take into account the ambient temperature as a variable. Rather, this improvement is due to the lowering of I_{DS}, which also lowered the negative output conductance of the device, especially, at $V_{GS} = 0$ V. Thus, reducing the gap between the modeled and observed output characteristics. This fact is also evident from the data of Table 3.3, where the gap between observed RMS errors for the proposed and the model presented in [98] evaluated at $T = 500$ K is relatively lower and the average RMS error for the proposed model shows $\sim 37\%$ improvement, which is lower than the earlier two reported values.

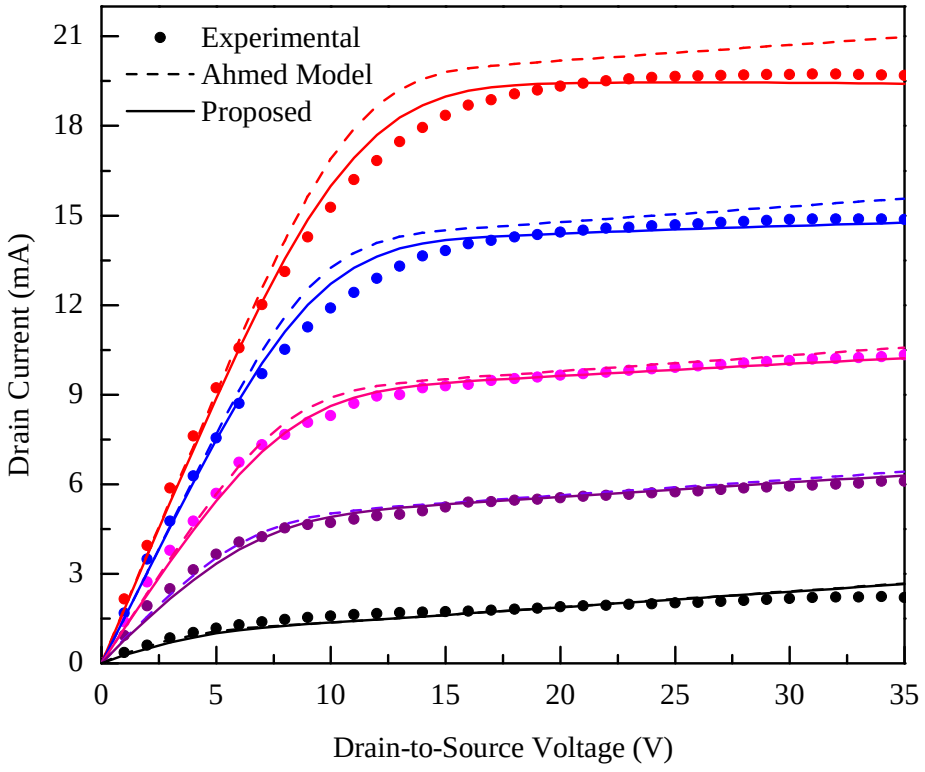

FIGURE 3.4: Modeled and experimental [189] DC characteristics at $T = 500$ K of a 1 μm SiC MESFET for $V_{GS} = 0$ V to -16 V with a step of 4 V.

Equation (3.27) is valid for the entire range of V_{DS} bias and a plot of G_{DT} as a function of V_{DS} with V_{GS} as a variable is shown in Fig. 3.5(a). For comparison purpose, G_D of Ahmed model [98] is also shown in Fig. 3.5(b). It can be seen from Fig. 3.5(a) that the modeled characteristics show a reasonable compliance to the experimental data. According to our conservative estimate, there is no reported model for SiC and GaN MESFETs, which can predict the negative G_D of the device, especially, in the saturation region of operation. The proposed model has the ability to give both negative as well as positive values of G_D with reasonable accuracy.

Table 3.4 shows RMS error values of the two competing models for a 0.3 μm GaN MESFET, whose $I - V$ characteristics are shown in Fig. 3.2. It is obvious from the outcome presented in Table 3.4 that at medium gate bias ($V_{GS} = -3$ to -5 V), the performance of the model presented in [98] is better than the proposed

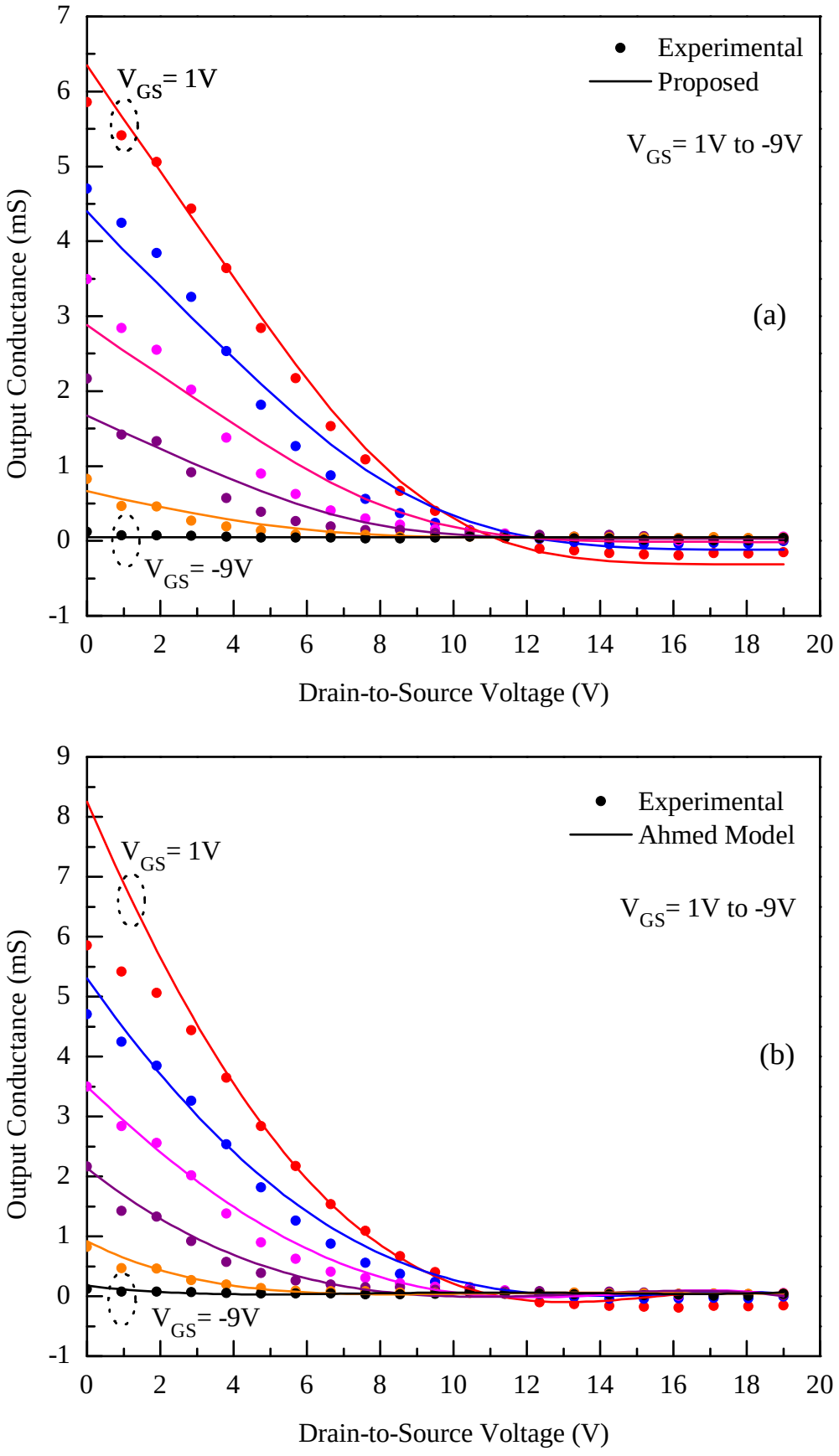

FIGURE 3.5: Modeled and experimental [196] output conductance of a 0.3 μm gate length GaN MESFET at $T = 300$ K (a) Proposed (b) Ahmed model [98].

model, however, the proposed model, in general, offers improved performance, as evident from the data of Table 3.4, and on the average, its performance is $\sim 25\%$ better than Ahmed model.

TABLE 3.4: Bias dependent RMS error values between the modeled and the experimental output conductance of a 0.3 μm gate length GaN MESFET. Bold faces represent lowest error values.

Model	V_{GS}						**Avg.**
	1 V	**−1** V	**−3** V	**−5** V	**−7** V	**−9** V	
Ahmed	0.6201	0.2647	**0.1987**	**0.2007**	0.1676	0.1309	0.2638
Proposed	**0.1363**	**0.2242**	0.2825	0.2511	**0.1504**	**0.1297**	**0.1957**

Figures 3.6 and 3.7 show experimental and modeled G_D of a 1 μm SiC MESFET at $T = 300$ K and $T = 500$ K, respectively. Both the figures are once again validating the proposed Eq. (3.27) representing drain conductance (G_{DT}) of wide bandgap MESFETs, both at room as well as at elevated temperature of operation. Table 3.5 represents RMS error values for the two temperatures under discussion. Average observed improvement relative to Ahmed model, shown in Figs. 3.6(b) and 3.7(b), is $\sim 21\%$ and $\sim 9\%$ at $T = 300$ K and $T = 500$ K, respectively. This demonstrates that the improvement offered by the proposed model is device and ambient dependent. However, in general, the proposed model is relatively better than the best reported analytical model for wide bandgap MESFETs. It is pertinent to mention here that though Ahmed model does not incorporate temperature dependent variable to adjust negative conductance in the saturation region of operation yet it adjusts the value of G_{DT} at $T = 500$ K by adjusting the variable γ, which appears in its definition.

A plot of Eq. (3.34) for $L_g = 1$ μm SiC MESFET is shown in Fig. 3.8, at $T = 300$ K (solid symbols) and $T = 500$ K (open symbols). In the figure, $V_{DS} = 5$ V curves show response of the device in the linear region of operation; whereas, $V_{DS} = 35$ V curves indicate the device G_{MT} for the saturation region of operation for the two temperatures under consideration. Examination of the figure clearly reveals

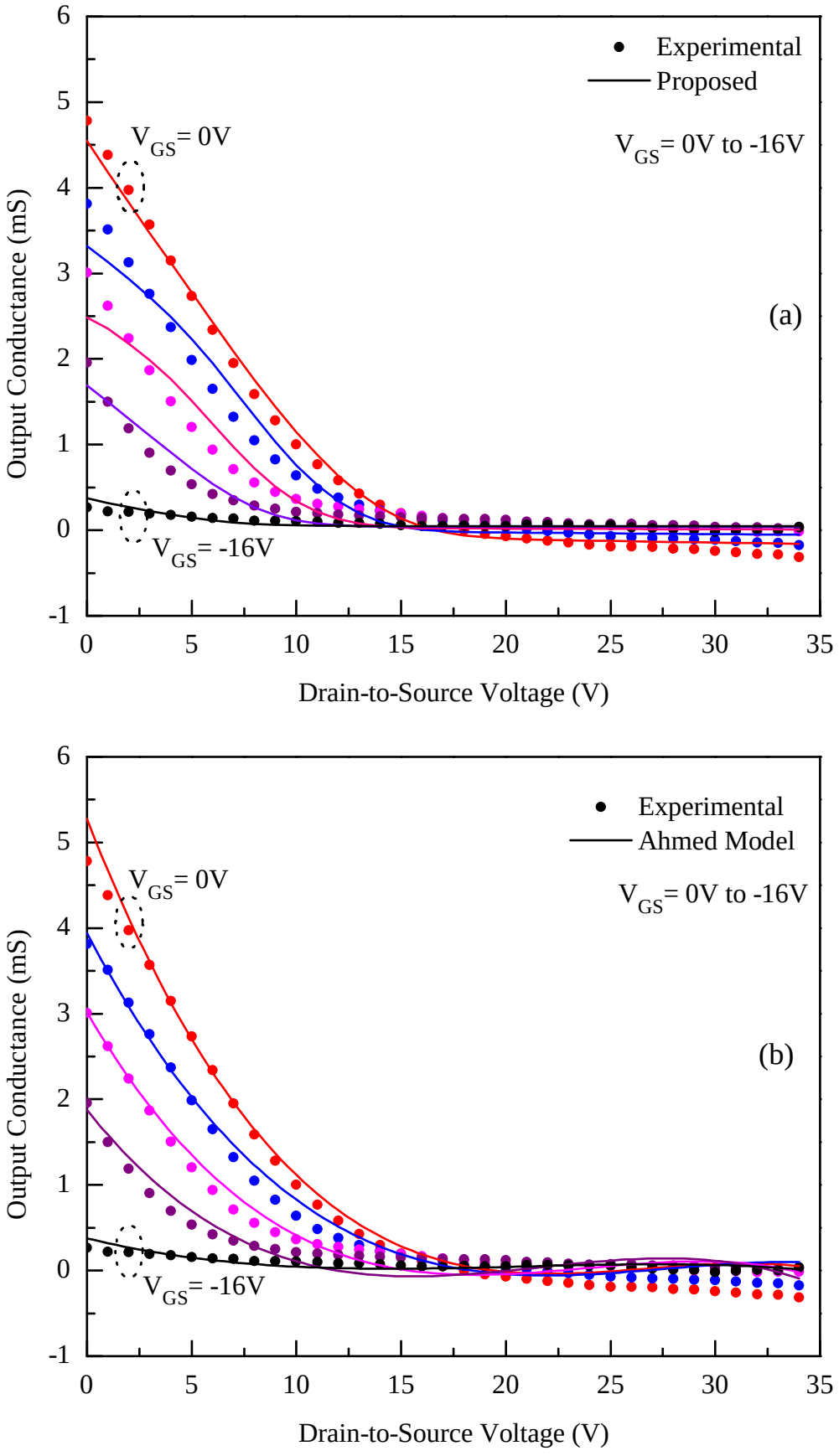

FIGURE 3.6: Modeled and experimental [189] output conductance of a 1 μm gate length SiC MESFET at $T = 300$ K (a) Proposed (b) Ahmed model [98].

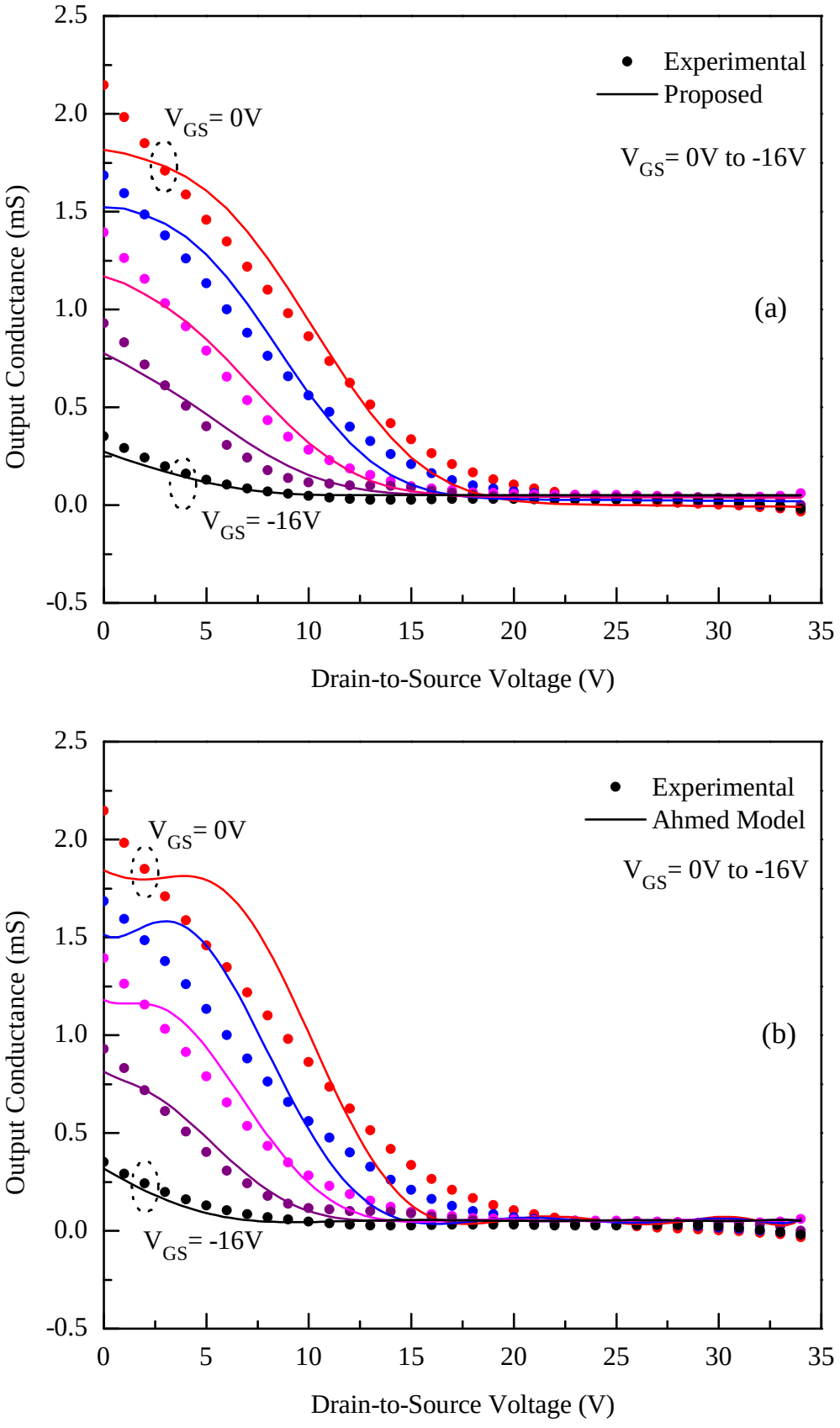

FIGURE 3.7: Modeled and experimental [189] output conductance of a 1 μm gate length SiC MESFET at $T = 500$ K (a) Proposed (b) Ahmed model [98].

TABLE 3.5: Bias and temperature dependent RMS error values between the modeled and the experimental output conductance of a 1 μm gate length SiC MESFET. Bold faces represent lowest error values.

Temp.	**Model**	V_{GS}					**Avg.**
		0 V	**−4 V**	**−8 V**	**−12 V**	**−16 V**	
$T = 300$ K	**Ahmed**	0.2530	0.2259	0.2380	0.1917	0.1882	0.2194
	Proposed	**0.1107**	**0.2043**	**0.2248**	**0.1834**	**0.1394**	**0.1725**
$T = 500$ K	**Ahmed**	0.1824	0.1569	0.1063	**0.0926**	**0.1111**	0.1299
	Proposed	**0.1362**	**0.1166**	**0.1035**	0.1109	0.1231	**0.1180**

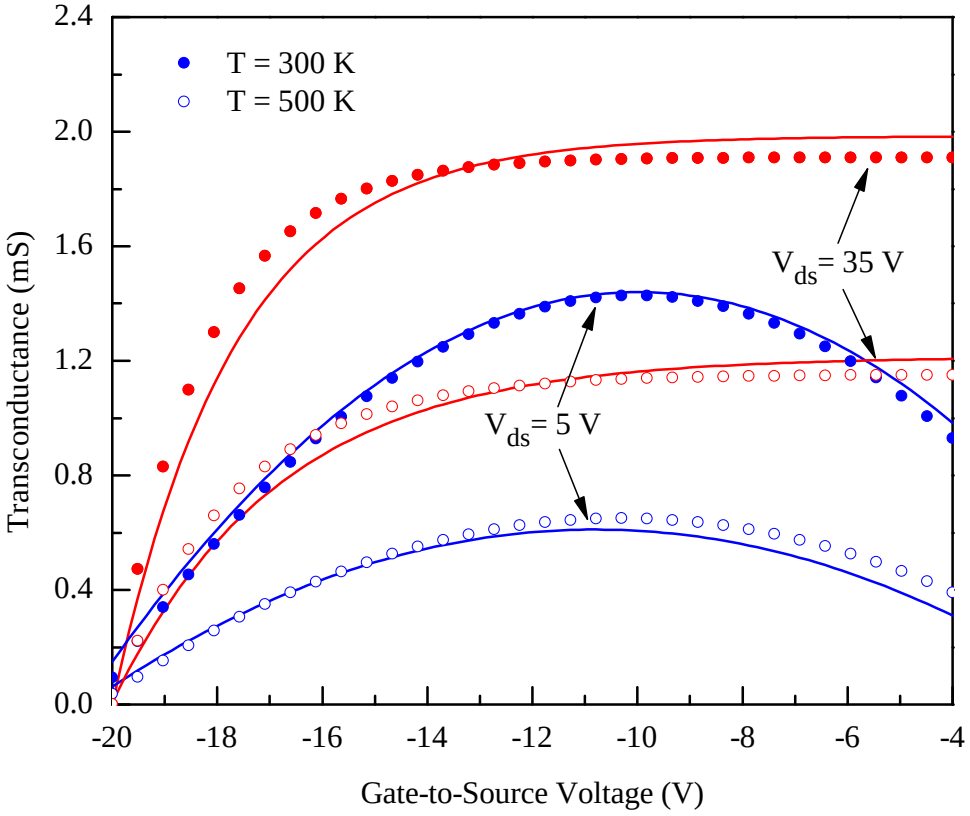

FIGURE 3.8: Measured (symbols) and modeled (lines) temperature dependent transconductance of a 1 μm gate length SiC MESFET.

that at $T = 500$ K, the G_M of the device is deteriorated, which could primarily be associated with the reduction in I_{DST} at elevated temperature.

An interesting feature, which can be noted from the plot of Fig. 3.8 is, that at $T = 300$ K, the profile of G_M responses (solid symbols) are not identical for linear

TABLE 3.6: Bias and temperature dependent RMS error values between the modeled and the experimental transconductance of a 1 μm gate length SiC MESFET. Bold faces represent lowest error values.

Temp.	**Model**	V_{DS}				**Avg.**
		5 V	**10** V	**25** V	**35** V	
$T = 300$ K	**Ahmed**	0.2532	**0.1241**	0.1786	0.3350	0.2519
	Proposed	**0.0850**	0.1271	**0.0188**	**0.0987**	**0.0824**
$T = 500$ K	**Ahmed**	**0.0649**	0.1270	0.0570	0.0898	0.0846
	Proposed	0.0685	**0.0872**	**0.0223**	**0.0521**	**0.0575**

and saturation region of operations. In the saturation region, the G_M profile gives a plateau for certain V_{GS} and then it approaches to zero, indicating that available channel crossection for the flow of carriers is diminishing with increasing magnitude of V_{GS}. On the other hand, in the linear region, where the carriers velocity is less than v_s, the observed peak indicates that for such bias, $V_{GS} \approx -10$ V, the channel performs relatively better than other V_{GS} values.

Table 3.6 shows RMS error values, once again, for the two models under discussion. It is obvious from the average data of the table, that the proposed model offers a $\sim 67\%$ improvement at $T = 300$ K and this value is $\sim 32\%$ at $T = 500$. This data clearly show that the proposed model exhibits a significant improvement in predicting G_{MT} of a wide bandgap MESFET.

3.4 Summary

An improved analytical model for wide bandgap power MESFETs is proposed to predict output and transfer characteristics. The proposed modified model incorporates negative conductance in the saturation region of operation caused by the device self-heating and harsh ambient environment where these devices are normally operated. It has been demonstrated that the proposed model can predict

output characteristics even for submicron MESFETs with a good degree of accuracy. A comparative analysis showed that the developed technique offers $\sim 50\%$ and $\sim 37\%$ improvement in predicting the output characteristics of wide bandgap MESFETs at $T = 300$ K and $T = 500$ K, respectively, relative to the best reported model in the literature. Based on the developed $I - V$ expression, device output conductance and transconductance were also modeled. It has been shown that the proposed technique can model the device output conductance for the entire range of its operation, both at room as well as at elevated temperature with an improved accuracy. Thus, the proposed technique could be useful in assessing the temperature dependent characteristics of wide bandgap MESFETs, meant for high temperature operation.

Chapter 4

Assessment of FET's Intrinsic Capacitors

4.1 Introduction

Silicon carbide (SiC) field effect transistors (FETs) are potential candidates for high temperature and high frequency applications, because they offer higher breakdown voltage and higher carrier mobility [198]. From the design point of view, high frequency capability of a SiC FET is primarily controlled by the device Miller capacitors determined by the depletion layer underneath the Schottky barrier gate. For accurate assessment of gate-to-source, C_{GS} and gate-to-drain, C_{GD} capacitors, it is imperative that the charge distribution underneath the Schottky barrier gate be known to a good degree of accuracy. In high frequency FETs, the gate length of the device is of submicron dimension and for such devices, the extension of charges on the edges of the gate cannot be ignored for accurate Miller capacitors assessment.

In 1976, Yamaguchi et al. [199] derived expressions for Miller capacitors of a FET. They calculated total charge by integrating the channel underneath the Schottky barrier gate. After estimating the total charge, C_{GS} and C_{GD} were calculated. Hartgring et al. [200] derived expressions for C_{GS} and C_{GD} using

Shockley's approximation, but their derived capacitor equations were too complex and difficult to handle by a design engineer.

In 1982, Takada et al. [131] derived analytical expressions for C_{GS} and C_{GD} by dividing the channel into three operational conditions, namely: a) before the pinch-off; b) after the pinch-off, and c) the intermediary status of the depletion. Statz et al. [118] showed that at zero or reverse bias, there is a large capacitor present between source and gate of the device that could cause large error if not taken into account. By involving this concept, they calculated total charge under the gate and derived expressions for C_{GS} and C_{GD}.

Scheinberg et al. [133] presented Miller capacitor model, in 1991, by using bias dependent nonlinear empirical equations. Hallgren et al. [116] also presented gate capacitor model of GaAs MESFETs and demonstrated a good agreement in the modeled and the experimental data but, the developed model was inefficient in time and required 50% more time than its competitors.

Rizk et al. [201] derived gate capacitor equations using normal Schottky junction expressions and claimed improvement in predicting values of Miller capacitors at a given bias. In 1993, Rodriguez et al. [202] presented an improved junction capacitor model for FETs and exhibited by using experimental data that, in addition to the improved accuracy, their developed model is 72% time efficient than its counterparts. Agostino et al. [134], continuing Statz et al. [118] work, also presented a nonlinear capacitor model for FETs. They derived physics-based expressions for nonlinear parameters of the device. In their model, they evaluated total charge underneath the gate by dividing the depletion into three regions. Characteristics thus, achieved were found in good agreement with the experimental data.

Bose et al. [136] derived Miller capacitors of FETs by using expressions presented by Takada and Rodriguez et al. [131, 202]. They showed that Miller capacitors are a function of gate length, as charge underneath the gate is proportional to the gate length of the device. They also extracted high frequency parameters of the device using assessed Miller capacitors and exhibited a reasonable compliance with the experimental data [136].

Murray et al. [137] derived expressions for C_{GS} and C_{GD} for both the linear and the saturation region of MESFETs output characteristics. They partitioned the charges underneath the gate into two regions; depletion region before the saturation, and after the saturation, which was further divided into two parts. First part was underneath the Schottky metal and the second part was extension of the depletion towards the drain side. Murrey et al. however, didn't compare their model experimentally, so no conclusion can be made about the accuracy of the model. In 2003, Ahmed [138] presented a method to calculate Miller capacitors of the device by using DC characteristics. Incorporating quarter circle assumption of potential at the source and at the drain side, C_{GS} and C_{GD} were found. In 2005, Aggarwal et al. [34] presented a capacitor model for SiC MESFETs. By calculating total charge under the gate as a sum of both linear and saturation regions, they showed that C_{GS} decreases as gate bias increases and doping concentration has a very small effect on the gate capacitor.

In this chapter, we have extended the work of Murray et al. in which they have calculated analytical expressions for C_{GS} and C_{GD} by taking into account only three regions underneath the Schottky barrier gate. In their calculation, they ignored the extension of the depletion towards the drain side of the gate, which could have a significant contribution in charge accumulation, especially in submicron devices. This discrepancy of Murray expressions has been addressed by dividing the Schottky barrier depletion layer in four distinct regions as illustrated in Figure 4.1. In the figure, Region-IV describes the extension of the depletion layer towards ungated drian side of the device, and it holds charges Q_{IV} as shown in the figure. Capacitors C_{GS} and C_{GD} are evaluated and compared with III Region model and tangible improvement, especially in the magnitude of C_{GD} is noted.

The remaining composition of the chapter is that Section 4.2 deals with charge evaluation in different regions of the Schottky barrier depletion layer and its variation as a function of applied bias. Section 4.3 describes Miller capacitors assessment and Section 4.4 compares the assessed values of Miller capacitors with the experimental data. Finally, Section 4.5 summarizes the conclusions drawn from this research.

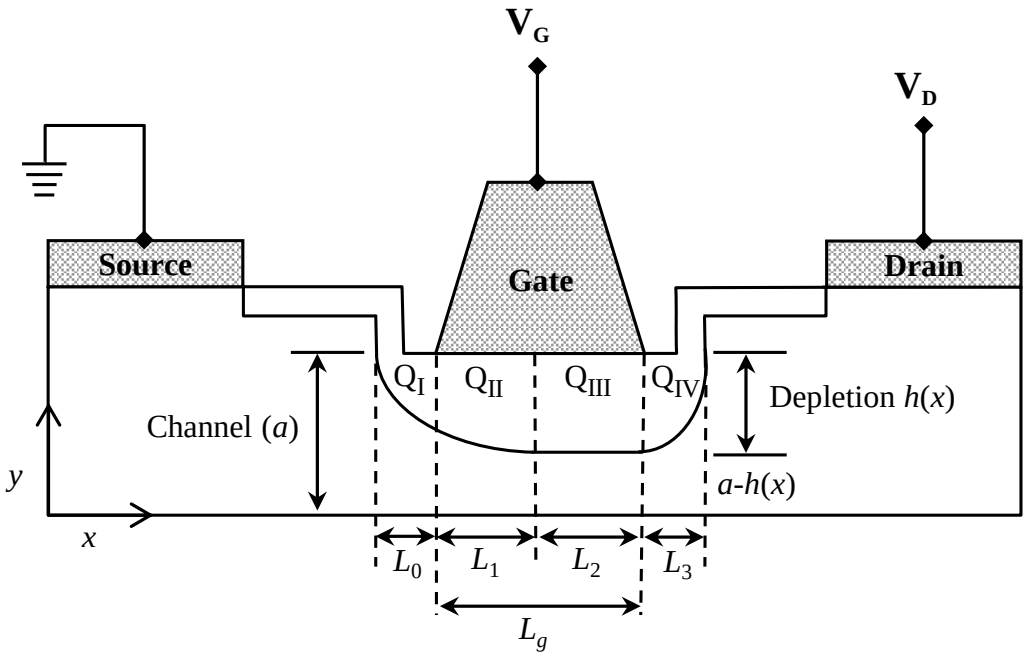

FIGURE 4.1: An operating MESFET with four distinct charge regions of the depletion layer: Region-I is defined by L_0; Region-II is defined by L_1: Region-III is defined by L_2 and finally, Region-IV is defined by the length L_3.

4.2 Charge Evaluation

To calculate charge underneath the Schottky barrier gate of a FET, one needs basic $I-V$ expression, which governs the current flow of the device. Under the applied field E, drain current, I_D can be written as [192].

$$I_D = qWN\mu(E)E(x)\left[a - h(x)\right] \tag{4.1}$$

where $h(x)$ is the depletion layer height, a represents epi-layer thickness of the device as shown in Fig. 4.1, q is the electronic charge, W is the device width, N is the doping density of epi-layer and $\mu(E)$ represents mobility of carriers, which can be defined as [10, 193].

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 E}{v_s}\right)^{\beta}\right]^{1/\beta}} \tag{4.2}$$

In above expression, μ_0 represents low field mobility, v_s is the saturation velocity of carriers and $\beta \approx 1$ is a fitting parameter. Equation (4.2) shows that μ is a function of applied field and typically it follows a bell shaped profile when plotted against the increasing values of E. Reduction in the magnitude of μ at relatively increased E is predominantly associated with increased scattering caused by the high amplitude lattice phonon.

Figure 4.1 shows a crossectional view of an operating FET, wherein $L_g = L_1 + L_2$ represents metallic part of the Schottky barrier gate, whilst L_0 and L_3 show extension in depletion region towards source and drain sides of the Schottky barrier gate, respectively. This constitutes a four regions depletion of the Schottky barrier and the charges in each region are represented by Q_{I} to Q_{IV}, respectively. At a given bias, $I_{D(\mathrm{lin})}$ and $I_{D(\mathrm{sat})}$ for linear and saturation region, respectively, is given as [137, 194].

$$I_{D(\mathrm{lin})} = I_P \left[\frac{3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3)}{1 + Z(u_d^2 - u_0^2)} \right] \tag{4.3}$$

$$I_{D(\mathrm{sat})} = qWN\gamma v_s a\,(1 - u_1) \tag{4.4}$$

In Eq. (4.4), $\gamma \approx 1$, a velocity saturation parameter that defines a smooth transition from the linear to the saturation region of operation. u_d and u_0 are normalized depletion layer heights towards drain and source side of the device, respectively. Variable u_1 also defines normalized depletion layer height but for location underneath the Schottky barrier gate where the carrier's velocity gets saturated. Normalized values of depletion layers as a function of applied bias are given as

$$u_d(V_G, V_D) = \sqrt{\frac{V_D + V_G + V_B}{V_P}}, \quad u_0(V_G) = \sqrt{\frac{V_G + V_B}{V_P}} \tag{4.5}$$

$$u_1(V_G, V_D) = \sqrt{\frac{V(L_1) + V_G + V_B}{V_P}} \tag{4.6}$$

where V_D and V_G are the drain and gate potentials, respectively, V_B represents built-in potential, V_P pinch-off voltage and $V(L_1)$ is the potential under the gate, across the length L_1. Other variables of Eqs. (4.3) and (4.4) are given as

$$I_P = \frac{q^2 N^2 \mu_0 W a^3}{6\epsilon_s L_g}, \quad V_P = \frac{qNa^2}{2\epsilon_s}, \quad Z = \frac{qNa^2\mu_0}{2\epsilon_s L_g v_s} \tag{4.7}$$

where ϵ_s is the relative permittivity. Channel length, L_1 can be evaluated by using Eqs. (4.3) and (4.4), and is given as [98].

$$L_1 = L_g Z \left[\frac{(u_1^2 - u_0^2) - (2/3)(u_1^3 - u_0^3)}{\gamma(1 - u_1)} - (u_1^2 - u_0^2) \right] \tag{4.8}$$

Potential drop at location L_1 can be assessed by applying Poisson's equation on two dimensional distribution of charges underneath the Schottky barrier depletion as shown in Fig. 4.1. By involving device physical variables and appropriate boundary conditions, it can be shown that [98]

$$V\left(L_g, u_1 a\right) = V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi\left(L_g - L_1\right)}{2au_1}\right] \tag{4.9}$$

where E_s represents saturation field. The first part of Eq. (4.9) represents potential drop in the region defined by L_1; whereas, the second part of this expression represents potential drop in the region L_2. Also from Fig. 4.1, it is obvious that $L_2 = L_g - L_1$ so

$$\begin{aligned} V\left(L_1\right) &= V_P\left(u_1^2 - u_0^2\right) \quad \text{and} \\ V(L_2) &= \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_2}{2au_1}\right] \end{aligned} \tag{4.10}$$

It is obvious from Fig. 4.1 that $V(L_0) = V_P u_0^2$ is the potential, which is caused by $V_G + V_B$. Using quarter circle approximation, L_3 can be approximated as $L_3 \approx L_g/4$ [98] resulting into

$$V(L_3) \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_3}{2au_1}\right] \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_g}{8au_1}\right] \tag{4.11}$$

So, the potential distribution across the Schottky barrier gate caused by V_D will be $V(L_0)+V(L_1)+V(L_2)+V(L_3)=V_D$, which can be written as

$$V_P u_0^2 + V_P\left(u_1^2-u_0^2\right)+\frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi\left(L_g-L_1\right)}{2au_1}\right]+\frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_g}{8au_1}\right]=V_D \tag{4.12}$$

4.2.1 For Region-I

As shown in Fig. 4.1, the length of Region-I, which is represented by L_0, has the corresponding accumulation of charges shown as Q_{I}. For this region using quarter circle approximation [136], the magnitude of Q_{I} can be expressed as

$$Q_{\mathrm{I}} \approx \frac{\pi}{4}\epsilon_s W u_0^2 V_P \tag{4.13}$$

4.2.2 For Region-II

By considering the region represented by L_1 of Fig. 4.1, one can see that the charge accumulation in this region is represented by Q_{II}, which can be evaluated as

$$Q_{\mathrm{II}} \approx qNW\int_0^{L_1} h(x)dx \tag{4.14}$$

For given values of V_D and V_G, the magnitude of Q_{II} can be known by rearranging Eqs. (4.1) and (4.2)

$$I_D\left(dx+\frac{qN\mu_0}{v_s\varepsilon_s}h(x)dx\right)=qN\mu_0 W\frac{qN}{\varepsilon_s}h(x)\left[a-h(x)\right]dx$$

After simplification and comparison with Eq. (4.14)

$$Q_{\mathrm{II}}=\frac{I_P V_P}{I_D}\times\frac{4\varepsilon_s W L_g}{a}\left[\left(1-\frac{ZI_D}{3I_P}\right)\left(u_1^3-u_0^3\right)-\frac{3}{4}\left(u_1^4-u_0^4\right)\right] \tag{4.15}$$

Equation (4.15) shows that the charge accumulation in Region-II is dependent upon the device physical parameters such as (WL_g/a) as well as on the device bias potentials, which control u_0 and u_1.

4.2.3 For Region-III

By looking at Fig. 4.1, one can judge that the length of Region-III is defined by $L_2 = L_g - L_1$, where it is assumed that the depletion remains constant to define the constant crosssectional area for the saturation current. So, under such conditions, charge accumulated in Region-III can be represented as

$$Q_{\text{III}} = qNWh_1(L_g - L_1) = qNWau_1(L_g - L_1) \tag{4.16}$$

4.2.4 For Region-IV

Again on the basis of quarter circle approximation [98], the charge accommodation in Region-IV can be approximated as

$$Q_{\text{IV}} \approx \frac{\pi}{4}\epsilon_s W u_1^2 V_P \tag{4.17}$$

Equation (4.17) represents the magnitude of charges accumulated in Region-IV, which are dependent upon the physical parameters W and a of the device. The variable a is indirectly there because of V_P as evident from Eq. (4.7). This shows that the devices meant for high power and frequency applications; where W and V_P both are usually high, Q_{IV} will have a significant contribution and cannot be overlooked. Furthermore, when L_g of the device is small, Region-II and Region-III are bound to shrink as one can see from Figure 4.1 and for such devices, Region-IV shall have a pronounced effect in the evaluation of C_{GD} capacitor of the device.

So, the total charge under the Schottky barrier gate can be attained by combining charges given in Eqs. (4.13), (4.15), (4.16) and (4.17), i.e.

$$Q_{\text{T}} = Q_{\text{I}} + Q_{\text{II}} + Q_{\text{III}} + Q_{\text{IV}}$$

$$Q_{\mathrm{T}} = \frac{\pi}{4}\epsilon_s W u_0^2 V_P + \frac{4 I_P V_P \varepsilon_s W L_g}{a I_D}\left[\left(1 - \frac{Z I_D}{3 I_P}\right)(u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right] \tag{4.18}$$

$$+ qNWau_1(L_g - L_1) + \frac{\pi}{4}\epsilon_s W u_1^2 V_P$$

Knowing the charge distribution as given by Eq. (4.18), one can find Miller capacitors both for the linear as well as for the saturation region of operation of a FET. Since it involves the entire depletion layer underneath the gate it is, therefore, assumed that the respective capacitor evaluation thus, achieved will have better accuracy compared to two or three regions depletion models.

4.3 Gate-to-drain Capacitor, C_{GD}

4.3.1 Linear Region

To evaluate gate-to-drain capacitor, C_{GD}, one can differentiate Eq. (4.18) w.r.t V_D keeping V_G constant.

$$C_{GD}^{L} = \left.\frac{\partial Q_{\mathrm{T}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} + \left.\frac{\partial Q_{\mathrm{III}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} + \left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} \tag{4.19}$$

In the linear region near the drain side, carriers are moving below the saturation velocity, we can therefore, assume that there would be negligible tapering of the depletion to define Region-III and Region-IV. The entire depletion can be treated as a uniformly distributed layer underneath the Schottky barrier gate. Thus, L_1 in such a case would be defined by the entire gate length, i.e. $L_1 = L_g$ and the contribution of V_D in changing the depletion layer defining Q_{III} and Q_{IV} would be negligible, therefore

$$Q_{\mathrm{III}} \approx Q_{\mathrm{IV}} \approx 0$$

In such a scenario, depletion layer underneath the Schottky barrier gate will have contribution made by the charges $Q_{\rm I}$ and $Q_{\rm II}$ alone, which are defined by Eqs. (4.13) and (4.15), respectively.

$$C_{GD}^{L} = \left.\frac{\partial Q_{\rm I}}{\partial V_D}\right|_{V_{G=\rm Cons}} + \left.\frac{\partial Q_{\rm II}}{\partial V_D}\right|_{V_{G=\rm Cons}}$$

Differentiating Eqs. (4.13) and (4.15) w.r.t V_D and using $u_1 = u_d$ and $L_1 = L_g$ yields

$$\left.\frac{\partial Q_{\rm I}}{\partial V_D}\right|_{V_{G=\rm Cons}} = 0 \quad \text{and}$$

$$\frac{\partial Q_{\rm II}}{\partial V_D} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{DL}}{I_D}\left\{(u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right\} + \frac{3u_d}{2V_P}\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\right]$$

where $\partial I_{D(\rm lin)}/\partial V_D = G_{DL}$, which is the output conductance for the linear region. So, C_{GD}^{L} for the linear region can be expressed as

$$C_{GD}^{L} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{DL}}{I_D}\left\{(u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right\} + \frac{3u_d}{2V_P}\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\right] \tag{4.20}$$

This expression gives variation in C_{GD}^{L} as a function of device and bias parameters. It shows that the magnitude of C_{GD}^{L} is directly proportional to (WL_g/a), which is the crossectional area defining the flow of current. This implies that by decreasing the available crossectional area, there is a decrease in the C_{GD}^{L}. A decrease in the crossectional area would mean that there is an extension in the height of depletion region caused by the applied potential. This explains the dependence of C_{GD}^{L} on the device bias potential.

4.3.2 Saturation Region

In the saturation region of operation, the Miller capacitor is denoted by C_{GD}^{S}, which can be defined as

$$C_{GD}^{S} = \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} + \left.\frac{\partial Q_{\mathrm{III}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} + \left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_D}\right|_{V_G=\mathrm{Cons}} \tag{4.21}$$

It is worth mentioning that the charge Q_{I}, as discussed before, is primarily caused by V_G, which therefore, will not contribute in defining C_{GD}^{S}. Equation (4.21) has three parts and the first part of this expression can be evaluated by involving Eq. (4.15), which gives

$$\begin{aligned}\frac{\partial Q_{\mathrm{II}}}{\partial V_D} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\Bigg\{\frac{-G_{DS}}{I_D}\left((u_1^3-u_0^3)-\frac{3}{4}(u_1^4-u_0^4)\right)\\ +\frac{3u_1}{2V_P}\left(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\right)\Gamma(V_G,V_D)\Bigg\}\end{aligned} \tag{4.22}$$

where $\partial I_{D(\mathrm{sat})}/\partial V_D = G_{DS}$, which represents output conductance for the saturation region. Now starting from Eq. (4.4) and by differentiating Eq. (4.12) w.r.t V_D keeping V_G constant and by involving Eqs. (4.6) and (4.8), the function $\Gamma(V_G, V_D)$ of Eq. (4.22) can be derived as

$$\begin{aligned}\Gamma(V_G,V_D) = \Bigg[1+\frac{E_s a}{\pi u_1 V_P}\Bigg\{\sinh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)-\frac{\pi}{2a}\cosh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)\\ \Bigg\{L_g Z\left(\frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2}+2u_1\frac{1-\gamma}{\gamma}\right)+\frac{L_g-L_1}{u_1}\Bigg\}\\ +\sinh\left(\frac{\pi L_g}{8au_1}\right)-\frac{\pi L_g}{8au_1}\cosh\left(\frac{\pi L_g}{8au_1}\right)\Bigg\}\Bigg]^{-1}\end{aligned} \tag{4.23}$$

The second part of Eq. (4.21) can be assessed using Eq. (4.16)

$$\frac{\partial Q_{\rm III}}{\partial V_D} = qNWau_1\left(-\frac{\partial L_1}{\partial V_D}\right) + qNWa\left(L_g - L_1\right)\frac{1}{2u_1V_P}\Gamma(V_G, V_D) \tag{4.24}$$

and by using Eq. (4.8), one can write

$$\frac{\partial L_1}{\partial V_D} = \frac{L_g Z\Gamma(V_G, V_D)}{V_P}\left[\left(\frac{(u_1^2 - u_0^2) - \frac{2}{3}(u_1^3 - u_0^3)}{2\gamma u_1(1-u_1)^2}\right) + \frac{1-\gamma}{\gamma}\right] \tag{4.25}$$

Combining Eqs. (4.24) and (4.25), we get

$$\frac{\partial Q_{\rm III}}{\partial V_D} = \frac{\varepsilon_s W L_g}{au_1}\Gamma(V_G, V_D)\chi(V_G, V_D) \tag{4.26}$$

where the function $\chi(V_G, V_D)$ is defined as

$$\chi(V_G, V_D) = \left[1 - \frac{L_1}{L_g} - Zu_1\left\{\frac{(u_1^2 - u_0^2) - \frac{2}{3}(u_1^3 - u_0^3)}{\gamma(1-u_1)^2} + 2u_1\left(\frac{1-\gamma}{\gamma}\right)\right\}\right] \tag{4.27}$$

Finally, to find the contribution of $Q_{\rm IV}$ towards C_{GD}^S, Eq. (4.17) is employed, where

$$\frac{\partial Q_{\rm IV}}{\partial V_D} = \frac{\pi}{4}\epsilon_s W\frac{\partial V(L_1)}{\partial V_D} = \frac{\pi}{4}\epsilon_s W\Gamma(V_G, V_D) \tag{4.28}$$

Now by combining Eqs. (4.21), (4.22), (4.26) and (4.28), final expression for C_{GD}^S is obtained as

$$C_{GD}^S = \Gamma(V_G, V_D)\left[\frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{DS}}{\Gamma(V_G, V_D)I_D}\left((u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right)\right.\right.$$
$$\left.\left. + \frac{3u_1}{2V_P}\left(1 - u_1 - \frac{Z}{3}\frac{I_D}{I_P}\right)\right\} + \frac{\varepsilon_s W L_g}{au_1}\chi(V_G, V_D) + \frac{\pi}{4}\epsilon_s W\right] \tag{4.29}$$

Equation (4.29) represents C_{GD}^S as a function of device physical as well as bias parameters. Usually, microwave devices are operated in the saturation region of operation therefore, Eq. (4.29) will play a crucial role in determining the device

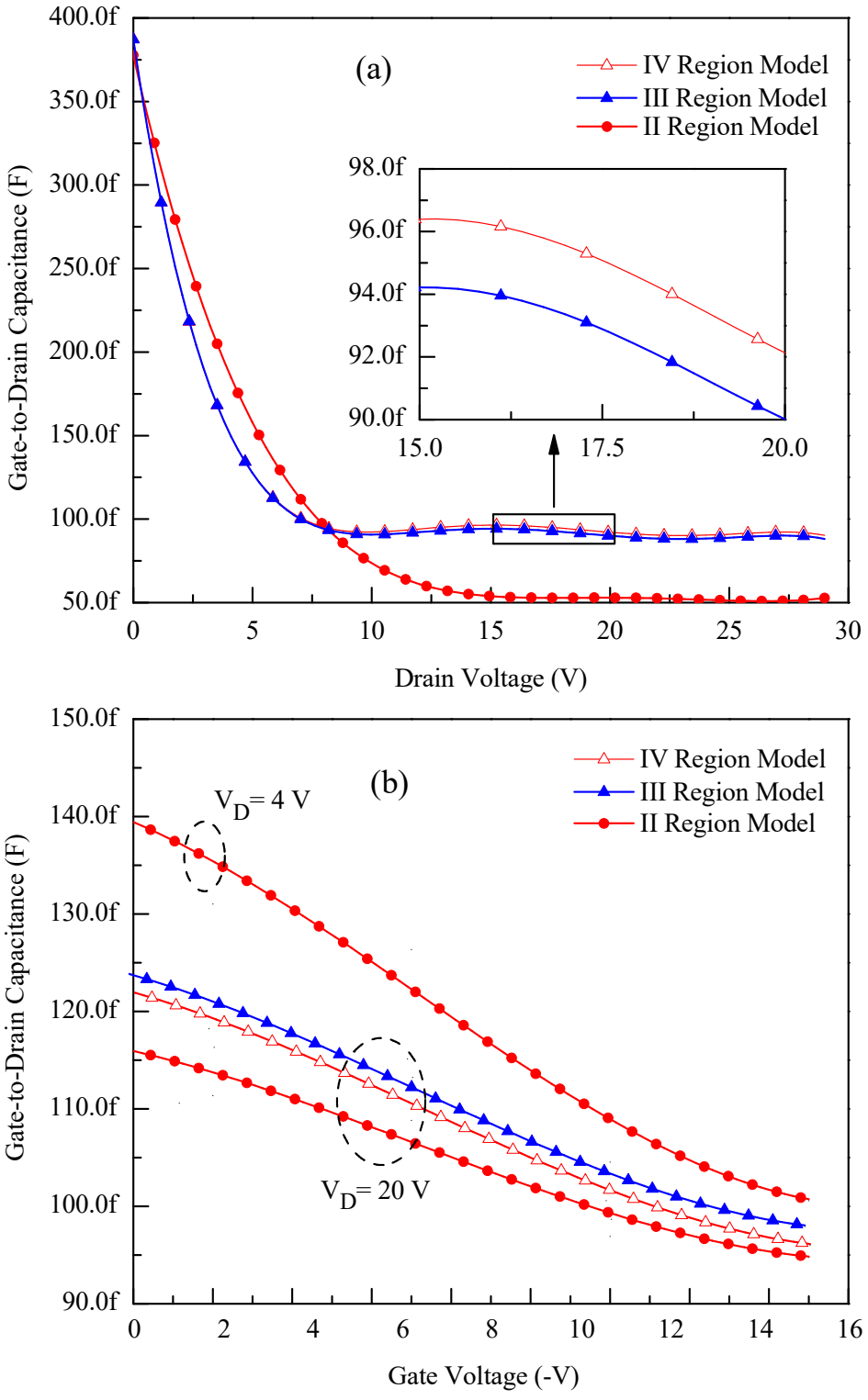

FIGURE 4.2: Variation in gate-to-drain capacitor (C_{GD}) for both linear and saturation regions of operation of a MESFET having $W = 500\ \mu$m, $L_g = 0.5\ \mu$m, $a = 0.3\ \mu$m and $N = 2.79 \times 10^{23}\ \text{m}^{-3}$; (a) as a function of drain bias (b) as a function of gate bias.

high frequency response. It is pertinent to mention here that Eq. (4.29) has been evaluated comprehensively by involving all possible regions underneath the Schottky barrier gate. It is, therefore, assumed that it should provide a better accuracy in assessing C_{GD}^{S} of a finished device as a function of applied bias. It is pertinent to mention here that for II Region model, $Q_{\rm II} + Q_{\rm III}$ are considered, for III Region model, $Q_{\rm I} + Q_{\rm II} + Q_{\rm III}$ are used, whereas for IV Region model, $Q_{\rm I} + Q_{\rm II} + Q_{\rm III} + Q_{\rm IV}$ are used to assess the respective Miller capacitors.

Figure 4.2 shows variation in C_{GD} as a function of V_D and V_G for a submicron MESFET. Figure 4.2(a) represents C_{GD} for both linear and saturation region of operation of a microwave MESFET. Moreover, it is pertinent to mention that the figure represents II, III and IV Region depletion layer models discussed in the preceding paragraphs. The figure exhibits a sharp decline in the magnitude of C_{GD} with increasing values of V_D for various models under discussion. This decline is primarily associated with increased depletion layer width as a function of V_D, which causes an increased separation between the charges defining the depletion layer capacitor. Examination of the figure also shows that there is a significant difference in the magnitude of C_{GD} for II Region depletion layer model relative to III and IV Region models. This is so, because the II Region depletion layer model to assess C_{GD} is a simplified model and it ignores the extension of depletion towards the drain and source side of the device. Apparently, III and IV Region models provide almost a similar C_{GD} vs. V_D profile; however, a zoomed view of Fig. 4.2(a), shown in the inset of the figure, revealed that there is a difference in the assessed values of C_{GD} for III and IV Region models. In some cases, this could meaningfully contribute in assessing the correct high frequency response of a microwave FET.

Figure 4.2(b) is plotted to represent once again variation in C_{GD} capacitor but in this case as a function of V_G. This figure is plotted using Eqs. (4.20) and (4.29) wherein, a relatively lower drain voltage value, i.e. $V_D = 4$ V is taken as a constant potential to represent linear region of operation, whilst $V_D = 20$ V represents saturation region of operation. In the linear region of operation, all the models under discussion have same response therefore, only one curve is shown at

$V_D = 4$ V; whereas, at $V_D = 20$ V, the plot shows an independent response of each model. Lowest values are observed for II Region model, whilst highest values are for III Region model. However, the profile of the plot at $V_D = 20$ V is identical for all the three models under evaluation.

4.4 Gate-to-source Capacitor, C_{GS}

4.4.1 Linear Region

Keeping in view the crossectional view of the depletion layer shown in Fig. 4.1, it is obvious that linear region capacitor, C_{GS}^{L} is defined by those regions of the depletion layer, which are identified as Q_{I} and Q_{II}. Therefore, one can write C_{GS}^{L} as

$$C_{GS}^{L} = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} \tag{4.30}$$

Differentiating Eq. (4.13) w.r.t V_G while keeping V_D constant, we can write value of the capacitor associated with Region-I as

$$\left.\frac{\partial Q_{\mathrm{I}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} = \frac{\pi}{4}\epsilon_s W \tag{4.31}$$

In writing Eq. (4.31), quarter circle approximation is assumed. Now using the definition of Q_{II} as given by Eq. (4.15) and combining it with Eq. (4.5) and by replacing $u_1 = u_d$, we can have

$$\frac{\partial Q_{\mathrm{II}}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{ML}}{I_D}\left((u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right)\right.$$

$$\left. +3u_d^2\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_d}{\partial V_G} - 3u_0^2\left(1 - u_0 - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_0}{\partial V_G}\right\}$$

where $\partial u_d/\partial V_G = 1/2u_d V_P$, $\partial u_0/\partial V_G = 1/2u_0 V_P$ and $\partial I_{D(\mathrm{lin})}/\partial V_G = G_{ML}$, so combining the above expression with Eqs. (4.30) and (4.31)

$$C_{GS}^{L} = \frac{\pi}{4}\epsilon_s W + \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{ML}}{I_D}\left((u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right)\right.$$
$$\left. + \frac{3}{2V_P}(u_d - u_0)\left(1 - \frac{Z}{3}\frac{I_D}{I_P}\right) - \frac{3}{2V_P}\left(u_d^2 - u_0^2\right)\right\} \tag{4.32}$$

where G_{ML} is the transconductance in the linear region of operation. Equation (4.32) represents variation in C_{GS}^{L} as a function of device applied bias. It clearly shows a significant contribution of Region-I in defining the magnitude of C_{GS}^{L}.

4.4.2 Saturation Region

In the saturation region of operation, gate-to-source capacitor, C_{GS}^{S} will be defined by the sum of charges marked as Q_{I}, Q_{II}, Q_{III} and Q_{IV} in Fig. 4.1, and is given by

$$C_{GS}^{S} = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} + \left.\frac{\partial Q_{\mathrm{III}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} + \left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} \tag{4.33}$$

Equation (4.33) is comprised of four terms. First term has the same definition as that of Eq. (4.31); whereas, the 2$^{\mathrm{nd}}$ term of Eq. (4.33) can be evaluated by differentiating Eq. (4.15) w.r.t V_G keeping V_D constant

$$\frac{\partial Q_{\mathrm{II}}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{MS}}{I_D}\left((u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right)\right.$$
$$\left. + 3u_1^2\left(1 - u_1 - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_1}{\partial V_G} - 3u_0^2\left(1 - u_0 - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_0}{\partial V_G}\right\} \tag{4.34}$$

where

$$\frac{\partial u_1}{\partial V_G} = \frac{1}{2u_1 V_P}\left(\frac{\partial V(L_1)}{\partial V_G} + 1\right)$$

For writing Eq. (4.34), we also used $\partial u_0/\partial V_G = 1/(2u_0 V_P)$ and $\partial I_{D(\mathrm{sat})}/\partial V_G = G_{MS}$, which represents transconductance in the saturation region of operation.

To evaluate potential $V(L_1)$ at the location where carriers are attaining the saturation velocity, we can differentiate Eq. (4.12) w.r.t V_G while keeping V_D constant

$$\frac{\partial V(L_1)}{\partial V_G} = -\left[\frac{1}{2u_0} + \frac{E_s a}{\pi u_1 V_P}\left\{\sinh\left(\frac{\pi(L_g - L_1)}{2au_1}\right) - \cosh\left(\frac{\pi(L_g - L_1)}{2au_1}\right)\right.\right.$$
$$\frac{\pi}{2a}\left\{L_g Z\left(\frac{(u_1^2 - u_0^2) - \frac{2}{3}(u_1^3 - u_0^3)}{\gamma(1-u_1)^2} - \frac{2u_1(u_1 - u_0)}{\gamma(1-u_1)}\right) + \frac{1}{u_1}(L_g - L_1)\right\}$$
$$\left.\left. + \sinh\left(\frac{\pi L_g}{8au_1}\right) - \frac{\pi L_g}{8au_1}\cosh\left(\frac{\pi L_g}{8au_1}\right)\right\}\right] \Gamma(V_{GS}, V_{DS}) = \Psi(V_{GS}, V_{DS}) \tag{4.35}$$

Combining Eqs. (4.34) and (4.35), we have

$$\frac{\partial Q_{\rm II}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{MS}}{I_D}\left((u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right) + \frac{3u_1}{2V_P}\right.$$
$$\left.\left(1 - u_1 - \frac{Z}{3}\frac{I_D}{I_P}\right)\left(\Psi(V_{GS}, V_{DS}) + 1\right) - \frac{3u_0}{2V_P}\left(1 - u_0 - \frac{Z}{3}\frac{I_D}{I_P}\right)\right] \tag{4.36}$$

Now to have the contribution in C_{GS}^S by the third part of charges referred to as $Q_{\rm III}$ in Eq. (4.33), we can differentiate Eq. (4.16) w.r.t V_G keeping V_D constant, which generates

$$\left.\frac{\partial Q_{\rm III}}{\partial V_G}\right|_{V_{D=\rm Cons}} = qNWa\left\{\frac{L_g - L_1}{2u_1 V_P}\left(\Psi(V_{GS}, V_{DS}) + 1\right) - u_1\left(\frac{\partial L_1}{\partial V_G}\right)\right\} \tag{4.37}$$

In writing the above expression, use of Eq. (4.35) is made. By combining Eqs. (4.8), (4.27) and (4.35) we have

$$\frac{\partial L_1}{\partial V_G} = \frac{L_g Z}{V_P}\left\{\frac{\chi(V_{GS}, V_{DS}) - 1 + \frac{L_1}{L_g}}{2Zu_1^2}\left(\Psi(V_{GS}, V_{DS}) + 1\right) - \frac{1-\gamma}{\gamma} - \frac{(u_1 - u_0)}{\gamma(1-u_1)}\right\} \tag{4.38}$$

This gives a final version of Eq. (4.37) as

$$\left.\frac{\partial Q_{\mathrm{III}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} = \frac{2\varepsilon_s W L_g Z u_1}{a}\left[\left(\frac{1-\frac{\chi(V_{GS},V_{DS})}{2}-\frac{L_1}{L_g}}{Z u_1^2}\right)\Big(\Psi(V_{GS},V_{DS})+1\Big) + \frac{1-\gamma}{\gamma}+\frac{(u_1-u_0)}{\gamma(1-u_1)}\right] \tag{4.39}$$

Fourth and the final part of the depletion layer, which contributes in the definition of C_{GS}^{S}, can be assessed by differentiating Eq. (4.17) w.r.t V_G keeping V_D constant

$$\left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} = \frac{\pi\epsilon_s W}{4}\left(\frac{\partial V(L_1)}{\partial V_G}+1\right) \tag{4.40}$$

Substituting the value of $\left(\frac{\partial V(L_1)}{\partial V_G}\right)$ from Eq. (4.35) into Eq. (4.40), we have

$$\left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_G}\right|_{V_{D=\mathrm{Cons}}} = \frac{\pi\epsilon_s W}{4}\Big[1+\Psi(V_{GS},V_{DS})\Big] \tag{4.41}$$

Combining Eqs. (4.31), (4.36), (4.39) and (4.41), we arrived at Eq. (4.42).

$$\begin{aligned} C_{GS}^{S} = {} & \frac{\pi}{4}\epsilon_s W + \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{MS}}{I_D}\Big((u_1^3-u_0^3)-\frac{3}{4}(u_1^4-u_0^4)\Big)\right. \\ & \left. +\frac{3u_1}{2V_P}\Big(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\Big)\Big(\Psi(V_{GS},V_{DS})+1\Big)-\frac{3u_0}{2V_P}\Big(1-u_0-\frac{Z}{3}\frac{I_D}{I_P}\Big)\right] \\ & +\frac{2\varepsilon_s W L_g Z u_1}{a}\left[\left(\frac{1-\frac{\chi(V_{GS},V_{DS})}{2}-\frac{L_1}{L_g}}{Z u_1^2}\right)\Big(\Psi(V_{GS},V_{DS})+1\Big)+\frac{1-\gamma}{\gamma}\right. \\ & \left. +\frac{(u_1-u_0)}{\gamma(1-u_1)}\right]+\frac{\pi\epsilon_s W}{4}\Big[1+\Psi(V_{GS},V_{DS})\Big] \end{aligned} \tag{4.42}$$

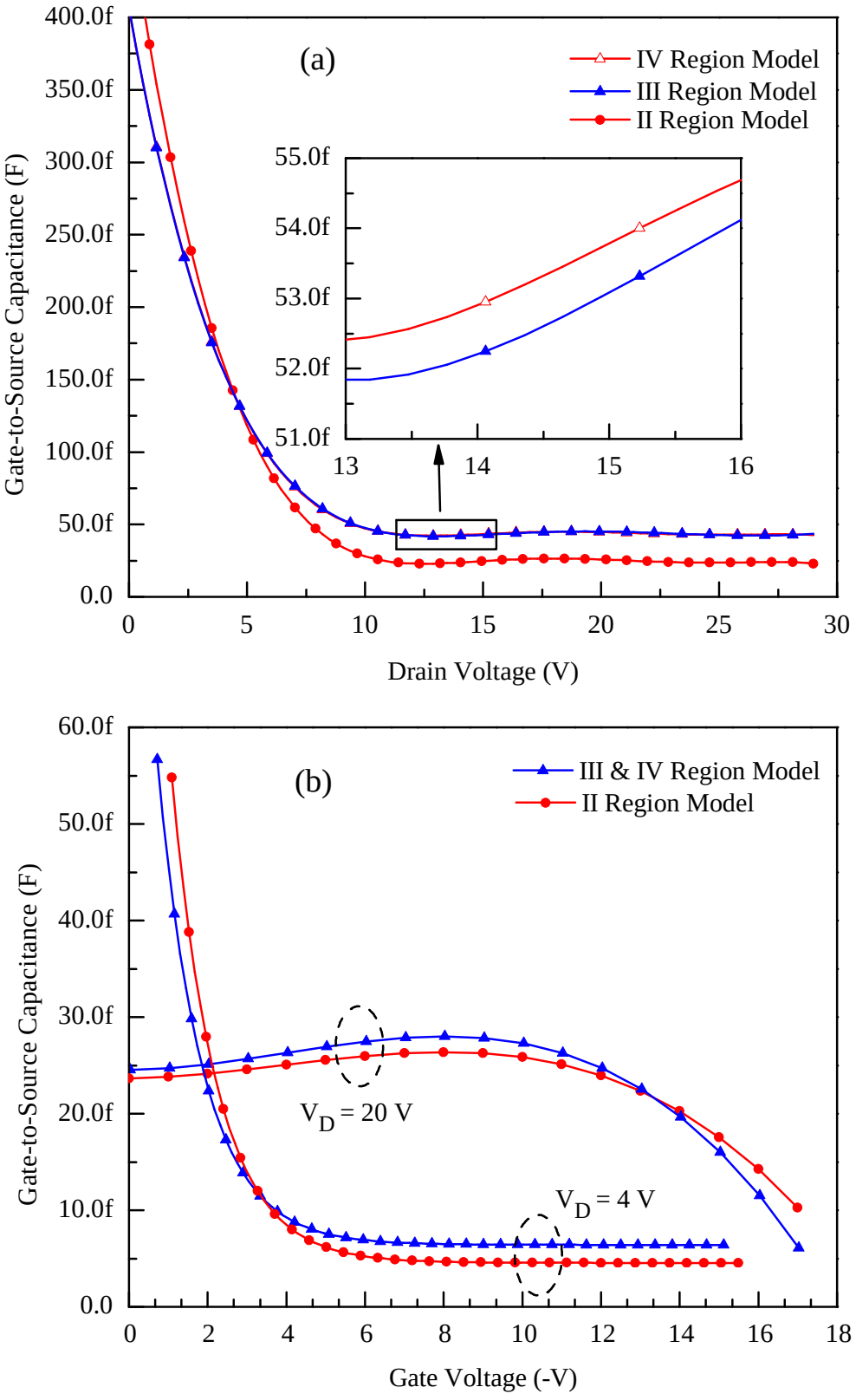

FIGURE 4.3: Variation in gate-to-source capacitor (C_{GD}) for both linear and saturation regions of operation of a MESFET having $W = 500\ \mu$m, $L_g = 0.5\ \mu$m, $a = 0.3\ \mu$m and $N = 2.79 \times 10^{23}\ \text{m}^{-3}$; (a) as a function of drain bias (b) as a function of gate bias.

This equation represents C_{GS}^{S} of the proposed four region model and its variation as a function of V_D and V_G as shown in Fig. 4.3(a) and 4.3(b), respectively. Careful examination of Fig. 4.3(a) reveals that II Region model, after the onset of current saturation, gives lower values of C_{GS}^{S} compared to III and IV Region models, whilst the difference between III and IV Region models in estimating C_{GS}^{S} is nominal, which is shown in the inset of Fig. 4.3(a). On the other hand, Fig. 4.3(b) represents C_{GS} for linear, that is $V_D = 4$ V plots, as well as for saturation region of operation, that is $V_D = 20$ V plots. It is pertinent to mention here that at $V_D = 20$ V, plots maintain almost a straight profile for a reasonable variation in V_G and then they exhibit a decline with increasing magnitude of V_G. A decline in the values of C_{GS}^{S} after $V_G = -8$ V, as evident from Fig. 4.3(b), could be associated with an increased depletion width caused by the applied V_G.

4.5 Discussion

To check the accuracy of the proposed IV Region Miller capacitors model in contrast to other models, Figs. 4.4 and 4.5 have been plotted, wherein experimental data of a submicron SiC MESFET is compared for C_{GD} and C_{GS} capacitors, respectively. It can be seen from Fig. 4.4 that the proposed IV Region model gives better fit to experimental data compared to other two models. As expected, III Region model is better than II Region model; whereas, IV Region model maps the experimental data with reasonable accuracy both as a function of V_{DS} and V_{GS}.

Figure 4.5 gives experimental and evaluated values of C_{GS} as a function of drain and gate bias. One can see from the figure that the behavior of III and IV Region models are identical and closed to the experimental data, whilst II Region model shows a significant deviation. Identical response of III and IV Region models in assessing C_{GS} is understandable because Region-IV, shown in Fig. 4.1, contributes only in C_{GD} resulting into an identical response of III and IV Region models in evaluating C_{GS} as evident from Figs. 4.5(a) and 4.5(b). Furthermore, improvement observed in assessing Miller capacitors using IV Region depletion

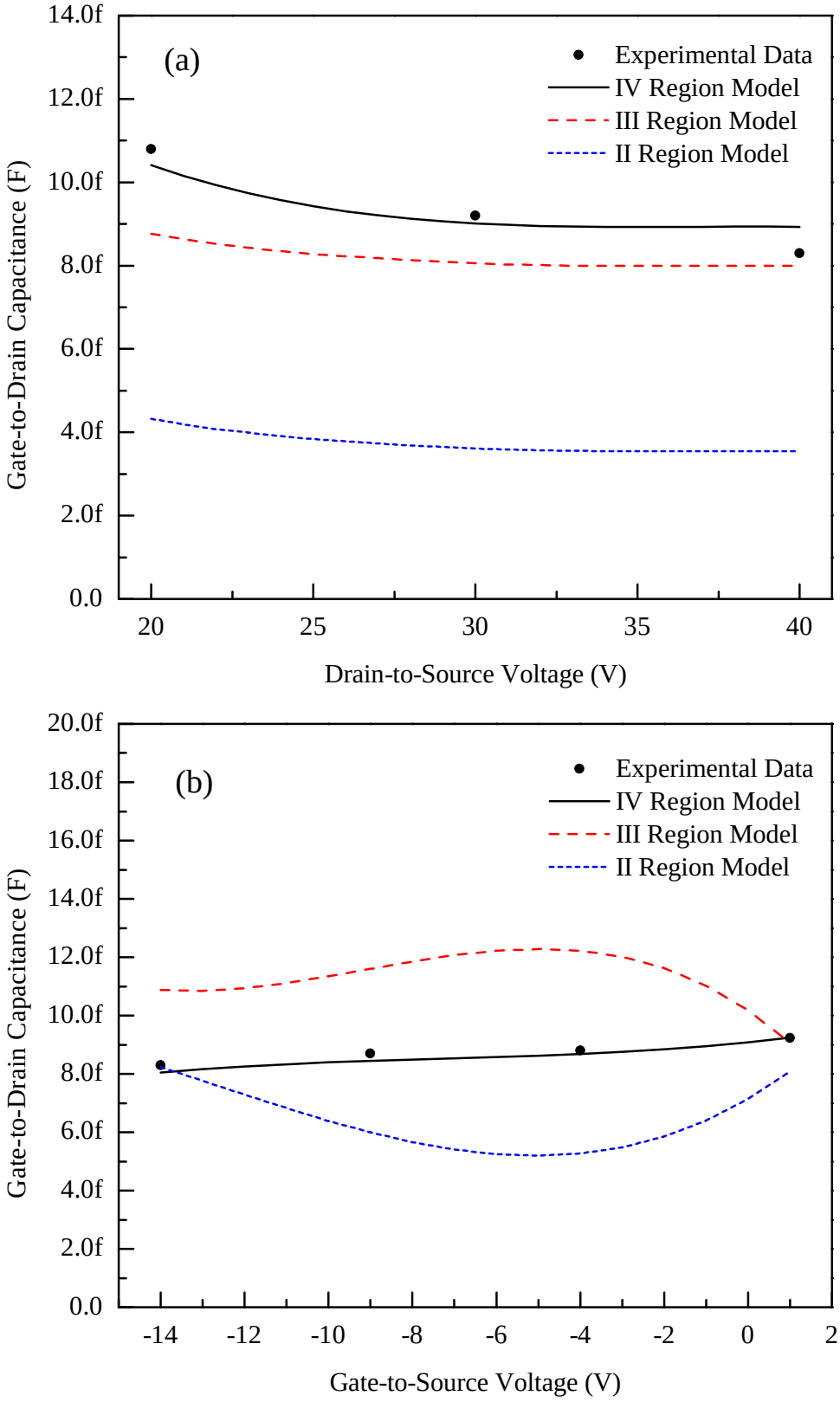

FIGURE 4.4: Gate-to-drain capacitor (C_{GD}) of a MESFET having $W = 500\ \mu$m, $L_g = 0.5\ \mu$m, $a = 0.3\ \mu$m and $N = 2.79 \times 10^{23}\ \text{m}^{-3}$; (a) as a function of drain bias (b) as a function of gate bias. Experimental data from Ref. [203].

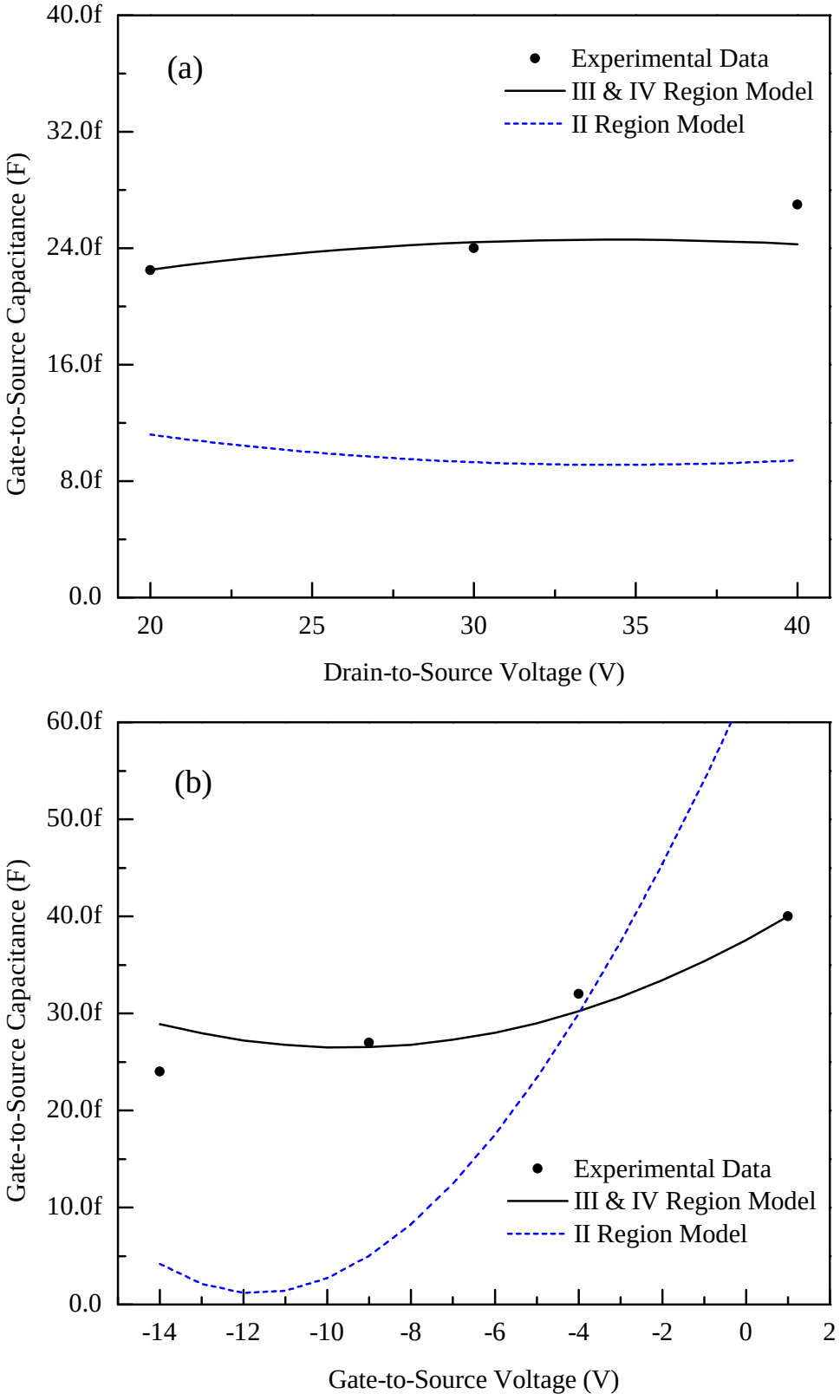

FIGURE 4.5: Gate-to-source capacitor (C_{GS}) of a MESFET having $W = 500\ \mu$m, $L_g = 0.5\ \mu$m, $a = 0.3\ \mu$m and $N = 2.79 \times 10^{23}\ \text{m}^{-3}$; (a) as a function of drain bias (b) as a function of gate bias. Experimental data from Ref. [203].

TABLE 4.1: Root mean square error (RMSE) in SiC MESFET C_{GS} and C_{GD} capacitors values evaluated using different depletion regions as illustrated in Fig. 4.1. The least RMSE for each case is shown in bold face.

Model	RMSE ($\times 10^{-8}$) w.r.t V_{DS}		RMSE ($\times 10^{-8}$) w.r.t V_{GS}	
	C_{GS}	C_{GD}	C_{GS}	C_{GD}
II Region	9.51	5.86	12.9	2.45
III Region	**1.06**	1.45	**1.31**	2.74
IV Region	**1.06**	**0.44**	**1.31**	**0.19**

layer model has been summarized in Table 4.1, wherein it is shown that there is 69% and 93% improvement in RMSE while assessing C_{GD} as a function of V_{DS} and V_{GS}, respectively, relative to III Region model.

4.6 Summary

In this chapter, an analytical model has been developed to assess Miller capacitors of a FET by distributing the depletion layer underneath the Schottky barrier gate of the device into four distinct regions. Region-I of the depletion is its extension towards the source side of the gate other than the Schottky barrier metal; whereas, Region-II starts from the Schottky metal to the point where the carriers' velocity gets saturated, and from this point to the end of the Schottky metal gate, the depletion layer is represented by Region-III. Finally, Region-IV is defined by the extension of the depletion towards the drain side of the device. Analytical expressions have been developed to assess the linear as well as the saturation region gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitors. It has been shown that three region analytical model to assess Miller capacitors, especially C_{GD} of the device reduces its accuracy because, it does not take into account accurately Region-IV of the device, which plays a crucial role in defining the Miller capacitors. The proposed technique exhibited 69% and 93% improvement in RMSE while assessing C_{GD} as a function of V_{DS} and V_{GS}, respectively, relative to III Region model when compared with the experimental data.

Chapter 5

Substrates Effects on FET's AC Parameters

5.1 Introduction

In this chapter, a comparison has been made by evaluating small signal equivalent circuit of GaN based HEMTs fabricated upon Si and SiC substrates. It is worth mentioning here that in the last few decades, heterostructure devices are gaining attention due to their superior characteristics in high power, frequency and temperature applications. Heterostructure devices, such as AlGaN/GaN and AlN/GaN/AlGaN high electron mobility transistors (HEMTs) have been used due to their intrinsic material and structure properties, such as high carrier mobility, $\mu \sim 1500$ cm^2/Vsec, high breakdown voltage ~ 3.3 MV/cm and high saturation velocity, $\upsilon_{sat} \sim 2.5\times10^7$ m/sec [100]. It is worth mentioning that commercially available GaN HEMTs are fabricated on silicon (Si) and silicon carbide (SiC) substrates. HEMTs fabricated on SiC substrate have demonstrated efficient power performance [204, 205], because of their low substrate losses and higher thermal conductivity. But, SiC substrate is extremely costly relatively to Si. Thus, Si substrate for GaN/AlGaN HEMTs fabrication could be an alternative solution due to its low cost [206]. However, Si substrate has low resistivity, which may induce

higher substrate losses [207]. This in turn could possibly restrict the performance of HEMT on Si, especially for microwave power applications.

For microwave power applications, HEMTs are operated at relatively high bias where the properties of chosen substrate play an important role in defining the small signal modeling (SSM) of the transistor. This is a crucial part for a reliable RF and microwave circuit design. For SSM, usually two methods are employed to extract small signal parameters.

(1) Evaluation of both extrinsic and intrinsic parameters by using an appropriate analytical approach [152, 153].

(2) Evaluation of the device extrinsic as well as intrinsic parameters through measured S-parameters by using an optimization algorithm [154].

In [208, 209], the authors applied Genetic Algorithm (GA) on 22 and 20 elements based equivalent circuit model of GaN HEMT, respectively. In 22 elements model [208], the authors introduced parasitic capacitors and conductors for better extraction of intrinsic small signal parameters. While in [209], the authors modified the conventional equivalent circuit model of HEMT by introducing extra pad capacitors, which are in series with gate, C_{PG} and drain, C_{PD} capacitors, and also placed parallel resistors for improved extraction of intrinsic parameters through GA. The circuit model presented in [209] was also used for reliable and efficient extraction of small and large signal parameters of GaN-on-Si and GaN-on-SiC substrates [210]. They modeled the substrate charging effects, which were evaluated by the external bypass RC circuits at the gate and drain sides. The elements of presented circuit were extracted from measured S-parameters under pinch-off and unbiased conditions.

Using Particle Swarm Optimization (PSO), Majumdar et al. [211] presented an improved technique for GaN HEMT to extract small signal parameters. On the other hand, the authors of Ref. [212] presented an efficient methodology for HEMT small signal parameter extraction. In their technique initially, extrinsic parameters were extracted using experimental S-parameters of a cold FET. The values

obtained from the experimental measurements of GaN-Si/SiC HEMTs were used as a primary source of reference for optimization process using PSO. Subsequently, by employing a de-embedding technique, intrinsic small signal parameters of a GaN HEMT were assessed.

In 2016, Sahoo et al. [110] presented a SSM of AlN/GaN/AlGaN HEMT on Si and SiC substrates. In their model, they considered substrate losses by using the analogy of transmission line losses. Through measured S-parameters, they presented the effects of Si and SiC substrates for high frequency performance of the device. Their study concluded that SiC substrate is a preferred substrate for GaN based HEMTs and offer substantially better performance than the devices fabricated using Si substrate.

5.2 AC Equivalent Circuits and Parameters Extraction

AC equivalent circuit model of an HEMT with substrate distributed components as proposed by [110] is shown in Fig. 5.1(a), while the conventional equivalent circuit is shown in Fig. 5.1(b). In the extrinsic part of Fig. 5.1(a), C_{PG} and C_{PD} are the pad capacitors of gate and drain, respectively. R_G, R_S and R_D denote gate, source and drain resistances, respectively; while, L_G, L_S and L_D represent gate, source and drain inductances, respectively. The substrate model consisting of C_{sub} and G_{sub} is implemented on gate and drain terminals; whereas, G_{epi} represents conductance through epi-layer of the transistor. In the intrinsic part of Fig. 5.1(a), the elements C_{GS}, C_{GD} and C_{DS} represent gate-to-source, gate-to-drain and drain-to-source capacitances, respectively. R_I, R_{GD} and R_{DS} denote channel, gate-to-drain and drain-to-source resistances, respectively. Finally, I_M is a current source, which represents response of the device after onset of current saturation. The elements C_{sub}, G_{epi} and G_{sub} are used in the model to evaluate the effect of substrate on the AC performance of HEMT device. Figure 5.1(b) shows the conventional device equivalent circuit model. In this model, the extra

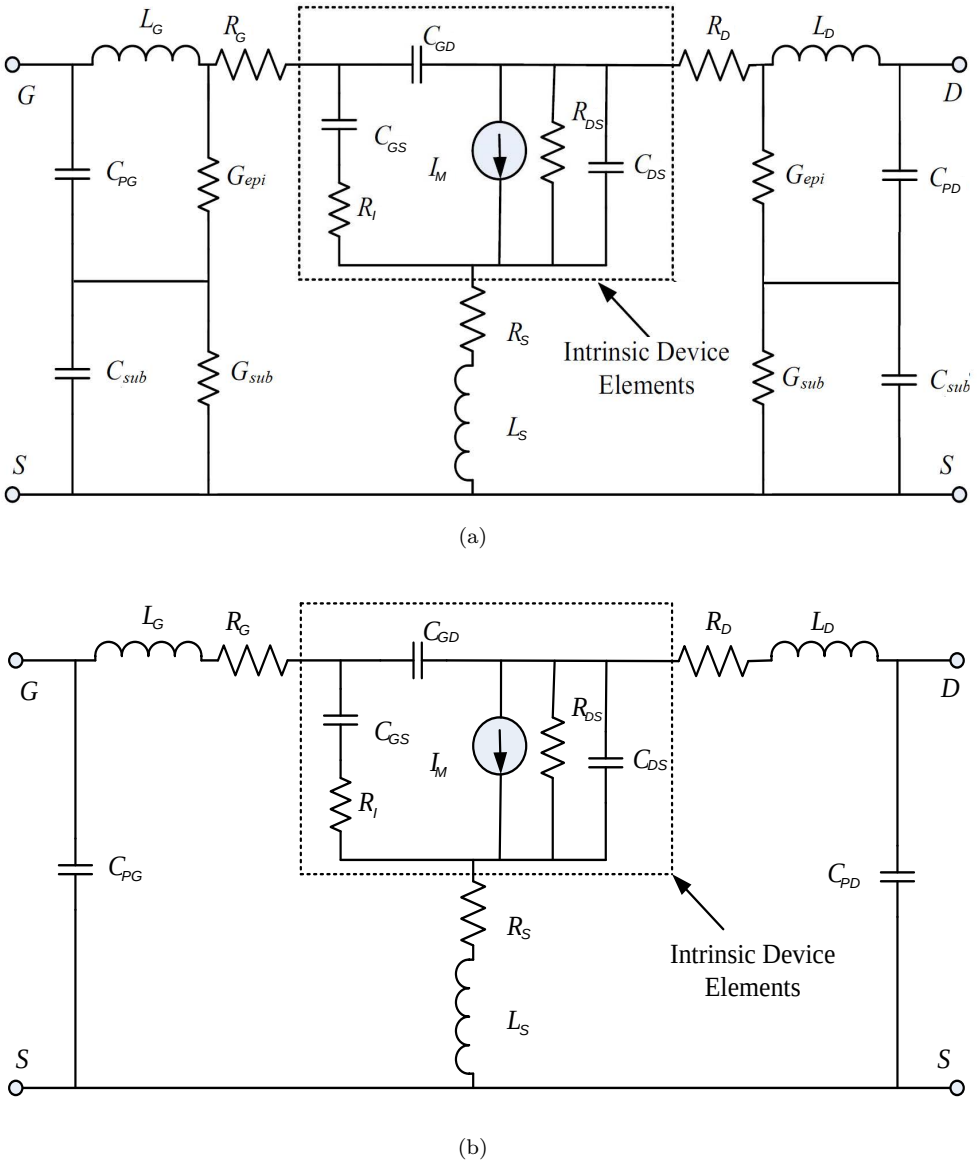

FIGURE 5.1: Small signal equivalent circuit of a GaN/AlGaN HEMT (a) with substrate loss elements (b) conventional model.

substrate components are not used. Rest of the parameters are same as that of Fig. 5.1(a).

In Fig. 5.1(a, b), intrinsic components are bias dependent and characterize the active region underneath the gate, while extrinsic components are bias independent [29]. The intrinsic capacitances, such as C_{GS}, C_{GD} and C_{DS} play an important role in evaluating the AC behavior of the device. The magnitude of G_M is influenced by τ, which is gate depletion charging and discharging time. To achieve high gain and high speed, the value of G_M should be as high as possible and τ as low

as possible. R_{DS} generally explained in terms of its reciprocity, which is output conductance G_D. A low value of G_D is desired and ideally it should be zero.

The values of extrinsic parameters are technology and material dependent. For low noise performance, the values of R_S and R_G should be low, whereas R_D controls the breakdown voltage of the device, therefore, for high power devices $R_D > R_S$ to enhance the power handling capability of the device. Furthermore, L_S, L_G and L_D determine the source, gate and drain impedances as a function of frequency. Pad capacitances, as first approximation, are usually omitted due to their low magnitude relative to other intrinsic capacitances of the model.

It is a well known fact that the device operational capabilities are determined by its intrinsic parameters. However, extrinsic parameters should also be known because the external signal would reach or leave the device by involving its extrinsic components. Measured S-parameters will have the impact on both of these parameters. Thus, an appropriate de-embedding technique is required to approximate the device intrinsic small signal parameters by involving measured S-parameters [152]. According to [29], after transforming S-parameters into Y-parameters, the intrinsic parameters of a FET can be associated with Y-parameters as:

$$Y_{11} = \frac{j\omega C_{GS}}{1 + j\omega R_I C_{GS}} + j\omega C_{GD} \tag{5.1}$$

$$Y_{12} = -j\omega C_{GD} \tag{5.2}$$

$$Y_{21} = \frac{G_M e^{-j\omega\tau}}{1 + j\omega R_I C_{GS}} - j\omega C_{GD} \tag{5.3}$$

$$Y_{22} = G_D + j\omega(C_{DS} + C_{GD}) \tag{5.4}$$

Then the values of intrinsic parameters at a given frequency, ω_i can be assessed by using the following equations.

$$C_{GD}(\omega_i) = -\frac{Im(Y_{12})}{\omega} \tag{5.5}$$

$$C_{DS}(\omega_i) = \frac{Im(Y_{22})}{\omega} - C_{GD} \tag{5.6}$$

$$C_{GS}(\omega_i) = \frac{Im(Y_{11})}{\omega} - C_{GD} \tag{5.7}$$

$$G_D(\omega_i) = Re(Y_{22}) \tag{5.8}$$

$$G_M(\omega_i) = Re(Y_{21}) \tag{5.9}$$

$$R_I(\omega_i) = \frac{1 - \left(1 - \frac{4Re(Y_{11})}{\omega^2 C_{GS}^2}\right)}{Re(Y_{11})} \tag{5.10}$$

$$\tau(\omega_i) = -\frac{1}{\omega} tan^{-1} \frac{Im(G)}{Re(G)} \tag{5.11}$$

where

$$Im(G) = G_M e^{-j\omega\tau} = Re(Y_{21}) - Im(Y_{21}) R_I C_{GS} - \omega^2 C_{GD} C_{GS} R_I \tag{5.12}$$

and

$$Re(G) = Re(Y_{21}) R_I C_{GS} - Im(Y_{21}) - \omega C_{GD} \tag{5.13}$$

S-parameters can be obtained from the following equations.

$$S_{t11} = \frac{(Y_0 - Y_{11})(Y_0 + Y_{22}) + Y_{12} Y_{21}}{\Delta Y} \tag{5.14}$$

$$S_{t12} = \frac{-2Y_{12}Y_0}{\Delta Y} \tag{5.15}$$

$$S_{t21} = \frac{-2Y_{21}Y_0}{\Delta Y} \tag{5.16}$$

$$S_{t22} = \frac{(Y_0 + Y_{11})(Y_0 - Y_{22}) + Y_{12}Y_{21}}{\Delta Y} \tag{5.17}$$

where

$$\Delta Y = (Y_0 + Y_{11})(Y_0 + Y_{22}) + Y_{12}Y_{21} \tag{5.18}$$

where Y_0 is the admittance at 50 Ω.

5.3 Results And Discussion

A MATLAB code involving PSO was developed and a detail description of PSO is given in [213]. Following are the main steps involved in the implementation of PSO:

(1) initialize swarm dimensions, velocity and position;

(2) define experimental S-parameters and extrinsic parameters;

(3) define dependence of intrinsic parameters on Y-parameters using Eqs. (5.5) to (5.11);

(4) update velocity and position of each swarm particle;

(5) find personal best, p_{best} position of the particle;

(6) find global best, g_{best} position;

(7) convert Y-parameters into S-parameters using Eqs. (5.14) to (5.17);

(8) evaluate error using objective function defined by Eqs. (5.19) and (5.20);

TABLE 5.1: Values of extrinsic parameters of an HEMT used in PSO to assess intrinsic parameters.

Parameter	Values
R_G	5 Ω
L_G	35 pH
R_D	1.5 Ω
L_D	35 pH
R_S	0.5 Ω
L_S	2 pH

(9) update velocity and position with respect to p_{best} and g_{best};

(10) stop algorithm if minimum error is achieved or iterations are complete, otherwise go to Step (4).

To minimize the error, an objective function based on the magnitude and the phase of S-parameters is designed and given by:

$$\text{RMSE(mag)} = \sqrt{\frac{\sum_{i=1}^{n}\sum_{j,k=1}^{2}(SM_{jk}(w_i) - \overline{SM}_{jk}(w_i))^2}{\overline{SM}_{jk}(w_i)}} \leq \varepsilon \tag{5.19}$$

$$\text{RMSE(phase)} = \sqrt{\frac{\sum_{i=1}^{n}\sum_{j,k=1}^{2}(SP_{jk}(w_i) - \overline{SP}_{jk}(w_i))^2}{\overline{SP}_{jk}(w_i)}} \leq \varepsilon \tag{5.20}$$

where SM and SP represent experimental data while, $\overline{SM}$ and $\overline{SP}$ show simulated data for magnitude and phase, respectively. j, k represent individual S-parameters while i is the frequency variation. The variable ε defines the tolerance value and for an accurate evaluation, it should be as small as possible. By using extrinsic circuit parameters given in Table 5.1, PSO having swarm size of 50, was executed to get optimized intrinsic parameters for GaN/AlGaN HEMTs whose measured S-parameters both for Si and SiC substrates have been reported in Ref. [110] by using the equivalent circuit given in Fig. 5.1(a).

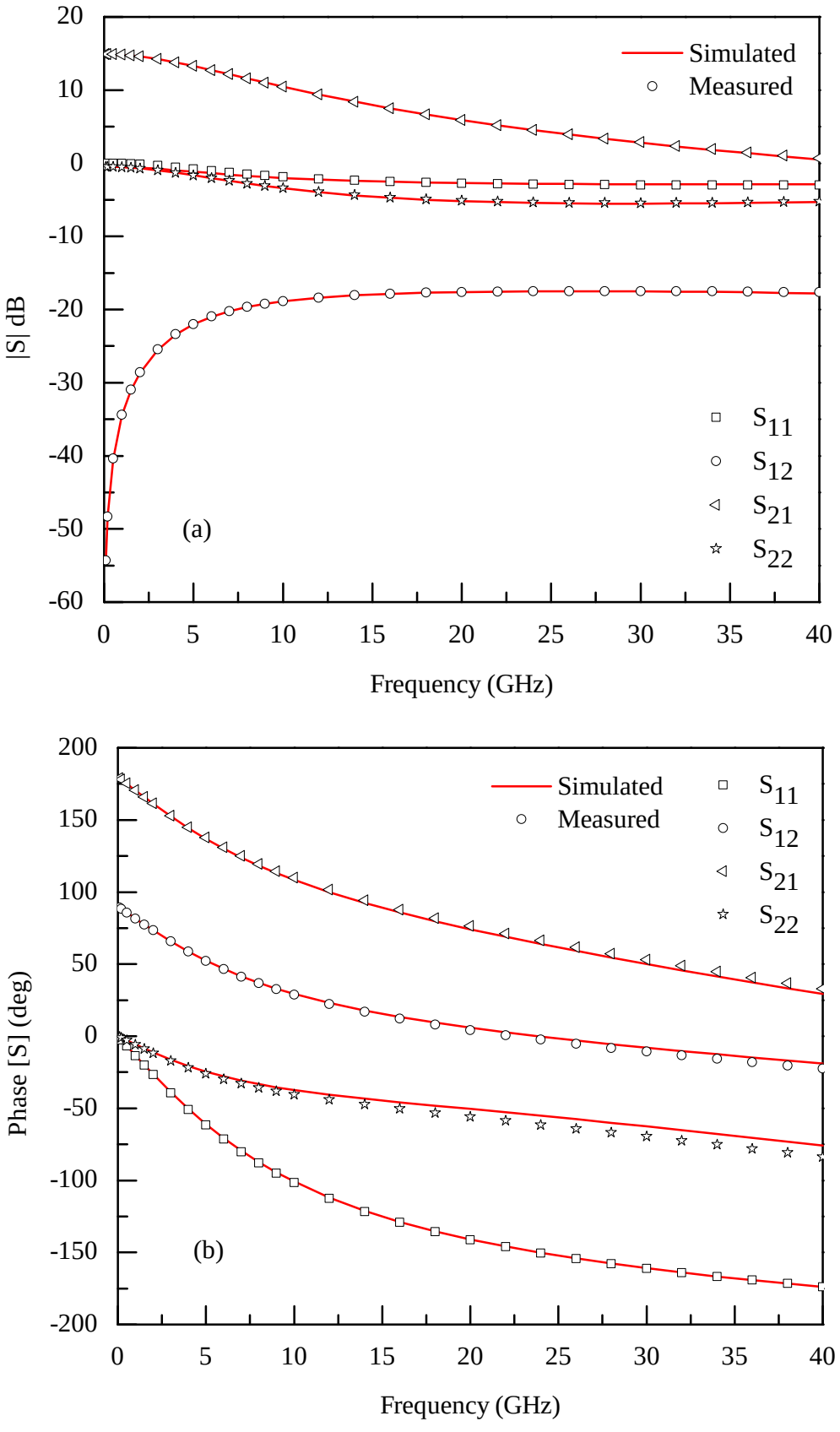

FIGURE 5.2: Measured and simulated S-parameters of a submicron GaN/AlGaN HEMT fabricated on Si substrate (a) magnitude (b) phase.

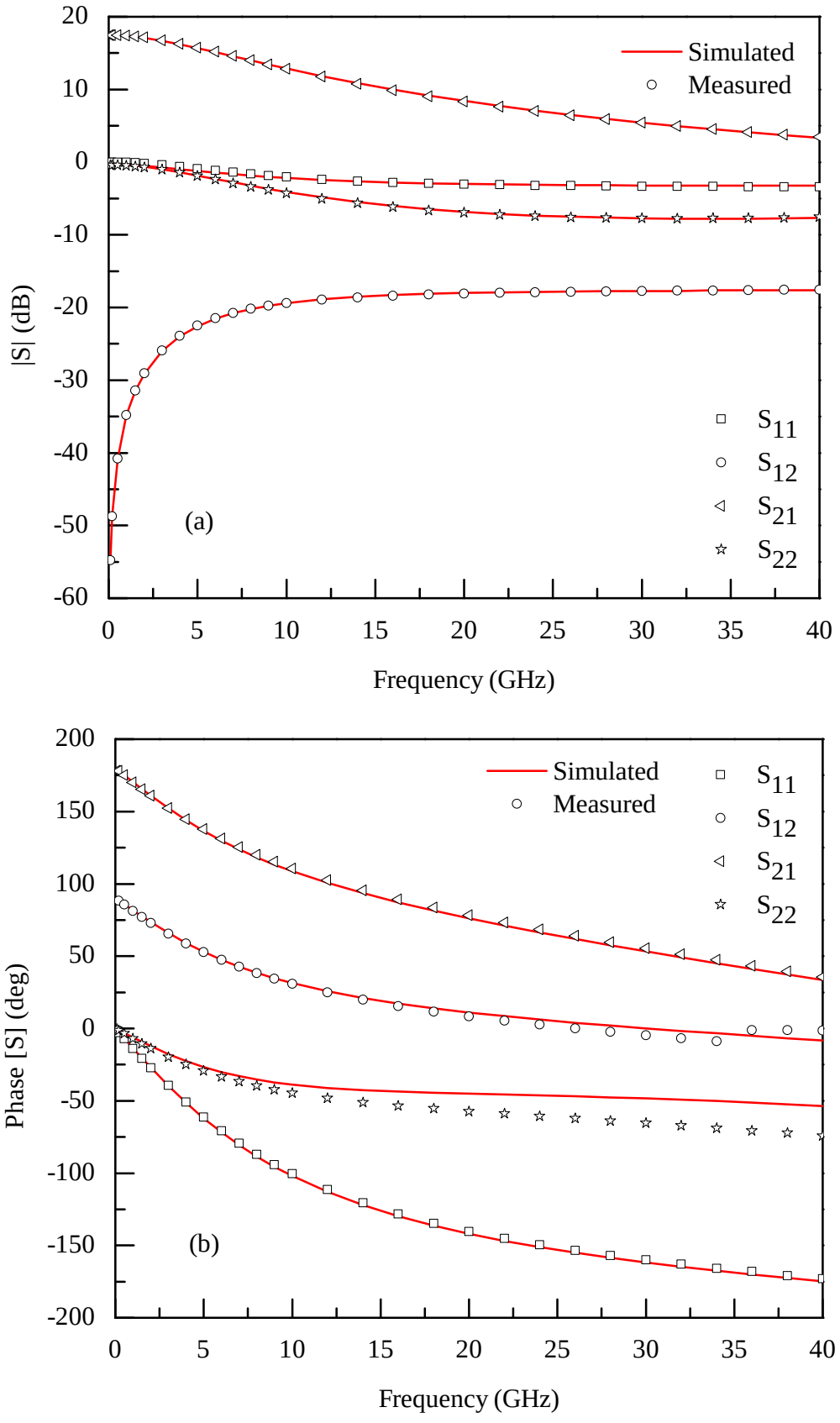

FIGURE 5.3: Measured and simulated S-parameters of a submicron GaN/AlGaN HEMT fabricated on SiC substrate (a) magnitude (b) phase.

Figure 5.2 shows measured and simulated S-parameters of a GaN/AlGaN HEMT assessed using equivalent circuit of Fig. 5.1(b). Some discrepancies are observed in Fig. 5.2(b), especially for S_{21} and S_{12} phases but by and large the simulation is in compliance with the experimental data. On the other hand, measured and simulated data of a device having same dimensions but on SiC substrate are shown in Fig. 5.3. Once again, the magnitude exhibited and exceptionally good fit but some discrepancies are there in measured and simulated phases of S-parameters as evident from Fig. 5.3(b).

Table 5.2 represents RMS error values for both the devices under discussion. Examining the data of the table, it is obvious that involving substrate distribution network as shown in Fig. 5.1(a), one would get some improvement both in the magnitude as well in the phase of simulated and observed S-parameters of the device. For Si-substrate, the table shows that on the average, the magnitude of error increases by considering equivalent circuit of Fig. 5.1(b) instead of Fig. 5.1(a) from 0.0354 to 0.0989 and in phase from 0.2724 to 0.5064. A similar pattern is also observed for the devices fabricated on SiC substrate. These values exhibit that the variation between two respective values is not that high and the observed improvement could be considered as marginal. Thus, a largely accepted equivalent circuit of GaN/AlGaN HEMT, shown in Fig. 5.1(b) is still accurate enough to demonstrate device characteristics at high frequency.

In Fig. 5.4, a comparison between measured and simulated insertion loss is provided for Si and SiC GaN/AlGaN HEMTs with and without substrate parameters. The insertion loss is calculated by using the following equation.

$$\text{Insertion Loss} = -20\log_{10}|S_{21}| \text{ (dB)} \tag{5.21}$$

It is evident from Fig. 5.4 that the insertion loss results for both the cases are in good agreement. A marginal change is observed for the cases in which substrate distributed network has been considered. This once again supported the idea that the inclusion of substrate distributed network increases the circuit complexity many fold but the advantages it gives are nominal. It is also observed from the

TABLE 5.2: Comparative analysis of RMS errors between measured and simulated S-parameters of submicron HEMTs fabricated on Si/SiC substrate.

Device	**S-Parameters**	**RMS Errors**				
		$\mathbf{S_{11}}$	$\mathbf{S_{12}}$	$\mathbf{S_{21}}$	$\mathbf{S_{22}}$	**Avg.**
Si substrate	Magnitude	0.0929	0.0113	0.0084	0.0229	0.0354
(With Distributed NW)	Phase	0.0353	0.1347	0.1358	0.7847	0.2724
Si substrate	Magnitude	0.0498	0.0528	0.1252	0.1678	0.0989
(Without Distributed NW)	Phase	0.1059	0.3199	0.8664	0.7366	0.5064
SiC substrate	Magnitude	0.0799	0.0125	0.0181	0.0466	0.0391
(With Distributed NW)	Phase	0.1352	0.0718	0.1298	1.8664	0.5502
SiC substrate	Magnitude	0.0615	0.0645	0.0987	0.1657	0.0976
(Without Distributed NW)	Phase	0.1619	0.2057	0.9757	1.1681	0.6277

figure that Si offers a relatively higher insertion loss than SiC substrate. This could be associated with the fact that Si substrate has low resistivity and thus, higher substrate losses. Furthermore, as expected, the substrate loss increases by increasing the frequency and the same behavior is exhibited by the plot of Fig. 5.4.

The extracted intrinsic parameters for both GaN/AlGaN-on-Si and GaN/AlGaN-on-SiC with and without substrate parameters are given in Table 5.3. These values are assessed using PSO technique discussed hitherto, which involved extrinsic parameters given in Table 5.1. From the data of Table 5.3, it is observed that the extracted parameters for both the cases are in good agreement with the technique given in Ref. [110] except the value of R_I. This shows that in the definition of intrinsic small signal parameters of the device the substrate has no or nominal effect. As far as the value of R_I is concerned, the same can be validated by using the expression $R_I = \upsilon_s L_g/3\mu I_{DS}$ [21], where L_g is the gate length of the device and I_{DS} is drain-to-source current. Using the device parameters, the value of $R_I = 0.34\ \Omega$, which is much closer to the value assessed by using PSO and given in Table 5.3.

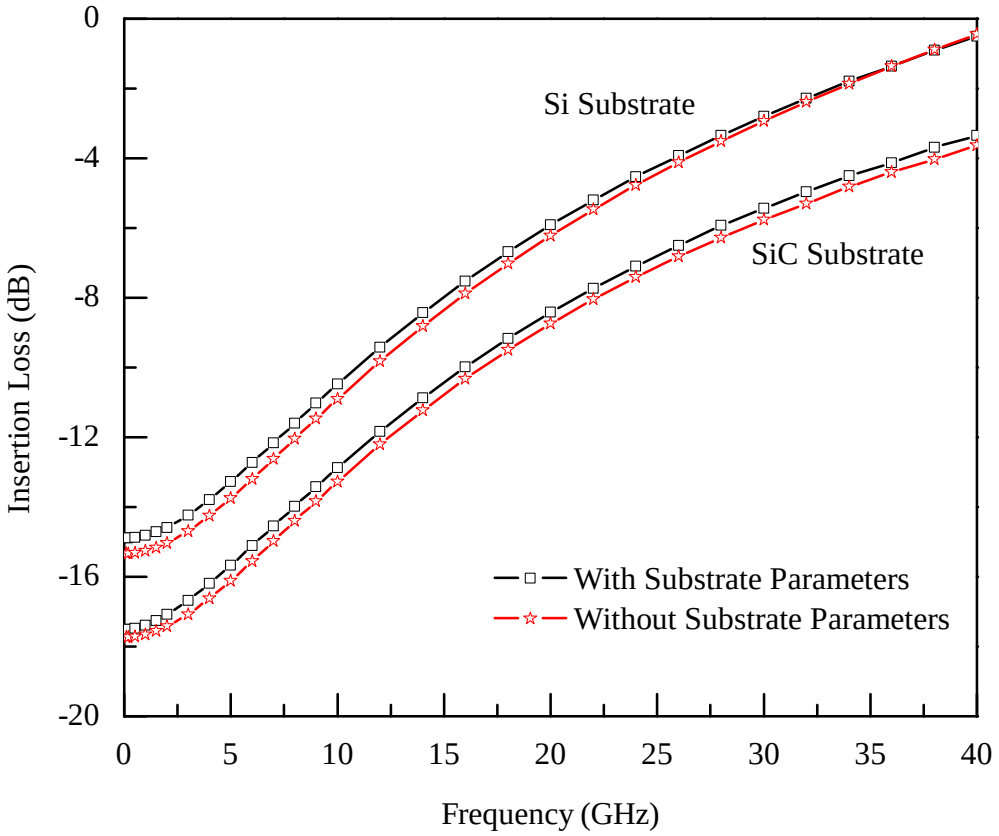

FIGURE 5.4: Insertion loss with and without substrate distributed network parameters of submicron HEMTs fabricated on Si and SiC substrates.

TABLE 5.3: Extracted intrinsic parameters of submicron HEMTs fabricated on Si and SiC substrates.

Parameters	With Distributed Elements [110]		Without Distributed Elements	
	Si Substrate	SiC Substrate	Si Substrate	SiC Substrate
R_I (Ω)	0.05	0.05	0.13	0.42
C_{GS} (fF)	255	230	252	227
C_{GD} (fF)	32	30	32	30
C_{DS} (fF)	31	27	31	27
G_M (mS)	60	80	60	81
τ (psec)	1.6	2.15	2.5	2.15

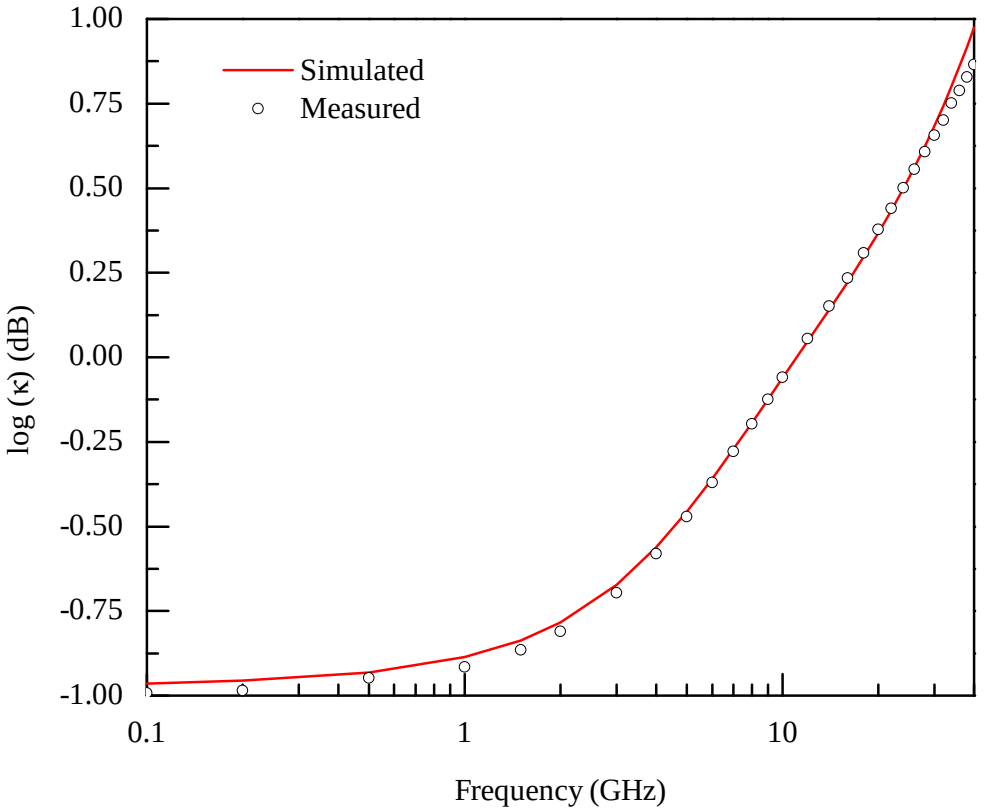

FIGURE 5.5: Plot of Rollet's stability factor, κ as function of frequency for a GaN/AlGaN HEMT fabricate on Si substrate.

To assess maximum stable gain (MSG), we can employ Eq. (5.22), which defines Rollet's stability factor, κ for values of S-parameters as

$$\kappa = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{5.22}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5.23}$$

Figure 5.5 shows variation of $\log(\kappa)$ as a function of frequency where $y = 0$ represents a point beyond that $\kappa > 1$. Thus, MSG as per the Rollet's criterion can be written as

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} \quad \text{when} \quad \kappa < 1 \tag{5.24}$$

For $\kappa > 1$, the maximum available gain (MAG) can be calculated by using the expression

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} \times \left(\kappa - \sqrt{\kappa^2 - 1}\right) \tag{5.25}$$

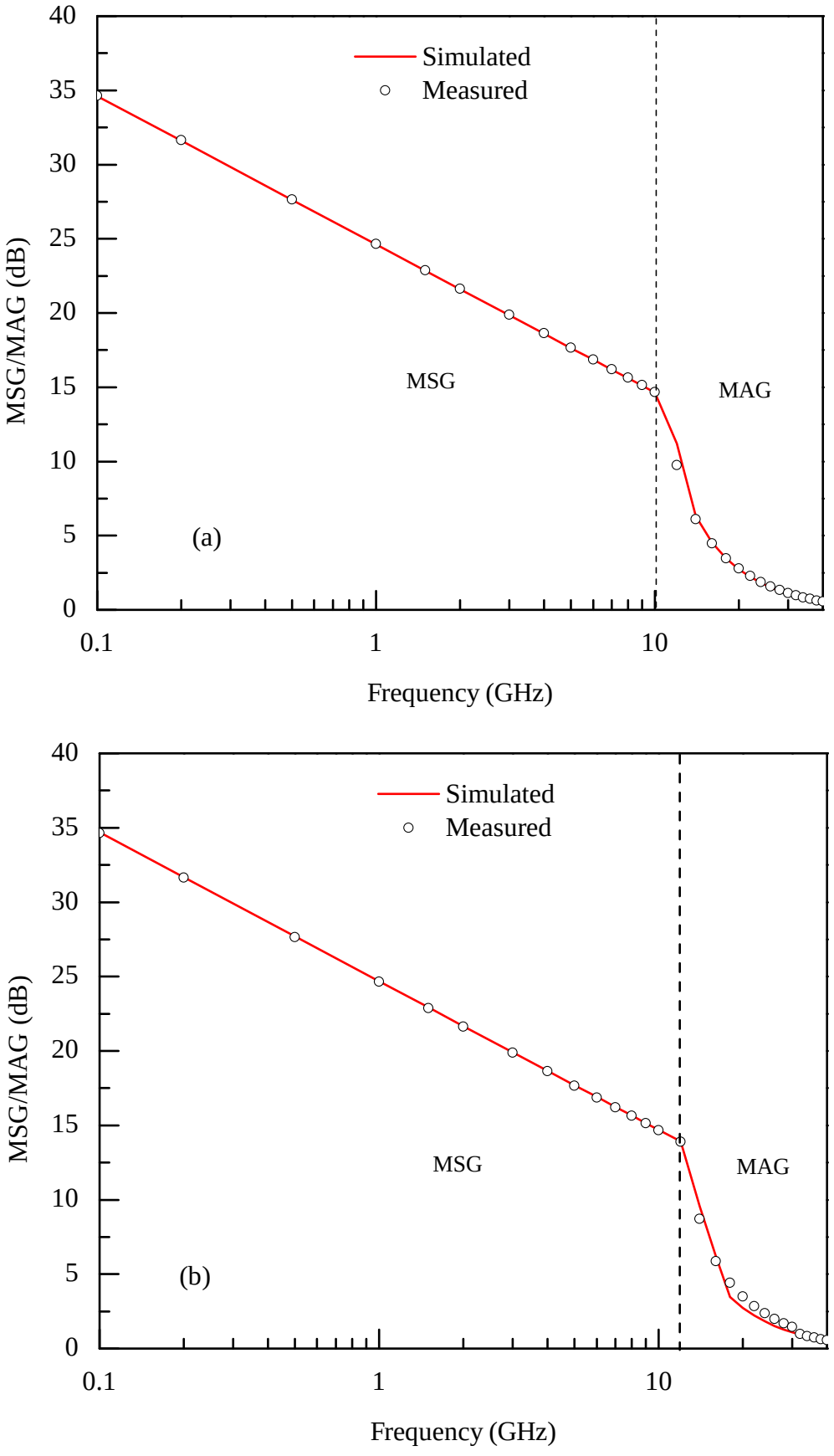

FIGURE 5.6: Maximum stable gain (MSG) and maximum available gain (MAG) of a submicron GaN/AlGaN HEMT fabricated on Si substrate assessed using (a) substrate distributed network shown in Fig. 5.1(a) and (b) without substrate distributed network Fig. 5.1(b).

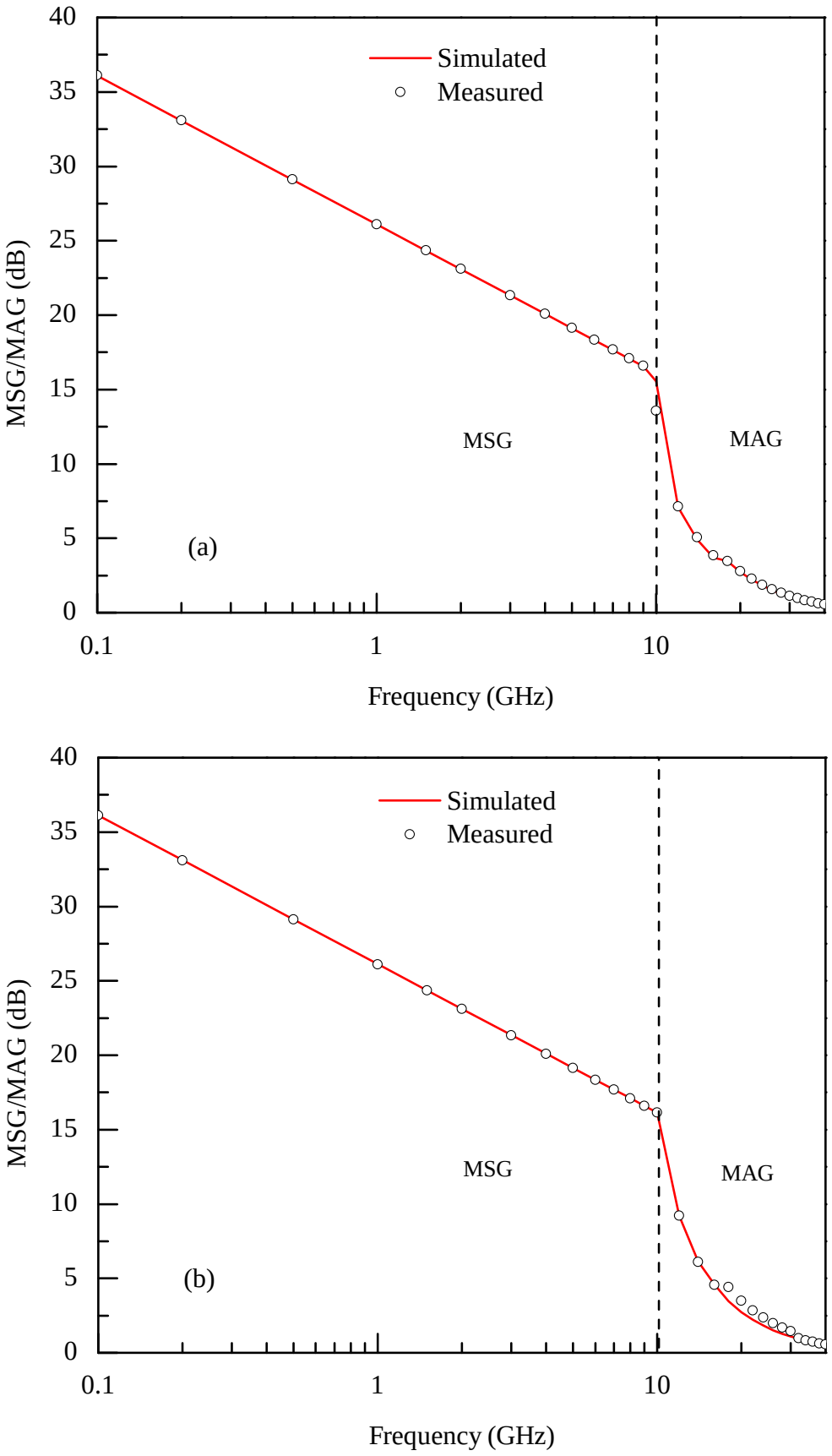

FIGURE 5.7: Maximum stable gain (MSG) and maximum available gain (MAG) of a submicron GaN/AlGaN HEMT fabricated on SiC substrate assessed using (a) substrted distributed network shown in Fig. 5.1(a) and (b) without substrate distributed network Fig. 5.1(b).

Figure 5.6 shows variation in MSG and MAG of a GaN/AlGaN-Si device. Figure 5.6(a) is attained using equivalent circuit given in Fig. 5.1(a) whereas, Fig. 5.6(b) represents the device gains using Fig. 5.1(b). It can be seen from the figure that there is no noticeable change in the performance of the device by using either of the circuit of Fig. 5.1. Therefore, once again it can be concluded that there is either no or nominal change in the assessed performance of the device by incorporating substrate distributed network as shown in Fig. 5.1(a). Since, this addition makes the calculation time consuming for an optimization software with little or no benefit thus, it can be avoided.

Gain frequency response of a submicron GaN/AlGaN-SiC HEMT is shown in Fig. 5.7. Simulation of Fig. 5.7(a) is attained using equivalent circuit of Fig. 5.1(a), whereas Fig. 5.7(b) modeled response is attained using the circuit of Fig. 5.1(b). Once again, we are constrained to state that the effects of substrate distributed network are very marginal and for practical applications can comfortably be ignored.

Furthermore, examining Figs. 5.6 and 5.7 juxtaposition, it can be said that devices fabricated on SiC substrates, which is an expensive substrate relative to Si, offer little advantages thus, for commercial and economical applications, Si might be a preferred substrate for GaN/AlGaN HEMTs fabrication.

5.4 Summary

Effects of silicon and silicon carbide substrates on the AC performance of a submicron AlN/GaN/AlGaN high electron mobility transistor are presented. Particle swarm optimization is used to extract intrinsic component values. Optimized intrinsic components are achieved using an objective function, which involves measured S-parameters. Sahoo et al's. modified circuit model with substrate losses is compared with the conventional model and it is observed that the extra substrate components have marginal or no impact on the device S-parameters. It

is further established that use of SiC substrate relative to Si offers little advantages as far as high frequency applications are concerned. Therefore, Si substrate could be employed for those applications where economical fabrication is a key consideration.

Chapter 6

Reliability of High Power FET's DC and AC Characteristics

6.1 Introduction

In this chapter, a modified model is presented to predict $I-V$ characteristics of submicron SiC MESFETs, including self-heating effects. It is shown that the modified model can predict the device characteristics with 48.46% improved accuracy compared to the best reported model [26].

SiC MESFETs can comfortably operate in the millimeter wavelength regime, showing power handling capability of $\sim$ 1 W/mm for continuous-wave operation and $\sim$ 2.5 W/mm for pulse input [214]. High-power applications of SiC MESFETs primarily depend on their material properties, which are summarized in Table 1.1. To allow the device to operate at microwave frequencies, an appropriate ratio between L_g and a, referred to as device aspect ratio (L_g/a), is considered to be a crucial design parameter. Reduction in L_g increases the high-frequency capabilities of the device but at the same time imposes stringent conditions on a, in terms of both its doping as well as its thickness to achieve good pinch-off without compromising the targeted drain current.

Short-channel SiC MESFETs offer high saturation velocity and high operating frequency but at the same time suffer from deterioration of the device characteristics, referred to as short-channel effects, among which the most common are [215]: (a) reduction in the device G_M; (b) increase in G_D, after the onset of current saturation; (c) shift in the device V_T, towards the negative side; and (d) reduction in the device V_{Br}. Short-channel effects can be controlled, to some extent, by optimizing the device channel and buffer layer structure underneath the channel [48, 77]. Hyuk et al. [216] demonstrated that short-channel effects can be reduced by having a thin but heavily doped channel. Song et al. [175] showed that a heavily doped p-type buffer allows the device to operate at relatively high power, and increasing the buffer layer thickness from 2.2 to 6 μm improves V_{Br} from 38 to 275 V.

When L_g of a MESFET is reduced to the submicron regime, intense heat generation occurs inside the channel because of the high electric field; resulting effects on the device characteristics are known as self-heating effects [80, 217]. it is obvious that, owing to its high thermal conductivity, MESFETs based on SiC have the capability to combat increased channel temperature while retaining their basic operation. However, the characteristics of the device may be modified [70] because the carriers become hot along with the lattice, thus affecting μ and crosssectional area of the channel $a-h(x)$, as shown in Fig. 6.1. Moreover, scattering of hot carriers into the buffer layers increases, and their subsequent collection by the drain defines a component of the drain current known as I_{sub}. Additionally, high drain and gate bias give rise to a strong y-directed electric field, which can potentially modify $h(x)$ by reducing its height, thus increasing $a - h(x)$ for the current flow, as shown in Fig. 6.1 [26, 218].

Simulation of $I - V$ characteristics of SiC MESFETs under different bias and ambient conditions, especially when $L_g < 1$ μm, has remained a challenging task for engineers working on device design. Numerous models have been reported in the literature, being routinely employed in simulation software packages to predict the $I - V$ characteristics of such devices [26, 111, 117, 119, 161]. These models are based on empirical or semiempirical modeling approaches, providing

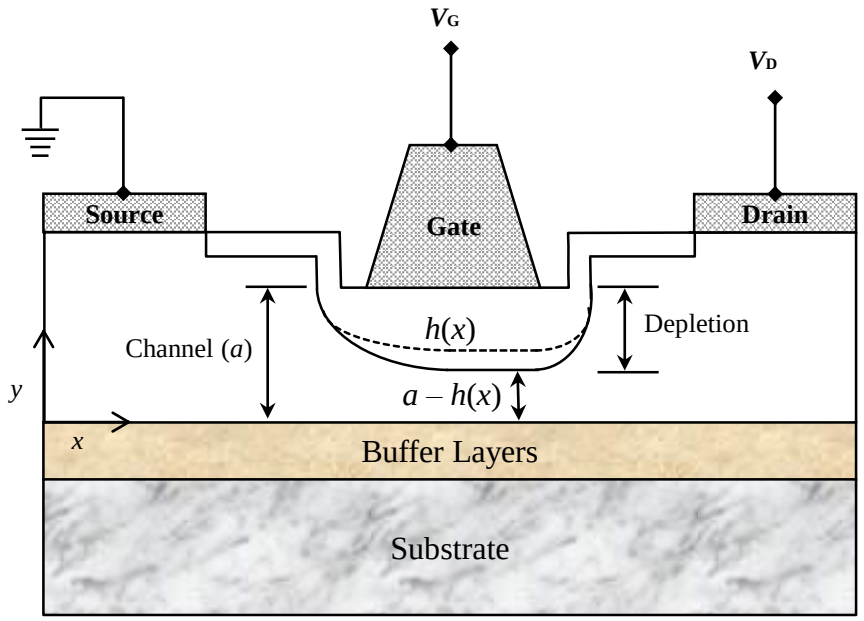

FIGURE 6.1: A crosssectional view of a SiC MESFET; the dotted line shows the modification of the Schottky barrier depletion under intense operating conditions.

quick handling of device parameters to obtain the required characteristics without considering much of the device physics. Therefore, using such techniques, the first-order response of the device is usually evaluated using a square-law expression [21], while second-order effects are incorporated using an appropriate nonlinear expression involving optimization variables [114, 129]. By using a single expression, such models can predict the output characteristics of microwave SiC MESFETs, including the shift in V_T, the compression in G_M, and the increase in G_D caused by device submicron geometry. However, to the best of the authors knowledge, none of these models incorporate self-heating effects to assess the reliability of the device characteristics under intense operating conditions.

A typical phenomenon that affects device characteristics when operating at high bias and under intense conditions is impact ionization. To initiate the impact ionization process, a critical field is required, and the bias at which this occurs for a given device depends on channel and buffer layer, the recess structure, etc. In Ref. [92, 186], it was demonstrated that, for a submicron SiC MESFET, impact ionization takes place for V_{DS} exceeding $>$ 100 V. Thus, a sharp change in I_{DS}, for a voltage prior to the onset of impact ionization in a SiC MESFET cannot be

associated with the impact ionization mechanism. Therefore, none of the models reported in literature can simulate the characteristics of SiC MESFETs for conditions in which the device exhibits a sharp increase in I_{DS} under intense operating conditions.

6.2 Model Development

In the saturation region of operation, the output characteristics of a FET device, under ideal conditions, can be approximated as follows [129]:

$$I_{DS} = I_{DSS}\left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right)^2, \tag{6.1}$$

where I_{DSS} represents drain-to-source current at $V_{GS} = 0$ V, δ simulates non-ideality in Schottky barrier of a FET, ΔV_T represents shifts in V_T because of the submicron geometry of the device, ξ takes into account the variation in V_T because of surface states, and γV_{DS} simulates dependence of V_T on V_{DS}. This is known as a square law, and it can generate the device characteristics after the onset of current saturation provided that $G_D = 0$ mS. To accommodate the finite G_D in the saturation region of operation, Riaz et al. [26] proposed that Eq. (6.1) can be redefined as

$$I_{DS} = I_{DSS}\left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right)^2 \times \left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right), \tag{6.2}$$

where λV_{DS} simulates finite G_D as a function of V_{DS} and $V_{ds(\text{sat})}$ is the value of V_{DS} at which the carriers attain the saturation velocity. To obtain a complete sweep of the output characteristics for $V_{DS} = 0$ to $V_{DS} < V_{Br}$, Eq. (6.2) can be rewritten as

$$I_{DS} = I_{DSS}\left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right)^2 \times \left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right) \tanh(\alpha V_{DS}). \tag{6.3}$$

Equation (6.3) is reported in Ref. [26] and represents a comprehensive expression to simulate the $I-V$ characteristics of SiC MESFETs including those with $L_g < 1$ μm. At high-bias, which is a requirement for high-power application or use of the device under high ambient temperature, the channel of the device exhibits unusual behavior; under such conditions, Eq. (6.3) fails to achieve the intended accuracy. To accommodate high-bias effects Eq. (6.3) can be modified as follows:

$$I_{DS} = I_{DSS}\left(1 - \frac{\delta V_{GS}}{V_T + \Delta V_T + \gamma V_{DS}}\right)^2 \times \left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right)\tanh(\alpha V_{DS}) + \left(1 + \exp\lambda_2(V_{DS} - V_{Br})\right), \tag{6.4}$$

where λ_2 is a fitting variable and the term appearing after the plus sign simulates the modification in channel crosssection for the flow of I_{DS}, in the form of either modification of the Schottky barrier depletion or expansion of the channel towards the buffer layers. Differentiating Eq. (6.4) with respect to V_{GS}, one obtains the following expression representing the device G_M

$$G_M = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V\,DS(\text{const})} = I_{DSS}\tanh(\alpha V_{DS}) \times \left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right) \times \left\{\frac{\delta}{V_{DS(\text{sat})}} - \frac{2\delta(1 + \lambda V_{DS})}{\xi V_T + \Delta V_T + \gamma V_{DS}} - \frac{3\delta^2 V_{GS}}{(\xi V_T + \Delta V_T + \gamma V_{DS})V_{DS(\text{sat})}}\right\}. \tag{6.5}$$

The values of $G_M(V_{GS})$ given by Eq. (6.5) and that reported in Ref. [26] are the same, because the term added in Eq. (6.4) is independent of V_{GS}. Differentiating Eq. (6.4) once again, but now with respect to V_{DS} while keeping V_{GS} constant, one obtains

$$G_D = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V\,GS(\text{const})} = I_{DSS}\left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right) \times \left\{\left(1 - \frac{\delta V_{GS}}{\xi V_T + \Delta V_T + \gamma V_{DS}}\right) \times \left[\lambda\tanh(\alpha V_{DS}) + \alpha\left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right)\right.\right.$$

$$\times \operatorname{sech}^2(\alpha V_{DS})\Bigg] + 2\left(1 + \lambda V_{DS} + \frac{\delta V_{GS}}{V_{DS(\text{sat})}}\right) \times \frac{\delta\gamma V_{GS}\tanh(\alpha V_{DS})}{(\xi V_T + \Delta V_T + \gamma V_{DS})^2}\Bigg\} + \left(\lambda_2 \exp\lambda_2(V_{DS} - V_{Br})\right). \tag{6.6}$$

6.3 Measured and Simulated DC Characteristics

To demonstrate the validity of Eq. (6.4), a submicron SiC MESFET was selected [175]; the physical parameters of the device are summarized in Table 6.1. A MATLAB code was developed based on Eq. (6.4) whose variables were optimized using the particle swarm optimization (PSO) technique [213, 219] with the help of an objective function given by Eq. (6.7)

$$\varepsilon = \sqrt{\sum_{j=S_1}^{N}\left\{\sum_{i=S_2}^{M}\left(I_{DS(exp)}^{i,j} - I_{DS(sim)}^{i,j}\right)^2 \Bigg/ \sum_{i=S_2}^{M} I_{DS(exp)}^{i,j}\right\}}. \tag{6.7}$$

Further, root-mean-square error (RMSE) between the optimized and the experimental characteristics was assessed using Eq. (6.8).

$$\text{RMSE} = \sqrt{\frac{1}{M}\sum_{i=S_2}^{M}\left(I_{DS(exp)}^{i} - I_{DS(sim)}^{i}\right)^2}. \tag{6.8}$$

In Eqs. (6.7) and (6.8), N and M represent the V_{DS} and V_{GS} bias values of the device having minimum values S_1 and S_2, respectively, whereas $I_{DS(exp)}$ and $I_{DS(sim)}$ represent experimental and simulated I_{DS}, respectively.

In Eq. (6.7), the variable ε represents an error value, which can be defined appropriately to ensure that the PSO terminates. Alternatively, optimization can also be achieved by allowing the algorithm to continue until the iteration count is reached. The strength of the objective function was assessed by evaluating the convergence rate of the PSO, which in this case was over 95%. The optimized values of the variables of Eq. (6.4) obtained in this way are listed in Table 6.2.

TABLE 6.1: Physical parameters of the submicron SiC MESFET [175]. L_g gate length, W gate width, a channel thickness, N doping density of the channel, b buffer layer thickness, N_b buffer layer doping density, x_p depletion layer thickness towards the buffer, and x_n depletion layer thickness towards the channel.

$\boldsymbol{L_g(\mu m)}$	$\boldsymbol{W(\mu m)}$	$\boldsymbol{a(\mu m)}$	$\boldsymbol{N(cm^{-3})}$	$\boldsymbol{b(\mu m)}$	$\boldsymbol{N_b(cm^{-3})}$	$\boldsymbol{x_P(\mu m)}$	$\boldsymbol{x_n(\mu m)}$
0.5	400	0.30	1.5×10^{17}	2.00	6×10^{15}	0.43	0.02

TABLE 6.2: Optimized parameters of Eq. (6.4) for a submicron SiC MESFET.

Variables	**Values**
$\lambda(1/V)$	0.0270
$V_T(V)$	12.00
Δ	-0.9534
ξ	-0.419
$\alpha(1/V)$	0.1698
$I_{DSS}(mA)$	70.81
γ	0.163
δ	-1.5898
$\lambda_2(1/V)$	0.4093

Figure 6.2 shows simulated and observed $I-V$ characteristics of a submicron SiC MESFET having $L_g = 0.5\mu$m. In Fig. 6.2(a), simulated characteristics are plotted using the model described in [26] whereas, in Fig. 6.2(b), simulated characteristics are attained using the proposed model defined by Eq. (6.4). Both plots show a smooth transition from the linear to the saturation region of operation, but after $V_{DS} \approx 40$ V, there is a sharp increase in the I_{DS} values. Since the observed sharp increase in I_{DS} retains its profile with further variation in V_{GS}, it cannot be associated with the impact ionization process. Were this increase caused by the impact ionization process, it would have shifted towards the lower V_{DS} values with increasing magnitude of V_{GS}, because increased V_{GS} magnitude would increase field inside the channel, which should result in earlier intimation of the impact ionization process [220]. Furthermore, it was demonstrated in [92, 221] that, in submicron SiC MESFETs, impact ionization takes place at $V_{DS} \sim 100$ V.

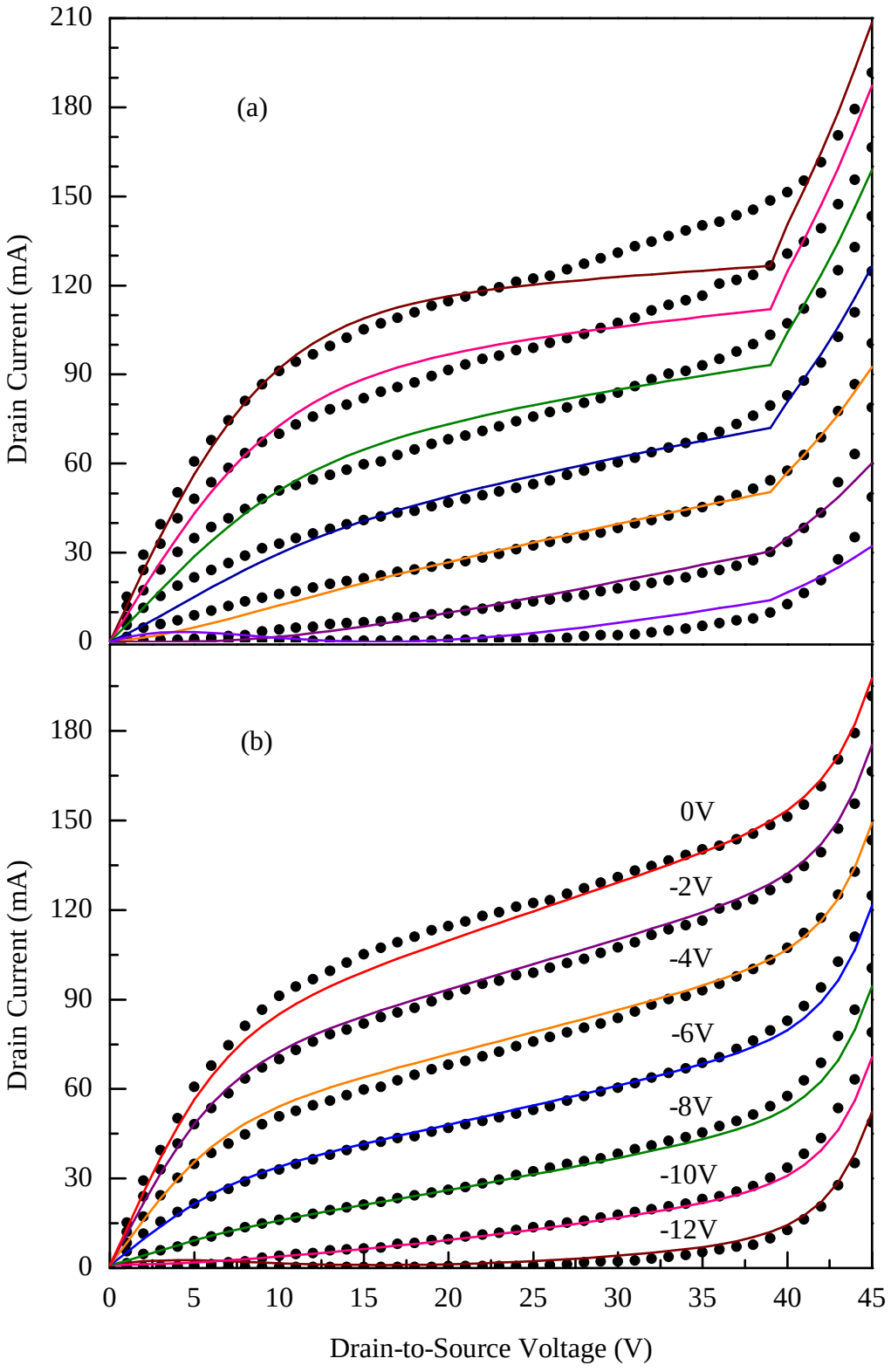

FIGURE 6.2: Simulated (solid line) and observed (filled circle) output characteristics of a 0.5 μm SiC MESFET obtained using **(a)** the Riaz model [26] and **(b)** by the proposed model for V_{GS} = 0 V to -12 V in steps of -2 V.

A plausible explanation for the observed $I-V$ characteristics could be that, at $V_{DS} \sim 40$ V, there is a strong $y-$directed field, which causes a modification in $h(x)$ resulting in an increased available crosssectional area, $a - h(x)$, for the current flow, as indicated by the dotted line in Fig. 6.1. This concept has been included in Eq. (6.4) using the term $[1 + \exp\lambda_2(V_{DS} - V_{Br})]$, and the result thus achieved exhibits good agreement with the experimental characteristics. According to this explanation, it is assumed that, since there is a wider barrier towards the buffer layer, i.e., $x_p = 0.43$ μm compared with $h(x)$, which can have a maximum value equal to a at $V_{GS} = V_T$,scattering of carriers towards the gate depletion will be relatively higher compared with their scattering towards the buffer layer. This causes a modification in $h(x)$ at $V_{DS} = 40$ V, and as a result I_{DS} increases, as shown by the experimental data in Fig. 6.2.

Table 6.3 presents a comparison of the performance of the proposed model relative to other models reported in literature [26, 115–117, 119]. The results in this table show that the second best model is that reported in Ref. [26] with average RMSE value of 4.89×10^{-3}, whereas the proposed model achieves an average RMSE of 2.52×10^{-3}, representing a $\sim 48\%$ improvement in the simulated output characteristics of the submicron SiCMESFET. Thus, one can say that the proposed model is capable of predicting the $I-V$ characteristics of SiC MESFETs, including in those regions which cause channel modification because of the intense operating conditions.

Figure 6.3 shows the simulated and observed G_M of the device under discussion. Simulation shown in Fig. 6.3 was carried out using Eq. (6.5) at $V_{DS} = 25$ V and $V_{DS} = 45$ V. One can see from the results in this figure that the device retained its functionality at both bias levels, revealing that the fundamental operation of the device remained intact; it therefore cannot be claimed that the device has entered the breakdown region. Rather, there is an improvement in the G_M value at $V_{DS} = 45$ V relative to $V_{DS} = 25$ V, once again supporting the argument that there is a reduction in $h(x)$ of the device after $V_{DS} = 40$ V, and as a result $a-h(x)$ value is increased. Thus, the conducting channel is relatively closer to the gate.

TABLE 6.3: Comparison of RMS error values of various models in simulating the $I-V$ characteristics shown in Fig. 6.2.

Model	**RMSE$\times 10^{-3}$ at V_{GS}**							**Average**
	-12V	**-10V**	**-8V**	**-6V**	**-4V**	**-2V**	**0V**	**RMSE$\times 10^{-3}$**
McCamant [117]	12.39	5.21	6.48	8.62	7.65	7.43	6.72	7.79
Curtice [119]	13.05	11.60	9.90	8.89	7.28	6.28	4.25	8.75
TOM3 [116]	12.30	6.74	5.59	7.11	7.10	7.74	6.52	7.59
Angelov [115]	12.36	6.45	5.20	7.90	9.28	10.33	10.22	8.82
Riaz [26]	8.42	7.05	5.49	3.37	2.48	3.56	3.87	4.89
Proposed	3.66	2.63	2.91	1.90	2.53	2.24	1.74	2.52

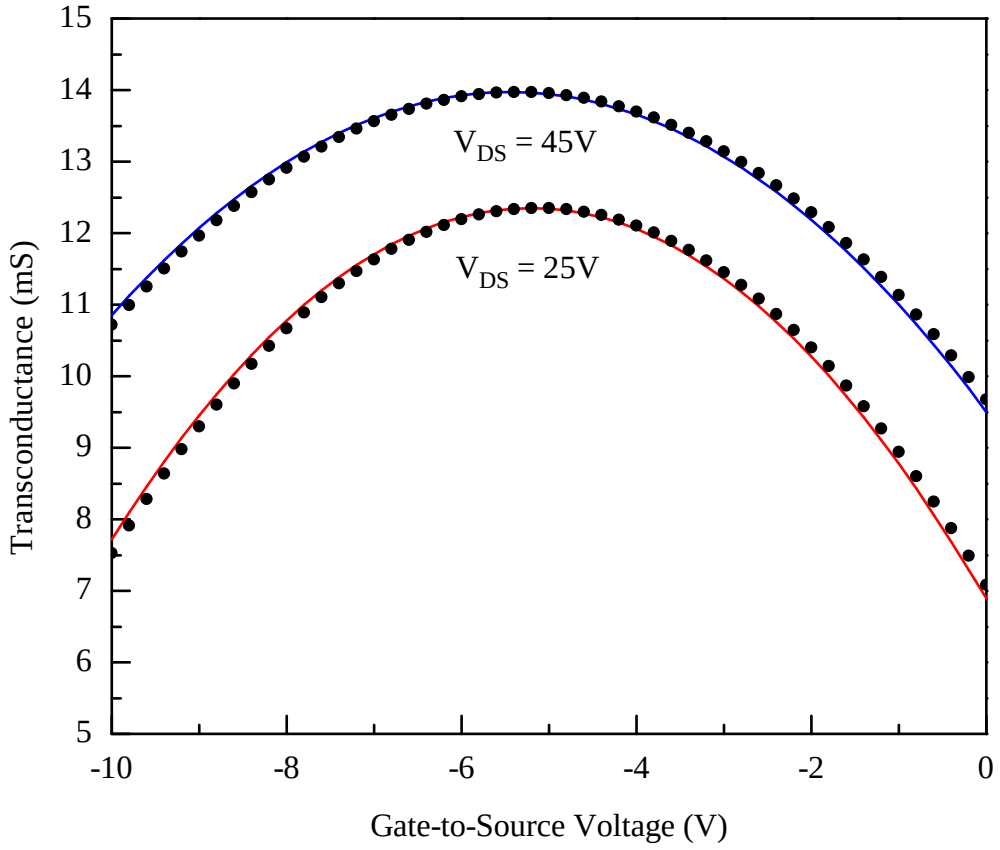

FIGURE 6.3: Simulated (solid line) and observed (filled circle) transconductance of a submicron SiC MESFET.

Also, in compliance with the nonlinearity principle defined in $V_T = (QSNa^2)/2\varepsilon_s$ where ε_s is the permittivity of SiC, the gate, under such circumstances, will have better control over the conducting channel. This could cause the increase in G_M

at $V_{DS} = 45$ V relative to $V_{DS} = 25$ V as observed in Fig. 6.3.

Figure 6.4 represents G_D versus V_{DS} response of the device under discussion at various V_{GS} values. Dots in this figure correspond to experimental data, whereas solid and broken lines indicate results obtained using the proposed model and that in [26], respectively. By examining the plots in this figure, one clearly sees that the Riaz model does not agree with the experimental data after $V_{DS} \approx 40$ V. This is the point where I_{DS} shows a sharp increase. Since above $V_{DS} \approx 40$ V, the Riaz model exhibits lines of constant slope in the $I_{DS}(V_{DS}, V_{GS})$ characteristics, their differentiation to obtain G_D results in constant values, hence a step response in G_D at $V_{DS} \geq 40$ V is witnessed in each part of Fig. 6.4.

Table 6.4 summarizes the RMS error values of the observed and simulated G_D of a submicron SiC MESFET at various V_{GS} bias levels. One can see from the data in this table that the proposed model achieves significantly lower RMS error values for the bias levels considered. Comparing the average RMS error, it can be calculated that the proposed model is $\sim 63.5\%$ better than the model reported in Ref. [26]. Thus, the proposed model is versatile enough to predict the device characteristics with improved accuracy by accommodating all possible variables, including those caused by intense operating conditions.

TABLE 6.4: RMS error values of output conductance (G_D) evaluated using the proposed model in comparison with that in Ref. [26], for a submicron SiC MESFET characteristics shown in Fig. 6.4.

Model	**RMSE$\times 10^{-3}$**				**Average**
	$V_{GS} = 0$**V**	$V_{GS} = -4$**V**	$V_{GS} = -6$**V**	$V_{GS} = -10$**V**	**RMSE$\times 10^{-3}$**
Ref. [26]	1.40	1.49	1.18	1.83	1.47
Proposed	0.52	0.67	0.48	0.52	0.54

To assess device reliability, the G_M/G_D ratio was evaluated and is shown in Fig. 6.5(a) at $V_{DS} = 25$ V,where the device functions normally, and in Fig. 6.5(b) at $V_{DS} = 45$ V, where the device has shown a sharp increase in I_{DS}. A value of $G_M/G_D > 1$ means that the variation in drain current (ΔI_{DS}) caused by variation at the gate electrode (ΔV_{GS}) will be more pronounced compared with the ΔI_{DS}

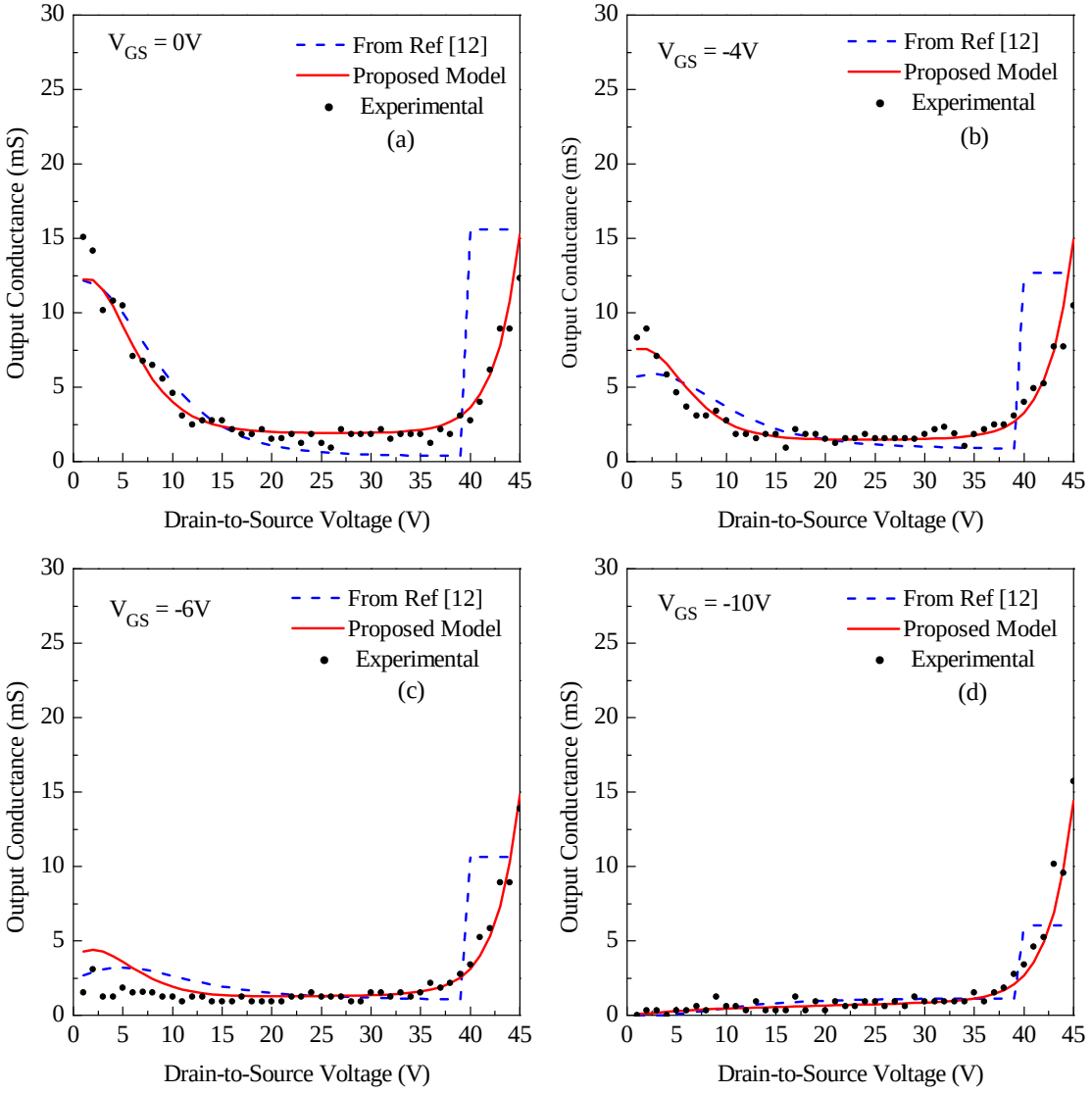

FIGURE 6.4: Comparison of output conductance (G_D) evaluated using the proposed model versus the best reported model [26] for a submicron SiC MESFET.

variation caused by ΔV_{DS} around the same Q-point. In other words, a relatively high value of G_D at any given bias level indicates poor control of the Schottky barrier on I_{DS}. Owing to this fact, the ideal value of G_D, after the onset of current saturation, is zero. Thus, to assess device reliability, it is obvious from Fig. 6.5(a) that $G_M/G_D > 1$ is observed for the entire region of operation considered. In contrast, it can be seen from Fig. 6.5(b) that $G_M/G_D < 1$ when measured at $V_{DS} = 45$ V. This shows that, although the device retains its functionality at $V_{DS} = 45$ V, because this potential is far below the potential required to start impact ionization process [92], its performance is still significantly deteriorated.

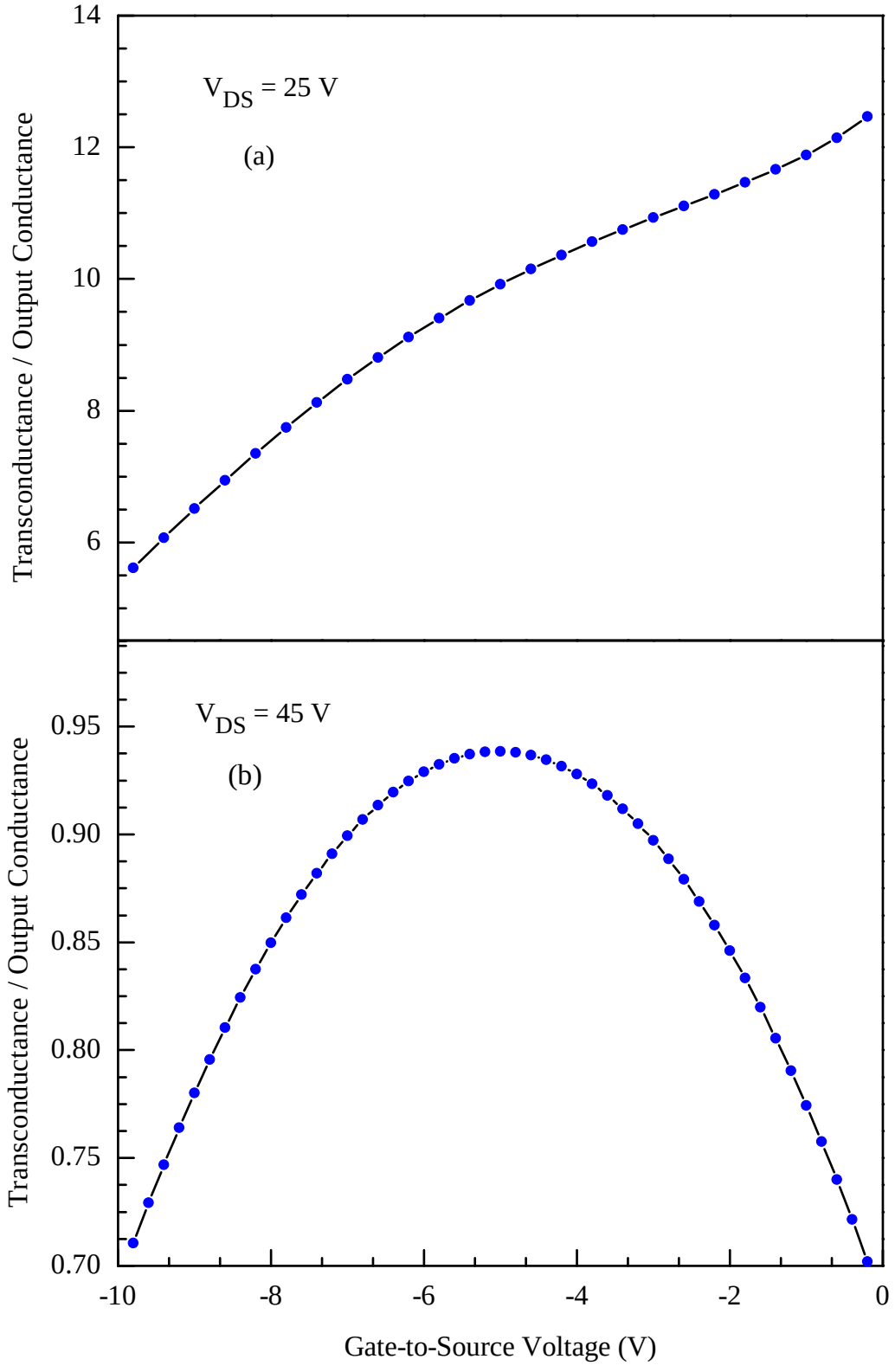

FIGURE 6.5: Ratio of transconductance to output conductance (G_M/G_D) at **(a)** $V_{DS} = 25$ V, where the device is operating normally, and at **(b)** $V_{DS} = 45$ V, where the device exhibits a sharp increase in drain current.

6.4 Assessment of Intrinsic AC Parameters

SiC MESFETs are used as active devices in microwave power amplifiers, showing the ability to handle power levels as high > 1 W/mm with power-added efficiency above 60% at frequencies greater than 2 GHz [19, 222]. It is therefore pertinent to assess the reliability of the device AC parameters at relatively high bias, i.e., $V_{DS} > 40$ V. Ahmed proposed a technique to assess the small-signal parameters of a FET device using its DC characteristics [138]. The same concept was extended to SiC MESFETs by Riaz et al. [172], who also proposed the following expressions for evaluation of the device Miller capacitances, namely the drain-to-source capacitance (C_{DS}), gate-to-drain capacitance (C_{GD}), and gate-to-source capacitance (C_{GS}):

$$C_{DS} \approx \left[\frac{2W\varepsilon_s \left\{ a - \left(I_{DS}/qN\upsilon_s W \right) \right\}}{L_g/4} \right] \tag{6.9}$$

$$C_{GD} \approx \left[\frac{\varepsilon_s W}{1 + (2/L_g)\left[a - \left(I_{DS}/qN\upsilon_s W \right) \right]} \right] \tag{6.10}$$

$$C_{GS} \approx (\varepsilon_s W L_g) \left[a - \frac{I_{DS}}{qN\upsilon_s W} \right]^{-1} \tag{6.11}$$

where υ_s is the electron saturation velocity. In Eqs. (6.9)-(6.11), the Miller capacitances have been defined using the channel current I_{DS} rather than $h(x)$, which is usually employed to define them. It is pertinent to mention here that, in the definition of aforementioned capacitors according to Ref. [26], I_{DS} is given by Eq. (6.3);whereas according to our modified definition, it is represented by Eq. (6.4). Therefore, the values of these capacitances will vary at $V_{DS} \approx 40$ V, the point where I_{DS} exhibits a sharp increase in its value and Eq. (6.3) fails to agree with the experimental data.

The variation of the device Miller capacitances as functions of the applied bias is shown in Fig. 6.6. In Fig. 6.6(a), C_{DS} is plotted as a function of V_{DS} for two

distinct V_{GS} bias levels. It is obvious from this figure that both plots, i.e., the one which represents the model reported in Ref. [172] and the proposed model, coincide for $V_{DS} \leq 35$ V. This is the point at which, according to the proposed explanation, the value of $h(x)$ starts changing, while this change becomes very prominent at $V_{DS} = 40$ V. For $V_{DS} > 40$ V, there is clear deviation between the profiles obtained using the two models. This deviation is primarily associated with the reduction in the value of $h(x)$, because at $V_{DS} \geq 40$ V, the channel carriers become hot and the y-directed field attracts these carriers towards the gate depletion, allowing the depletion to shrink mainly at the drain side of the channel. This will make the depletion less tapered towards the drain side of the gate electrode, thus making it more aligned with the gate metal. This will cause the drainsource charges to be further off from one another, resulting in a reduction in C_{DS}, as is evident from Fig. 6.6(a).

Figure 6.6(b) shows the variation in C_{GD} as a function of applied bias. The data of Fig. 6.6(b) were plotted using Eq. (6.10), with filled symbols representing C_{GD}, assessed using the proposed I_{DS} expression defined by Eq. (6.4), while the open symbols in Fig. 6.6(b) represent C_{GD} simulated using I_{DS} expression given by Eq. (6.3). Once again, there is a clear deviation in C_{GD} magnitude at $V_{DS} \geq 40$ V between the two models under discussion. Although the device is apparently functioning at $V_{DS} \geq 40$ V, the plot in Fig. 6.6(b) indicates that the device will not show reliable performance under this bias condition.

Finally, Miller capacitance C_{GS}, which is the most crucial capacitor involved in determining the high-frequency performance of a device, was evaluated and is shown in Fig. 6.6(c). These plots were obtained using Eq. (6.11), where the dependence of C_{GS} on I_{DS} is evident. Since there are two different definitions for $I_{DS}(V_{DS}, V_{GS})$, viz. Equations (6.3) and (6.4), their use in defining C_{GS} will result in two different profiles, as seen in Fig. 6.6(c). This figure clearly shows that, when using the proposed definition of I_{DS}, there is a significant increase in the magnitude of the C_{GS} capacitance. This increase could be associated with the reduction in $h(x)$, which eventually brings the two plates of the capacitor closer to one another, hence increasing the value of C_{GS}, as evident from Fig. 6.6(c).

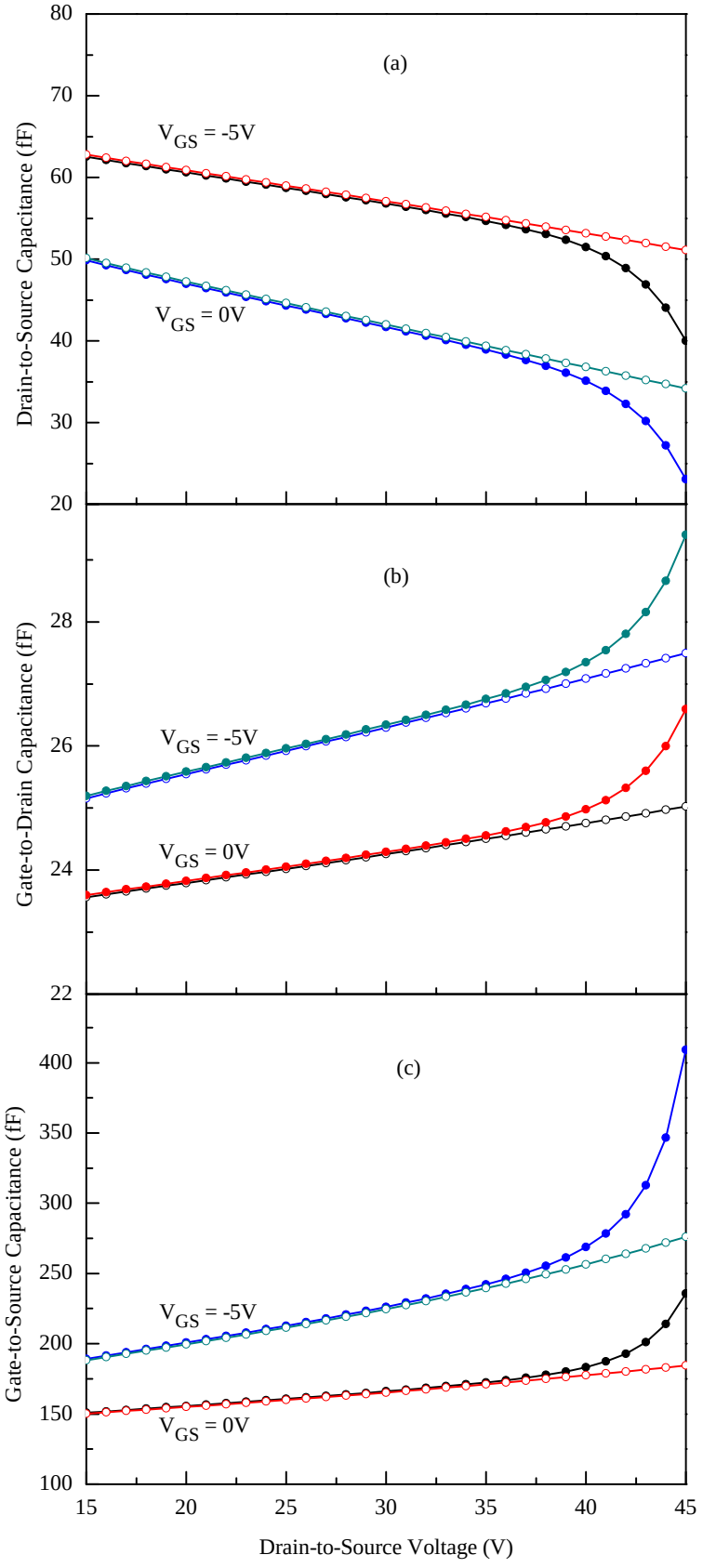

FIGURE 6.6: **(a)** Drain-to-source capacitance, C_{DS}, **(b)** gate-to-drain capacitance, C_{GD}, and **(c)** gate-to-source capacitance, C_{GS}, of a 0.5 μm SiC MESFET. Open circles (○), represent values obtained from [26]; whereas filled circles (●) show capacitances calculated using the model proposed herein.

TABLE 6.5: Variation in Miller capacitance values on changing the V_{DS} of a submicron SiC MESFET from 35 to 45 V, obtained using the conventional [172] and the proposed techniques.

Model	$\boldsymbol{C_{DS}}$		$\boldsymbol{C_{GD}}$		$\boldsymbol{C_{GS}}$	
	$V_{GS} = 0$V	$V_{GS} = -5$V	$V_{GS} = 0$V	$V_{GS} = -5$V	$V_{GS} = 0$V	$V_{GS} = -5$V
Ref. [172]	13.23%	7.27%	2.07%	2.94%	7.27%	13.23%
Proposed	40.79%	26.84%	7.63%	9.01%	26.83%	40.77%

Since the high-frequency performance of a SiC MESFET is defined by the expression

$$f_T \approx \frac{G_M}{2\pi(C_{GS} + C_{GD})}, \tag{6.12}$$

an appropriate assessment of the capacitances involved in Eq. (6.12) is crucial to obtain reliable knowledge about the AC performance of the device. The variation in the capacitance values for $V_{DS} = 35-45$ V of a submicron SiC MESFET is summarized in Table 6.5. Considering the performance of the proposed model, which demonstrated an improvement of $\sim 48\%$ in predicting the characteristics of a SiC MESFET as shown in Fig. 6.2, it can be claimed that the changes in the capacitance values are much greater than those predicted by the model in Ref. [172]. Thus, by using the proposed model in the assessment of the Miller capacitances, one can better predict the AC performance of a device for higher bias levels, at which $h(x)$ is modified because of intense channel conditions.

Figure 6.7 shows the variation in f_T as a function of the applied bias. The data shown in this figure were obtained using Eq. (6.12), wherein the Miller capacitances were evaluated using the modified definition involving I_{DS} as given by Eq. (6.4). The plot in Fig. 6.7, in compliance with the results for the Miller capacitances, again shows deviation between the two models under discussion, for $V_{DS} \geq 35$ V. This implies that, at relatively higher bias levels, though the device will function, its AC performance will deteriorate because of the changes occurring in the device channel. Furthermore, examining Figs. 6.3 and 6.6 together reveals a contradictory observation: in Fig. 6.3, the magnitude of G_M increases

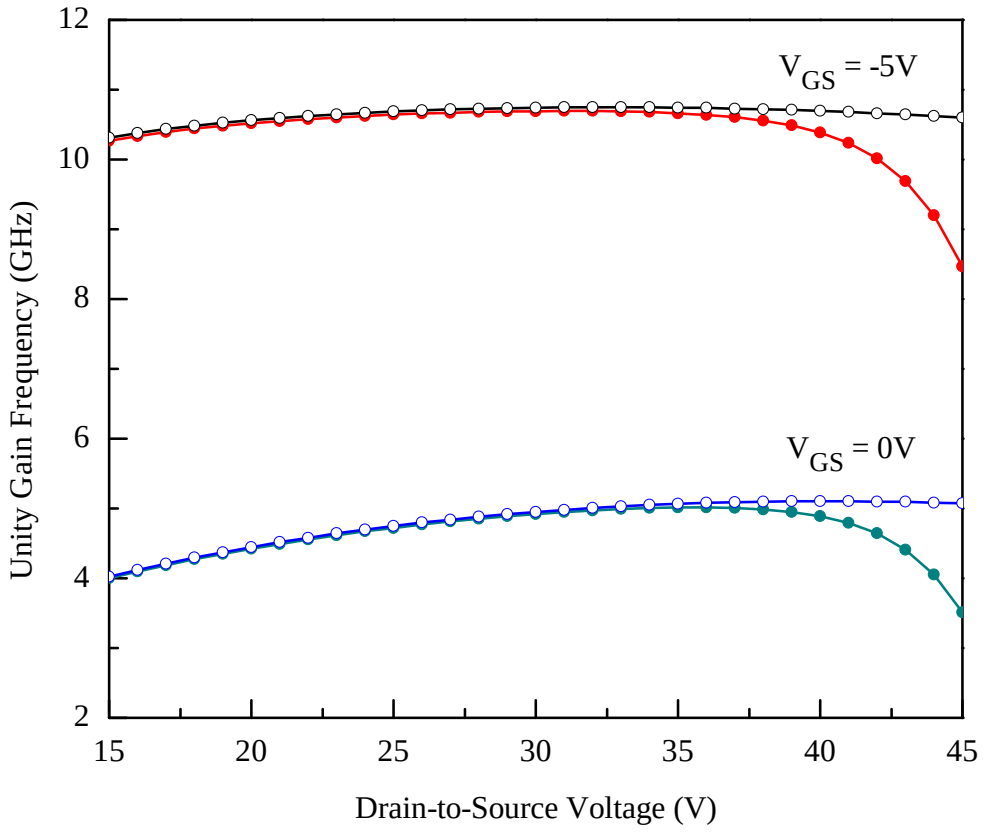

FIGURE 6.7: Unity gain frequency (f_T) of a 0.5 μm SiC MESFET. Open circles represent values of f_T obtained from Ref. [172], whereas filled circles represent simulated values of f_T obtained using the proposed model.

at $V_{DS} = 45$ V, which will contribute positively to determining f_T of the device as per Eq. (6.12); meanwhile, the values of the C_{GS} and C_{GD} capacitances exhibit an increase at $V_{DS} = 45$ V. Since the increase in magnitude of C_{GS} and C_{GD} is much greater than the positive contribution made by G_M in Eq. (6.12), they dominate in defining f_T response of the device, resulting in the declining profile for $V_{DS} = 35{-}45$ V.

The time taken by the channel to respond to the changing voltage of the Schottky barrier gate in the form of an input signal is referred to as the transit time (τ) of the device. Basically, this is the time consumed by the Miller capacitances (C_{GS} and C_{GD}) to adjust to the new values whenever there is a change in the signal at the gate electrode of the device. Carriers passing the region defining C_{GS} and C_{GD} will have knowledge of the gate signal, thus the time consumed by C_{GS} and C_{GD} during their charging and discharging process will be the factor determining

τ, which can be expressed as

$$\tau \approx \left[\frac{C_{GS} + C_{GD}}{2G_M}\right]. \tag{6.13}$$

Equation (6.13) captures the dependence of τ on C_{GS} and C_{GD}, as plotted in Fig. 6.8. This figure also shows that the value of τ starts to deviate from its conventional profile for $V_{DS} = 35{-}45$ V.

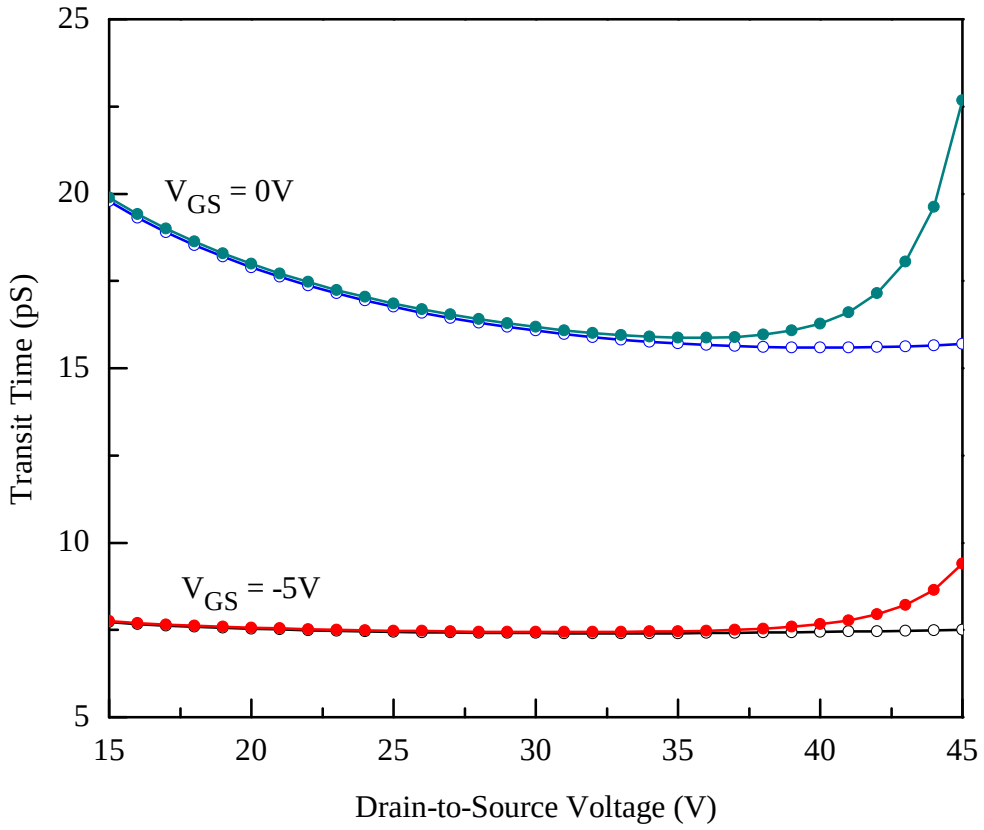

FIGURE 6.8: Transit time delay (τ) of a 0.5 μm SiC MESFET. Open circles represent values of τ obtained from Ref. [172], whereas filled circles represent simulated values of τ obtained using the proposed model.

The channel resistance (R_I) of the device is evaluated using Eq. (6.14), as plotted in Fig. 6.9.

$$R_I = \left[\frac{\upsilon_s L_g}{\mu I_{DS}}\right]. \tag{6.14}$$

At relatively higher bias, i.e. $V_{DS} \geq 35$ V, the value of R_I starts to reduce, which is in line with the explanation presented hitherto; namely, in Eq. (6.14), the current I_{DS}, which appears in the denominator of the expression, increases

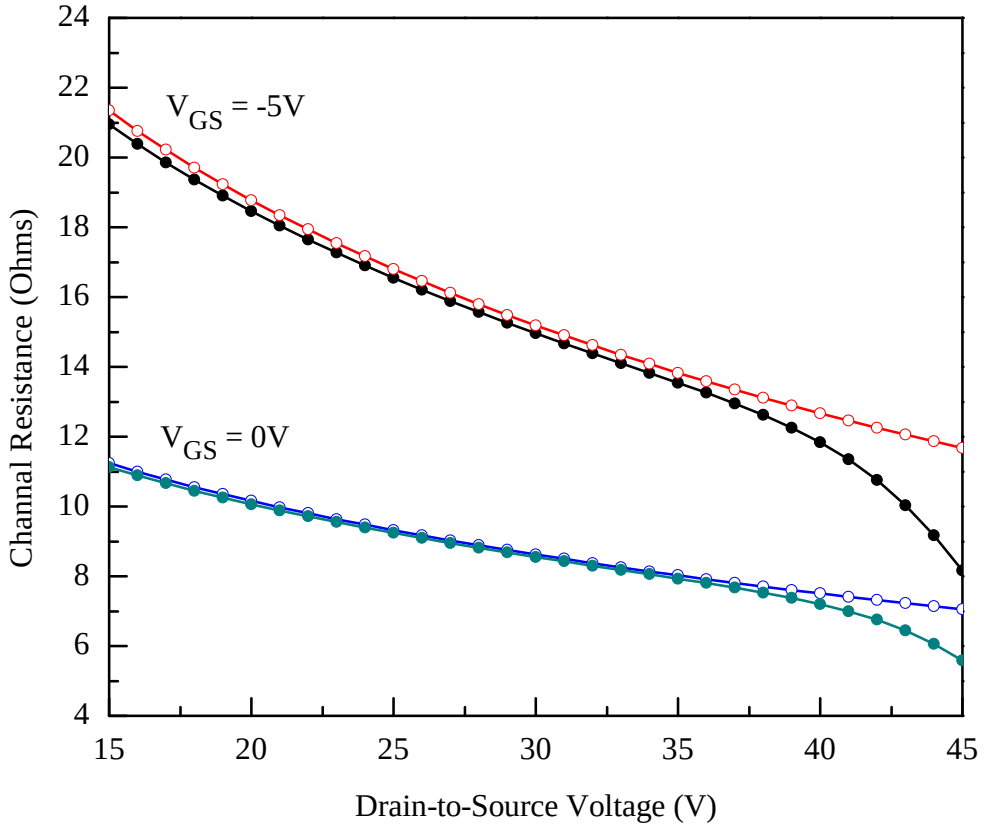

FIGURE 6.9: Channel resistance (R_I) of a 0.5 μm SiC MESFET. Open circles represent values of R_I obtained from [172], whereas filled circles represent simulated values of R_I obtained using the proposed model.

at $V_{DS} = 35{-}45$ V, as shown in Fig. 6.2, thus there is a decline in R_I after $V_{DS} = 35$ V. This reduction in R_I indicates that carrier flow becomes easier under the applied bias. Since all other variables involved in the definition of R_I are constant, apart from the crosssectional area of the channel, which increases with the decrease of $h(x)$ as established above, a reduction in R_I after $V_{DS} = 35$ V is also observed. This explanation is consistent and supports the arguments given above to explain the other DC and AC characteristics of the device.

Table 6.6 summarizes the AC parameters of the device under discussion. One can see from the data in this table that, at $V_{DS} = 25$ V, the values evaluated from Ref. [172] closely match those obtained using the proposed technique. However, at $V_{DS} = 45$ V, the evaluated AC parameters deviate significantly from those in Ref. [172], as the latter does not take into account the variations that take place in the device under intense operating conditions. Therefore, the proposed model

TABLE 6.6: Intrinsic small-signal parameters of 0.5 μm SiC MESFET at V_{GS} = 0 V evaluated using the model of Riaz [172] in comparison with that proposed herein.

Bais	V_{DS} **= 25 V**	V_{DS}**= 45 V**	V_{DS} **= 25 V**	V_{DS}**= 45 V**
Parameter	**Ref. [172]**		**Proposed**	
C_{GS}(fF)	211.46	276.02	212.77	409.12
C_{GD}(fF)	25.92	27.49	25.95	29.40
C_{DS}(fF)	44.60	34.17	44.33	23.05
G_M(mS)	7.28	10.52	7.28	9.83
G_D(mS)	1.93	1.93	1.93	15.27
τ(ps)	16.75	15.69	16.85	22.66
$R_I(\Omega)$	9.32	7.04	9.24	5.59
f_T(GHz)	4.74	5.07	4.72	3.51

provides an improved assessment of the operational reliability of the device under high-bias conditions.

6.5 Summary

The operational reliability of submicron SiC MESFETs was investigated. A non-linear model was developed to simulate the $I-V$ characteristics of the device. It was demonstrated that the proposed model can predict the output characteristics of the device both under normal conditions as well as at relatively high drain bias. It was demonstrated that, for a submicron SiC MESFET, at V_{DS} = 35 V, the gate of the device starts to lose control over the channel and the drain current shows a sharp rise in magnitude. It was also shown that, at such drain bias levels, the device performance remains intact, provided that the transconductance to output conductance ratio (G_M/G_D) is greater than unity. The developed model demonstrates a 48% improvement in simulating the output characteristics

of a submicron SiC MESFET, and 63.5% improvement in predicting the output conductance of the device. The small-signal parameters of SiC MESFETs were evaluated using the proposed technique and compared with the Riaz model. It was established that, at relatively high bias levels, the AC response of the device will deteriorate because of the intense channel conditions, which change the device Miller capacitances and other parameters associated with them. The developed technique could represent a useful tool to assess the performance of high-power microwave SiC MESFETs over a wider bias range.

Chapter 7

Conclusion and Future Work

This chapter presents concluding remarks pertaining to DC and AC characteristics reliability of wide bandgap MESFETs and HEMTs. The performance of FETs depend upon the material used for their fabrication. Devices fabricated using SiC and GaN have superior performance, both in DC and AC domain compared to GaAs based devices. SiC based devices have excellent heat conduction in high power applications and shows maximum stability in performance.

It is established that the device characteristics can be predicted by using analytical or numerical models. Numerical models are easy to conceive, as they deal with the device parameters, which can be manipulated effectively and efficiently through a nonlinear expression. On the other hand, analytical models require a comprehensive knowledge of the electric field distribution inside the channel and can be quite complex, as the field distribution inside the channel is non-uniform, and depends both on the device geometry, as well as, on applied bias.

It is discussed that RF performance of FETs rely mainly upon the device intrinsic parameters. Parameter extraction techniques play a crucial role in determining the accuracy of the predicted intrinsic parameters. For accurate small signal modeling, a suitable capacitor model is needed. Such a model could help the design engineer to assess the reliability of the device under changing conditions.

It is shown by making an exhaustive review of relevant literature that SiC and GaN based devices can be operated at higher drain-to-source voltages, and have the ability to mitigate reasonably well, self-heating effects compared to 2^{nd} generation devices such as GaAs. Self-heating effects are directly proportional to the power handled by the device. Under high bias, characteristics of the device could degrade and a simple model, either analytical or numerical, may not be accurate enough to predict the device performance. So, to get better understanding and wide applicability, there is a need to develop a model for SiC and GaN MESFETs that incorporates self-heating effects.

As a 1^{st} part of this research, an improved analytical model for wide bandgap power MESFETs is developed to predict output and transfer characteristics. The proposed model incorporates negative conductance in the saturation region of operation caused by the device self-heating and harsh ambient environment where such devices are usually subjected to. It has been established that the developed model can predict output characteristics even for submicron MESFETs with a good degree of accuracy. A comparative analysis showed that the developed technique offers $\sim 50\%$ and $\sim 37\%$ improvement in predicting the output characteristics of wide bandgap MESFETs at $T = 300$ K and $T = 500$ K, respectively; relative to the best reported model in the literature. Based on the developed $I-V$ expression, device output conductance and transconductance are also modeled. It has been shown that the developed technique can model the device output conductance for the entire range of its operation, both at room, as well as, at elevated temperature with an improved accuracy. The validity of the model is checked for a wide range of data set and also for devices of varying dimensions. It is observed that the proposed technique could be useful in assessing the temperature dependent characteristics of wide bandgap MESFETs, meant for high temperature operation.

As a 2^{nd} part of this research, an analytical model has been developed to assess intrinsic capacitors of microwave power FETs by distributing the depletion layer underneath the Schottky barrier gate of the device into four distinct regions. Region-I of the depletion is its extension towards the source side of the gate than

the Schottky barrier metal; whereas, Region-II starts from the Schottky metal to the point where the carriers' velocity gets saturated, and from this point to the end of the Schottky metal gate, the depletion layer is represented by Region-III. Finally, Region-IV is defined by the extension of the depletion towards the drain side of the device. Analytical expressions have been developed to assess the linear, as well as, the saturation region gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitors. It has been shown that three region analytical model to assess intrinsic capacitors, especially C_{GD} of the device reduces its accuracy because, it does not take into account accurately Region-IV of the device, which plays a crucial role in defining the intrinsic capacitors. The proposed technique exhibited 69% and 93% improvement in RMSE while assessing C_{GD} as a function of V_{DS} and V_{GS}, respectively; relative to III Region model when compared with the experimental data.

In heterostructure devices, properties of the chosen substrate play an important role in determining the characteristics of an HEMT. As a 3$^{\text{rd}}$ part of this study, effects of Si and SiC substrates on the AC performance of submicron GaN HEMTs are presented. Particle swarm optimization (PSO) is used to extract intrinsic component values of the device. Optimized values are achieved through an objective function, which involves measured S-parameters. Sahoo et al's. modified circuit model with substrate losses is compared with the conventional model and it is observed that the extra substrate components have marginal or no impact on the device S-parameters. It is further established that use of SiC substrate relative to Si offers little advantages as far as high frequency applications are concerned. Therefore, Si substrate could be employed for those applications where economical fabrication is a key consideration.

As a 4$^{\text{th}}$ of this research, operational reliability of submicron SiC MESFETs is investigated. A nonlinear model is developed to simulate the $I-V$ characteristics of the device. It is demonstrated that the proposed nonlinear model can predict the output characteristics of the device, both under normal conditions, as well as, at relatively high drain bias. It is established that, for submicron SiC MESFETs, the gate electrode of the device starts losing its control over the channel at relatively

high bias, and the drain current shows a sharp rise in magnitude. At such drain bias levels, the device performance remains intact, provided that the transconductance to output conductance ratio (G_M/G_D) is greater than unity. The developed technique demonstrated a 48% improvement in simulating the output characteristics of submicron SiC MESFETs, and 63.5% improvement in predicting the output conductance of the devices. Small signal parameters of SiC MESFETs are also evaluated using the developed technique and compared with earlier reported data. It is established that, at relatively high bias levels, the AC response of the device deteriorates because of the intense channel conditions, which change the device intrinsic capacitances and other parameters associated with them. The developed technique could represent a useful tool to assess the performance of high-power microwave SiC MESFETs over a wider bias range.

7.1 Future Extension

Wide bandgap semiconductors, especially GaN, are known as future Si of microelectronic industry. FETs made from wide bandgap semiconductors are attaining greater popularity in microwave power industry and for their efficient utilization, an effort has been made in this thesis to give a better operational understanding of such devices. The current research can be extended further into following possible areas:

1. Reliability of GaN devices is in embryonic stage in power applications. In order to get competitive FETs, SiC should be a preferred substrate for GaN devices. Although, Si is a dominant material but SiC bulk material has changed the trend of the technology. The quality of SiC wafer is improved with low micropipe density and provides good results for large scale fabrication process. So, from research point of view it would be interesting to investigate electrical properties of SiC substrates based GaN MESFETs/HMETs for microwave power applications.

2. In our nonlinear model, we have predicted the output characteristics of the device at relatively high drain bias without considering the temperature effects. This work can further be extended to develop a model to evaluate the performance of the device at elevated temperatures for its various regions of operation. The model should be capable of predicting temperature dependent DC and AC parameters of the device and could directly be coupled in CAD involving power FETs.

3. Schottky barrier height plays an important role in the device performance. We have presented an analytical model for wide bandgap power MESFETs to predict transfer and output characteristics by dividing the Schottky barrier layer into four distinct regions. The developed technique can further be extended by taking into account the Schottky barrier hight as a temperature dependent variable, which can also lead to a temperature dependent capacitor model for wide bandgap MEFETs.

4. To cater the increasing needs of communication, there is a pressing demand for high power and frequency devices. To accommodate high frequency, the gate length of a FET should be as small as possible and on the other hand, to address high power requirements, the gate width should be large enough to generate sufficient current; resulting into interdigitated FETs. A study of gate length dependent interdigitated FETs involving self and ambient heating to assess their DC and AC potential, under harsh conditions, would be a useful study for microwave power applications.

5. Impact ionization is a limiting factor in defining the response of high power FETs. Once the impact ionization started, the current would be no longer under the control of the gate, and the device is bound to lose its normal behavior. The initiation of impact ionization depends upon the channel conditions, which are driven by the channel field, mainly defined by the Schottky barrier gate and the buffer layers. A study to assess impact ionization in wide bandgap FETs as a function of channel field would be beneficial for power related applications involving FETs.

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