CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD

Design of High Frequency PWM Inverter as a Part of 100kVA Solid State Transformer

by

Abdur Rehman

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By

Abdur Rehman

(DEE143001)

Dr. Keliang Zhou, Associate Professor

University of Glasgow, Glasgow, UK

(Foreign Evaluator 1)

Dr. Mihai Rata, Associate Professor

Stifen cel Mare University of Suceava, Romania

(Foreign Evaluator 2)

Dr. Muhammad Ashraf

(Thesis Supervisor)

Dr. Noor Muhammad Khan

(Head, Department of Electrical Engineering)

Dr. Imtiaz Ahmad Taj

(Dean, Faculty of Engineering)

DEPARTMENT OF ELECTRICAL ENGINEERING

CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

ISLAMABAD

2022

I dedicate this thesis to my wife, daughter Anosha and son Muhammad Talha for their love, endless support & encouragement.

CAPITAL UNIVERSITY OF SCIENCE & TECHNOLOGY ISLAMABAD

Expressway, Kahuta Road, Zone-V, Islamabad
Phone:+92-51-111-555-666 Fax: +92-51-4486705
Email: info@cust.edu.pk Website: https://www.cust.edu.pk

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This is to certify that the research work presented in the thesis, entitled "**Design of High Frequency PWM Inverter as a Part of 100kVA Solid State Transformer**" was conducted under the supervision of **Dr. Muhammad Ashraf**. No part of this thesis has been submitted anywhere else for any other degree. This thesis is submitted to the **Department of Electrical Engineering, Capital University of Science and Technology** in partial fulfillment of the requirements for the degree of Doctor in Philosophy in the field of **Electrical Engineering.** The open defence of the thesis was conducted on **December 24, 2021.**

Student Name : Abdur Rehman (DEE-143001)

The Examination Committee unanimously agrees to award PhD degree in the mentioned field.

Examination Committee :

(a) External Examiner 1: Dr. Haroon-ur-Rashid
Professor
PIEAS, Islamabad

(b) External Examiner 2: Dr. Fida Muhammad Khan
Professor
Air University, Islamabad

(c) Internal Examiner : Dr. Umer Amir Khan
Assistant Professor
CUST, Islamabad

Supervisor Name : Dr. Muhammad Ashraf
Professor
CUST, Islamabad

Name of HoD : Dr. Noor Muhammad Khan
Professor
CUST, Islamabad

Name of Dean : Dr. Imtiaz Ahmad Taj
Professor
CUST, Islamabad

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List of Publications

It is certified that following publication(s) has been made out of the research work that has been carried out for this thesis:-

1. **A. Rehman** and M. Ashraf, "Design and analysis of PWM inverter for 100KVA solid state transformer in a distribution system", *IEEE Access*, vol. 7, pp. 140152-140168, 2019.

(Mr. Abdur Rehman)
Registration No: DEE143001

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(Mr. Abdur Rehman)

Registration No: DEE143001

Abstract

The emergence of high power converters establishes the existed power grid much more dynamic, vibrant than it was ever before. One of the scorching research directions in power electronics field is a Solid State Transformer (SST) which aims at replacing the existing broadly used conventional Line Frequency (50/60Hz) Transformers (LFT).

This research dissertation deliberates a high frequency PWM inverter design for 11kV/ 381V, 100kVA solid-state transformer for a power distribution system application. Half Bridge topology strategy, incorporating less number of switches with reduced losses as compared to full bridge configuration is implemented. This design outpaces and alleviates the predecessors in terms of efficiency and THD measurements. The mathematical analysis and computer simulations are carried out to design the proposed converter. This anticipated design has been premeditated in MATLAB/SIMULINK environment for effectiveness of study and performance measures. The use of medium frequency transformer has contributed in efficiency rise of the proposed converter in comparison with its predecessors. The input DC voltage is shared firstly by two capacitors in this arrangement; leading to the reduction of cost. Apart from SST applications, the proposed inverter topology can be used in a number of industrial applications with small modifications.

A radical structure for fabrication of three phase 15KV high frequency PWM inverter, incorporating high voltage capacitors, IGBTs and medium frequency isolation transformer in half bridge topology perspective for 100 KVA three phase SSTs in energy distribution system has been anticipated. It is also apprehended in hardware laboratory for a half-bridge configuration in downscaled values, where it revealed that these experimental results are consistent and demonstrate good agreement, covenant with the simulation fallouts and confirm the reliability of the inverter. From the measurement, the efficiency of the proposed inverter is found to be at 98% average with reduced THD.

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Abbreviations

1Φ	Single Phase
3Φ	Three Phase
AC	Alternating Current
$\mathbf{B_{max}}$	Saturation Flux Density
BHB	Boost Half Bridge
CTs	Conventional Transformers
DC	Direct Current
DAB	Dual Active Bridge
DHB	Dual Half Bridge
DG	Distributed Generation
DES	Distributed Energy Storage
DER	Distributed Energy Resource
EMI	Electromagnetic Induction
ESAC	Energy Systems Analysts Consortium
ERC	Engineering Research Centre
EVs	Electric Vehicles
FB	Full Bridge
FREEDM	Future Electric Energy Delivery & Management
FEM	Finite Element Method
FET	Field Effect Transistor
HB	Half Bridge
HF	High Frequency
HFT	High Frequency Transformer
HVSC	High Voltage Shore Connection

HV-HF	High Voltage High Frequency
IGBT	Insulated-Gate Bipolar Transistor
KVA	Kilo Volt Ampere
kHz	Kilo Hertz
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
MF	Medium Frequency
MFT	Medium Frequency Transformer
MIT	Massachusetts Institute of Technology
MOSFET	Metal Oxide Semiconductor Field FET
MLI	Multilevel Inverters
MFPT	Medium-Frequency Power Transformer
MVHFT	Medium Voltage High Frequency Transformer
NSF	National Science Foundation
PCB	Printed Circuit Board
PET	Power Electronics Transformer
PF	Power Factor
PWM	Pulse Width Modulation
QAB	Quadruple Active Bridge
R&D	Research and Development
SiC	Silicon Carbide
SMPS	Switched-Mode Power Supply
SST	Solid State Transformer
THD	Total Harmonic Distortion
VSC	Voltage Switch Converter
ZVS	Zero Volt Switching

Symbols

A_e	Effective Cross Sectional Area
ΔB	Transformer Flux Swing
D	Duty Cycle
f_s	Switching Frequency
K	Park's Transformation Equation
K_m	Material Constant
K_u	Window Constant
μ	10^{-6}
V_a, V_b and V_c	Grid AC Voltages
θ_1 and θ_2	Modulation Angles
Φ	Phase
δ	Skin Depth
η	Efficiency

Chapter 1

Introduction

In modern ages, the convolution of the electrical grid has grown up due to the increased use of renewable energy and related distributed generation sources. To manage and cope with this intricacy, new technologies and expertise are vital for better control with reliable and consistent operation of the grid. Among such technologies, the most demanding, innovative and state of the art technology is electronic based transformer, which is known as the solid state transformer. Solid State Transformer technology is quite inventive but presently the acquaintance on accomplishment of these systems in the grid perspective seems to be relatively scarce, inadequate and rather limited. For achievement of more insight into mechanisms of this maneuver, the prevailing exploration will focus and stress on emerging and developing a design of high frequency PWM inverter, being a significant part of transformer isolated DC-DC converter portion of SST. This chapter endeavor's to introduce the concept of SST and discourses its various topologies and configurations with emphasis on their behaviors. Further, it also ponders on the most viable, practicable and workable configuration suited to our requirement coupled with the guidelines for achievement of design.

1.1 Background

Transformer is considered as a vibrant and significant energy transfer device with help of electromagnetic induction [1, 2], operationally making use of Faraday's law

and Ampere's law. Consequently, transformers are incorporated in applications where step-down/step-up of voltage from one level to another level is required; thereby resulting in creation of an electric isolation between two circuits. The three focal ingredients of the modern power system (wherein a power transformer plays the most precarious, vital & steering role) include generation, transmission and distribution. In an overview, in case of Utility Power Transmission and Distribution arrangements, the electrical power delivered by the utilities, is collected from the point of generation to the end user. This phenomenon covers two essential schemes, which are known as the transmission and distribution. The transmission system is deliberated as the most important scheme which acts as a backbone of the utility grid in carriage of the power at the extensive and broader level. These utility power plants are connected specifically to this backbone for transportation of power to local distribution systems, and then on to the user. Transmission lines (operating at very high voltages) transmit electricity to distribution sub-stations where it is further dispersed to commercial, industrial and residential customers. Figure 1.1 elucidates an outline of a centralized power network; thereby emphasizing its transmission and distribution features. An ordinary power plant generates voltages at a rate 11kV or 13kV and among these generations , the preference is given to the produced voltage from 11kV/13kV to 132kV or 220kV and 500kV or even greater [3], with help of step up transformer in order to address losses in transmission at a distant end. Electric power of 11 kV supply is provided at the consumers locations and light industry in our country. The key and main part in high voltage transmission systems is grid station, primarily designed to produce the voltage in either step-up or step-down configuration in a transmission system [3]. The switching, voltage step-down and controlling equipment are arranged in such a manner so that the sub-transmission voltage may be reduced to primary distribution voltage (in residential as well as industrial scenario), thereby constituting the distribution substation. 11kV/381V transformer plays a vital and momentous role in power distribution system at consumer end [4].

In present power distribution system, an unexpected rise of nonlinear loads has been found; where de-rating of conventional transformer is noticed up to 50% if 60% of its loads comprising switched-mode power supply (SMPS) [5]. Similarly

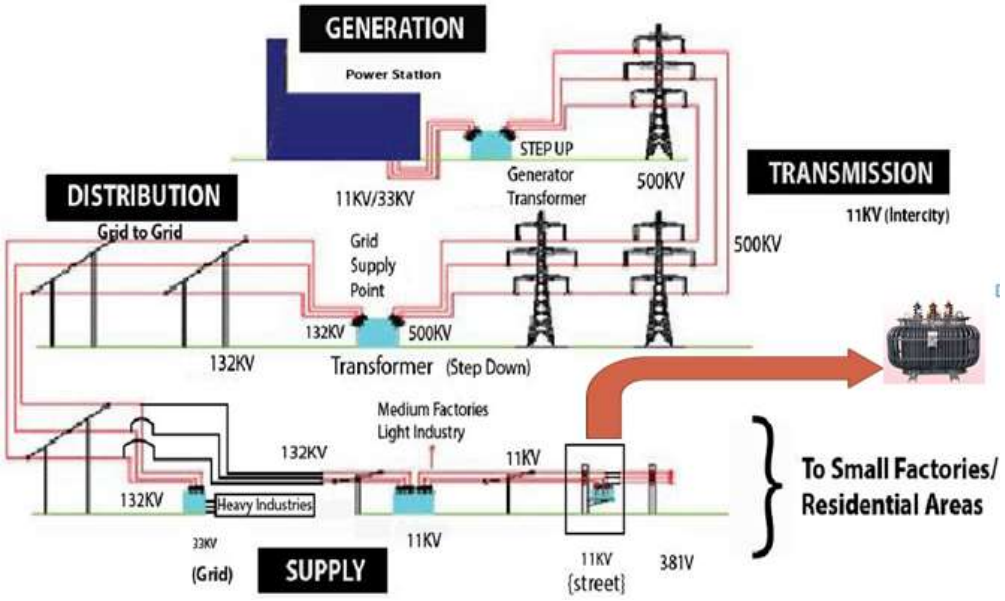


FIGURE 1.1: A figure showing an example for centralized power network [4].

de-rating of power cables and generators also occurs due to nonlinear loads. These electronic (nonlinear) loads illustrate non-sinusoidal currents generated from AC mains thereby causing current distortion, known as "harmonics". Key effect of harmonic currents observed in transformer phenomenon is the additional heat generation [6]. In order to overcome these problems and further to achieve flawlessness and perfections, the scientists have developed an innovative kind of transformers, which are far better and also effective than the primitive ones. Those devices are known as Solid State Transformers (SST) [7].

1.2 Solid State Transformer Technology

During past two decades, SSTs have evolved rapidly and considered the most suitable and appropriate conversion device for replacing the outmoded and obsolete low frequency transformer where volume savings, substantial efficiency improvement and cost economization can be achieved. Various systems and applications of SST technology have been proposed and analyzed. Conceptually the basic perception diagram of SST is the combination of high frequency transformer and power components [8]. From practical aspect, the SST configuration comprises of three main stages (i.e., a rectifier, isolation through HF/MF transformer and finally DC-AC converter to reproduce line frequency AC) [9]. The most promising,

auspicious and practical three stage structure was presented in [10, 11], facilitating the anticipated solution contains low and medium voltage dc buses and completely decoupled arrangement between two AC sources with proficient enough for reactive power compensation.

Till date, the fabrication of SST is in research and developments (R&D) phase [12]. In fact, SST invention is a practical semiconductor scheme adopted to achieve high power density at high frequency exploit, ensuing in reduction of the size and cost. It is also environmentally responsive as no liquid dielectric is incorporated for cooling and other related purposes [13]. SST can be made operational with refined communication interface, which comprises smart metering, diagnostics as well as space control elements. SSTs are also considered for use in single wire earth return transmission systems for delivery of rated voltage to support an extensive range of supply/input voltages; thereby ensuing in a virtuous overall system load regulation [14].

Since SST is the arrangement of power electronics circuits and high/medium frequency transformer; therefore the voltage regulation, voltage dip/sag protection, the fault segregation and DC output are some of its main features [15]. Consequently SST is picked up as the energy routers incorporating both AC & DC interfaces in impending distribution systems [16]. The advantages, accessibility and availability of the functionalities such as power flow control, reduced weight, compact volume, voltage sag ride through capability, voltage outage compensation, direct regulation of voltage, isolation of fault, power factor correction, harmonic isolation, cost effectiveness and environmental friendly make the SST, an enabling technology for future energy systems and applications characterized by space limitations [17, 18]. Many firms as well as research organizations are undertaking study in this prevailing field and committed in analyzing models to suit them in a certain application. It is also estimated in [19] that the SST market would be commercialized in a year or so and demonstrate remarkable growth rate in future.

The concept of SST was initially presented by McMurray [12] during 1968; this perception was basically initiated on solid state switches using high frequency isolation working as a traditional transformer. Solid State Transformer was planned in

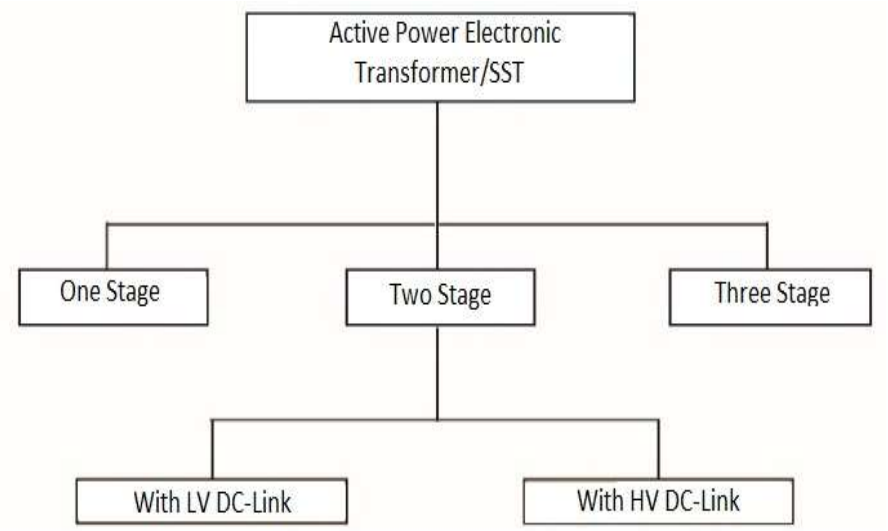


FIGURE 1.2: General classification of SST [20, 21].

National Science Foundation (NSF) Generation-III Engineering Research Centre (ERC) as "Future Electric Energy Delivery & Management (FREEDM) Systems" which came into existence during 2008 and hence then in 2010; the proposal of SST was acknowledged as one of the ten most promising technologies by Massachusetts Institute of Technology (MIT) appraisal [22]. The choice of the most appropriate and veracious configuration for SST execution is a main hallmark, which can be tackled by analyzing a few of the existed latent, possible and promising topologies which can provide unidirectional power course. In this scenario, a number of available topologies for SST (including general AC-AC power Converter) has been deliberated and studied [23]. Some of these topologies and configurations are not in support of the parameter of bidirectional power flow. An effort is undertaken to categorize SST topologies and to earmark the most befitting one as per obvious and explicit needs [24]. Figure 1.2 illustrates the general classification of SST topologies [20, 21].

1.2.1 Single-Stage SST

A number of single-stage topology (direct AC-AC conversion) exists which facilitates a unidirectional power flow; however the lack of DC link is still taken as the major drawback of this topology, which is evident from Fig. 1.3. In the figure, MVAC stands for medium voltage AC as 3300 or 6600 VAC, whereas LVAC defines low voltage AC as 240 to 600 VAC. Here the combination of storage elements

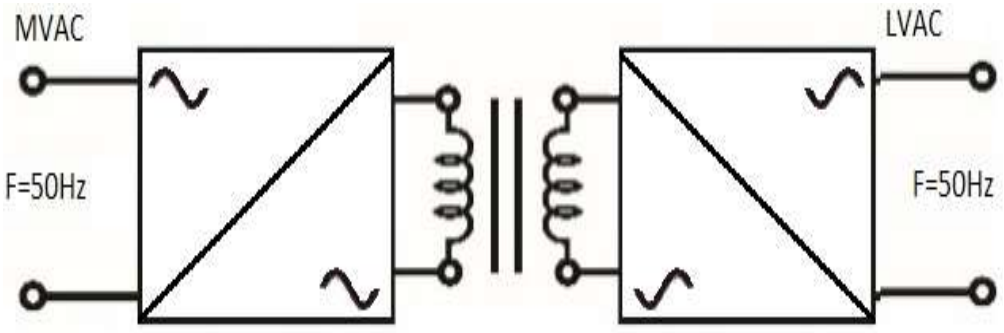


FIGURE 1.3: A single stage topology [25, 26].

and Power flow improvement would definitely demand for extra devices/procedures; which will lead to the system complication, increment in size and cost of the overall system. Yet due to simple and brief configuration, it presently does offer the promising cost and light weight solutions [25, 26]. In overall perspective its advantages include high conversion efficiency, removal of low reliable and bulky component-electrolytic capacitor, whereas its disadvantages include complexity, less flexibility.

1.2.2 Two-Stage SST

A direct current link of this design may not be considered suitable for Distributed Energy Storage (DES) and Distributed Energy Resource (DER) integration, owing to high energy voltage and absence of arrangement for isolation from the grid [27]. However, the fabrication under this arrangement may not be practically feasible in SST applications. It possesses two stage conversions, where galvanic isolation coupled with voltage step down arrangements is addressed in DC-DC converter stage; hence in one of the arrangement, the low voltage DC link does not exist. Figure 1.4 illustrates two stages SST Topology [28].

1.2.3 Three-Stage SST

Three-stage structural design, with two DC links, is the most workable and realistic solution exists due to its high flexibility and control performance characteristics. It ensures numerous purposes and actions which are enviable to SST functions.

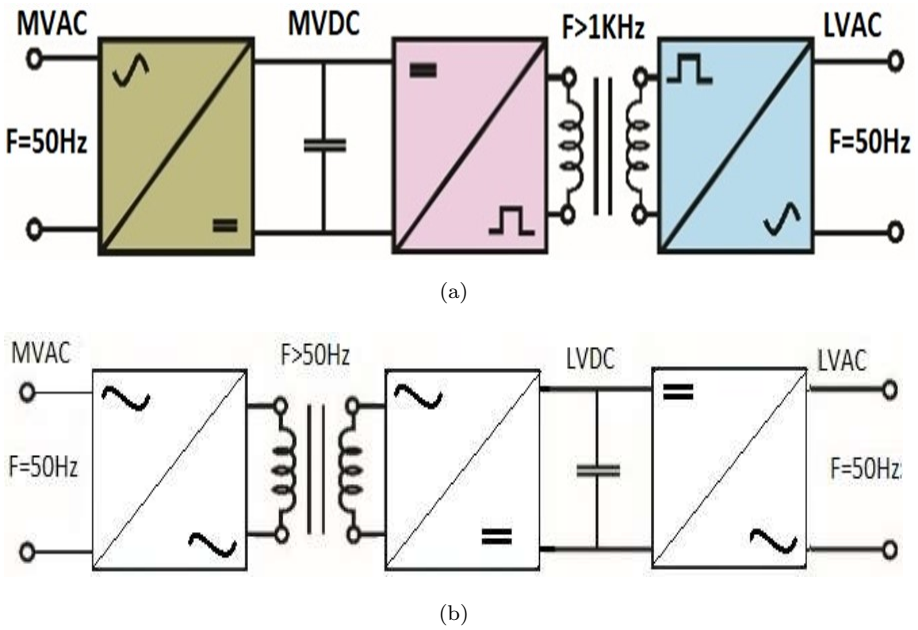


FIGURE 1.4: A two-stage SST with (a) MVDC link and (b) LVDC link [28].

This configuration covers the rectification of AC voltage at the input to a corresponding DC voltage, resulting in MVDC link. Then, this medium voltage direct current (MVDC) is processed to change into HF AC voltage, which is routed to high/medium frequency transformer. At this stage, the voltage level is condensed, rectified once more to a low voltage DC level and finally constitutes a low voltage DC link. At further stage, this obtained low voltage direct current (LVDC) is transformed once more in order to achieve 50 Hz AC voltage. Figure 1.5 exhibits typical arrangement of SST incorporating AC-DC converter, transformer isolated DC-DC converter with ability of galvanic isolation and lastly low frequency inverter. SST with such three stages topology is measured and taken as the most accepted and doable transformer in distribution system; that is why it also referred as a three port power exchanger and energy router [29].

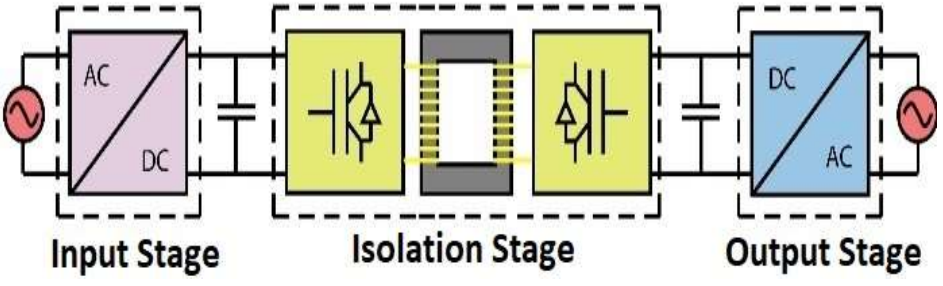


FIGURE 1.5: Block scheme of SST with medium frequency intermediate transformer [29].

It is accomplished from all the aspects that a three stage SST topology is the most appropriate execution. This three-stage contains five parts, equipped with a MVDC/HVDC link for connection of power sources and a LVDC link to connect energy storage devices as one system. It's the most acceptable deliberation because of the absolute separation between two ac sources with proficiency of reactive power regulation. Being energy efficient, their power capability is ten (10) times greater than the traditional transformers [30].

Although SST is considered as an addition of extra cost factor, yet it is preferred to practice owing to its obvious gains and recompenses. Presently SSTs are fabricated/designed in a small quantity by Energy Systems Analysts Consortium (ESAC), ABB, Alstom and US Naval Academy [31]. It increases the overall efficiency of distribution system. Presently the commercialization of SST is very low; nevertheless, it is predictable to take-off within a few years [31].

Identification of the most viable topology proficient enough in supporting additional functionalities in contrast to a regular transformer is of prime importance. In case of single stage SST topology, the absence of a DC-link restricts its operation in integration of renewable energy sources and also exhibits no arrangement for voltage regulation and reactive power compensation; thereby no input power factor correction coupled with complexity and less flexibility. Therefore, single stage topology is not given due consideration in contestants of SST applications for future grid requirements.

Two stages SST with high DC (i.e., HVDC) link is less applicable topology as it is devoid of isolation arrangement from the grid; thereby not complying with smart grid requirements. Moreover, this DC link is not appropriate for distributed energy store (DES) as well as distributed energy resources (DER). The removal of large ripple currents to achieve voltage regulation is the main challenge in this configuration and hence virtually not feasible in SST applications. The DC-AC converter fragment of this topology being a double phase inverter is common for high order SST topologies as well [27, 32, 33].

The most practical topology of the SST is a three-stage configuration (segregated five blocks/parts). It is a topology enriched with high voltage DC link as well as with low voltage dc links. These links are meant to augment the ride through

competency of SST; thereby allowing the improvement of power quality at input as well as output ends. This three stage topology offers all the preferred SST functionalities. The LVDC link contributes for all the anticipated SST functionalities including interfacing DER and DES. The structural design of this topology comprises of distinct rectifier, isolated DC-DC converter (i.e. HF inverter, HFMP/MFHP Transformer and rectifier) and lastly DC-AC converter. This topology offers incredible advantages over the rest of topologies including high flexibility, control performance and weighed as the most workable, practical and realistic solutions [34–37].

1.3 Transformer Isolated DC-DC Converter

A core circuit for high frequency link power conversion system relating to high efficiency and galvanic isolation is the isolated DC-DC converter. The transformer isolated DC-DC converter as an entity and the SST as a system; both these arrangements make use of a high frequency inverter at the primary side of the HPMF transformer for the purpose of production of ac voltage. The transformer isolated converters (DAB or DHB) are used predominantly for provision of galvanic isolation and prevent the transmission of voltage transients to the output. Power conversion using high frequency inverters are attaining improved consideration in scheming high frequency, power distribution arrangements. Researchers and investigators are carrying out extensive study on design of high frequency inverters in different topologies. In bridge arrangement, the vital structures proposed are full bridge and half bridge inverter in step down as well as step up mode; where performance evaluation has been deliberated through experimental results [38–40].

1.4 Power Inverter

Power Inverter is the fundamental and essential part of two stages SST as well as three stages SST. The three-stage configuration is strongly preferred for the connection of power sources and energy storage expedients into one system. A

most challenging and demanding portion from the electronics point of view is the design of high frequency power inverter as a part of isolation stage of SST, which is also called as a transformer isolated DC-DC converter stage. Therefore, in a design perspective, high frequency Power Inverter (being part of 2^{nd} and 3^{rd} SST topology) is the most significant and exciting block of SST, therefore it is preferred for research analysis.

Power Inverters basically are electronic devices used to change a fixed DC voltage into AC voltage of variable (requisite) frequency with fixed or variable magnitude. A power inverter may be entirely electronic or a blend of mechanical effects (like a rotary device) and electronic circuitry. In power system applications, the two mainly employed inverter technologies include Pulse Width Modulation (PWM) inverter and Resonant Inverter. PWM Inverters regulate by adjusting the duty cycle in controlling the width of the pulses in the switching arrangement scenario and therefore are used for the variable loads as in our case. The resonant inverters are electrical converters based on resonant current oscillation and are used for fixed load only. Key function of these inverters is to lessen the switching losses of the devices [41]. Implementation of Resonant Inverter in this case is not supported due to the load limitations as it cannot work on variable load. Hence motivation for fabrication of high frequency PWM Inverter is implemented. In PWM Inverter, PWM techniques play a vital role in controlling DC to AC conversion and offer many advantages such like less generated noise, minimized harmonics and controlled net output voltage [42].

PWM inverter consists mainly of two bridge topologies: (1) Full-bridge inverters and (2) Half-bridge inverters. In inverter fabrication scenario, these two topologies are evaluated in the light of their performance parameters such as cost, size, current ripple, transformer turn ratio, switching power loss etc. The most promising and main difference between half-bridge and full bridge topologies lies in the output voltage. In case of half bridge configuration, this value is half the supply voltage, whereas in case of full-bridge topology it is the same output voltage [43]. Figure 1.6 illustrates the half bridge inverter topology, whereas Fig. 1.7 highlights full bridge inverter topology. Half Bridge Inverter topology is the most favorable for

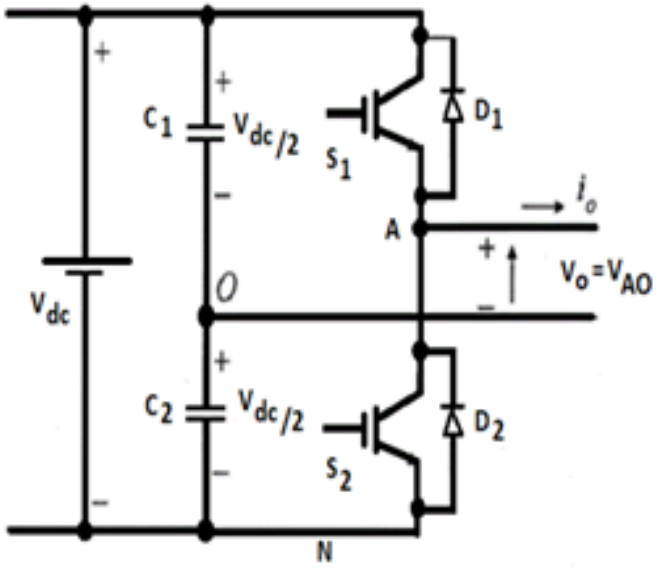


FIGURE 1.6: Half bridge inverter topology [41–43].

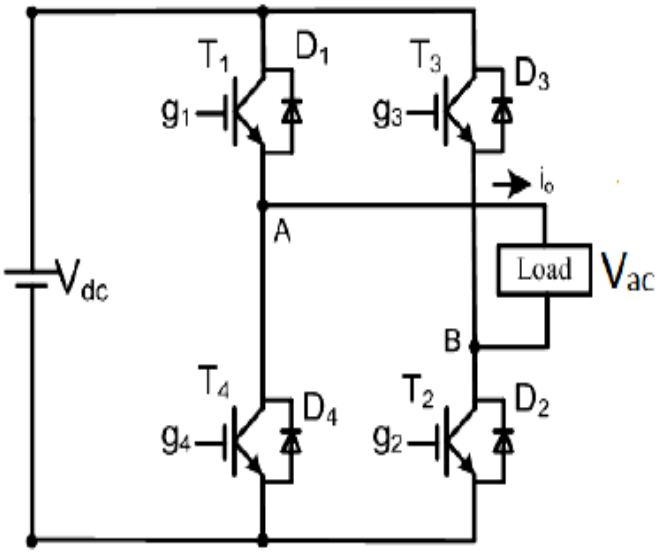


FIGURE 1.7: Full bridge topology [41–43].

implementation as per our system requirement due to a low voltage and half of the supply voltage at the output.

1.5 Limitations of HFTs and MFTs

Transformers are considered and proved to be the most consistent, unswerving and effectual electric expedients. However, the flexibility, improvement in power quality and bidirectional energy controls capability aspects in case of conventional

distribution transformers are found to be deficient, which are considered to be essential in vigorous and energetic distributed networks. These features inspire and encourage the researchers as well as academicians to search for alternatives. Medium-and high-frequency transformers are a fundamental component in many isolated power-converter topologies proposed for electric distribution applications (e.g., solid-state power substations). High power medium frequency transformer is deliberated as one of the vivacious and significant essentials of isolated DC-DC converters in applications such as future all-DC offshore wind farms, traction and solid state transformers. MFT has gained global interest as it is the focal constituent in high power converters and substitutes the conventional 50/60 Hz transformer. The bulkiest unit within future MV conversion structures is the magnetic circuit, and there is an interest to minimize the size of the magnetic circuit so as to reduce overall size and weight of high power converters. With extensive efforts to realize this objective of magnetic circuit size reduction, the method most commonly employed is that of increasing the frequency so as to cut down the volume as frequency is inversely proportional to area product. Low frequency transformer appears to be unsuitable in certain electrical environments and applications, and therefore new design methods are to be employed. The first issue to be considered with the MFT is the type of magnetic core to be used. The characteristics expected from a core material include that it should have a low core loss, high saturation flux density (B_{sat}); and unrestricted continuous operation at high temperatures [44]. High Voltage HFTs are designed to handle up to 15,000 volts safely and accurately using frequencies from 20 KHz to over 1 MHz whereas, high voltage MFTs are designed to handle voltages using frequencies from 400-800 Hz or comparable frequencies [44].

The use of higher switching frequency can lessen the overall size of magnetic elements; but it may result in addition of core/copper losses, ultimately resulting in generation of electromagnetic interference (EMI). Leakage inductance and AC resistance of the windings can ominously impact the efficiency of the transformer. In order to appraise the effectiveness and impact of the transformer structure on the values of leakage inductance, analysis of the transformers with different winding arrangements, considering the skin effect, can be of a prime importance. It

is indispensable to consider the skin effect for obtaining an accurate estimate of the leakage inductance and AC resistance especially in HF/VHF applications. Because of the magnetic field generation due to passing of current, the current is pushed towards the outer surface of the conductor to flow. This phenomenon is baptized as skin effect and results in a lesser exploitation of the inner surface of the conductor; and subsequently, a lesser effective current carrying cross section area. Skin effect intensifies with increase in frequency; thereby, reducing the cross-sectional area. Due to the correlation of the inductance with the cross sectional area, the leakage inductance also decreases. Likewise, with increase in frequency, there is an anticipated increase in resistance of the windings; for the reason as the resistance is inversely proportional to the effective area of the cross section. Henceforth, the inclusion of the skin effect in the analysis is vital [45].

1.6 Applications of SST and Isolated DC-DC Converter

Transformers are established at generating stations end. The distribution substations are used in transportation of electric power at a long distance to the lower voltages required by homes, businesses and other utilities (i.e. with the key function to trim down the high voltages). But today's existed transformers only operate in one direction. Some of the functionalities provided by SST structure include: (1) Protection of load and the power system from power supply disturbances and disorders, (2) Sag and outage compensations, (3) Load transients and harmonic regulations, (4) Unity input power factor (PF) under reactive load, (5) Sinusoidal input current for non-linear loads, (6) Protection against output short circuit, (7) Operation on distributed voltage level, (8) Integration of energy storage and (9) Medium frequency isolation [46].

To implement this technology in a befitting manner, tremendous efforts have been carried out to design SST and reconnoiter its impending application in distribution system. Figure 1.8, on one hand, depicts the customary distribution system incorporating transformer for integrating the renewable energy resources, operating the traction & locomotive system, and interfacing the FACTs devices. The

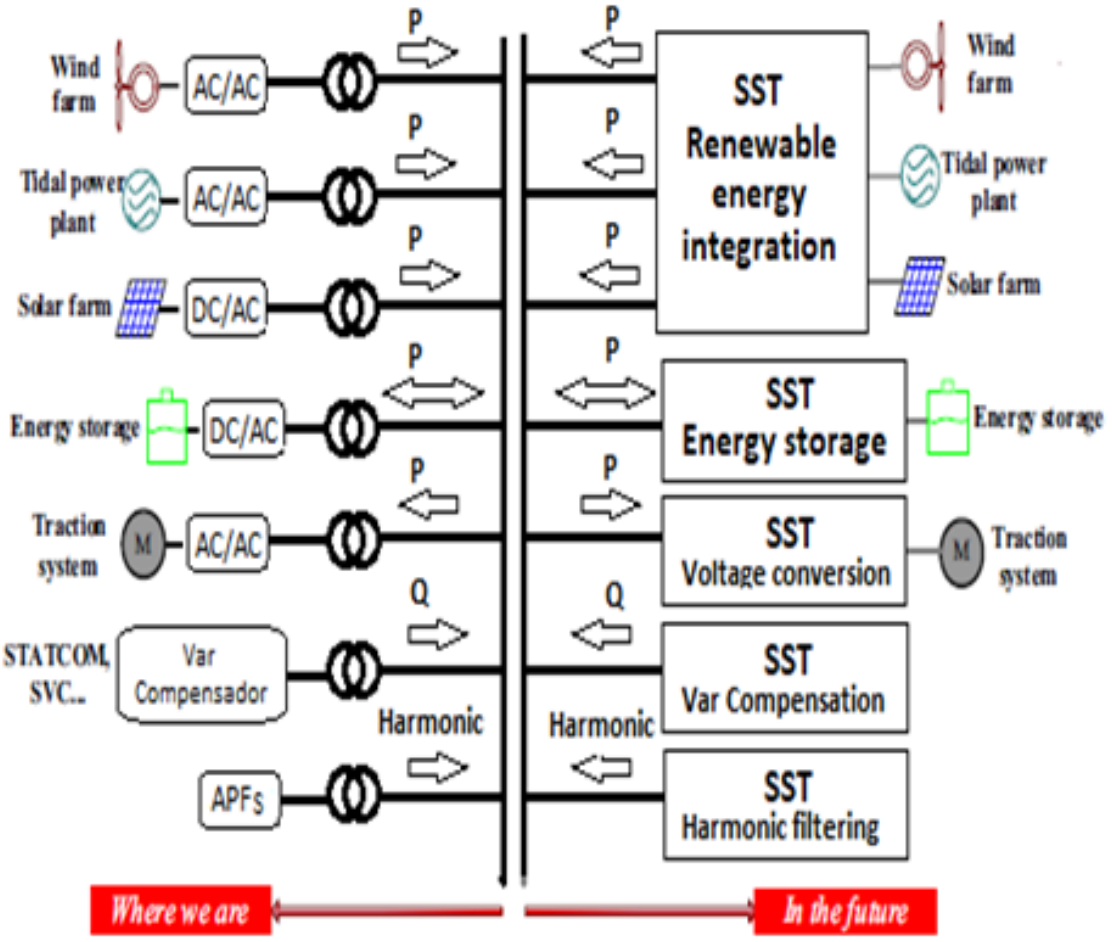


FIGURE 1.8: SST applications in future distribution system [48].

examples include the active power filters and reactive power compensator. On the other hand, this figure also highlights the anticipated impending SST based distribution system. From this study it is obvious that the SST can substitute the traditional transformer coupled with some power electronics with appropriate cohesive and dense system potentials. In addition, the efficiency and cost concerns of the SST may be tackled prudently. Nevertheless, the consistency and lifetime of the SST interfaced distribution system are a concern for the utilities [47].

The applications of Solid State Transformer in certain spheres are much more gorgeous, striking and attractive one. Some of the examples from such applications are: (1) Locomotive and related Traction system as a significant and momentous weight reduction mechanism. It results in enhancement of efficiency and reduction in EMC and harmonics, (2) Desired energy generation as a mean for cheaper offshore platforms, (3) Smart Grid applications for adjustment of energy distribution dynamically, (4) Integration with other energy systems, (5) Applications between

generation source and load or distribution grid to attain unity power factor from energy transportation, (6) Controlling active power between two distribution grids and action as a reactive power compensator for both grids, (7) Connection between the MV-and LV-grid to control the amount of reactive power flow and (8) Action as an interface for distributed generation and smart grids. Diverse applications lead to different requirements.

Figure 1.9 exhibits a schematic overview of SST applications.

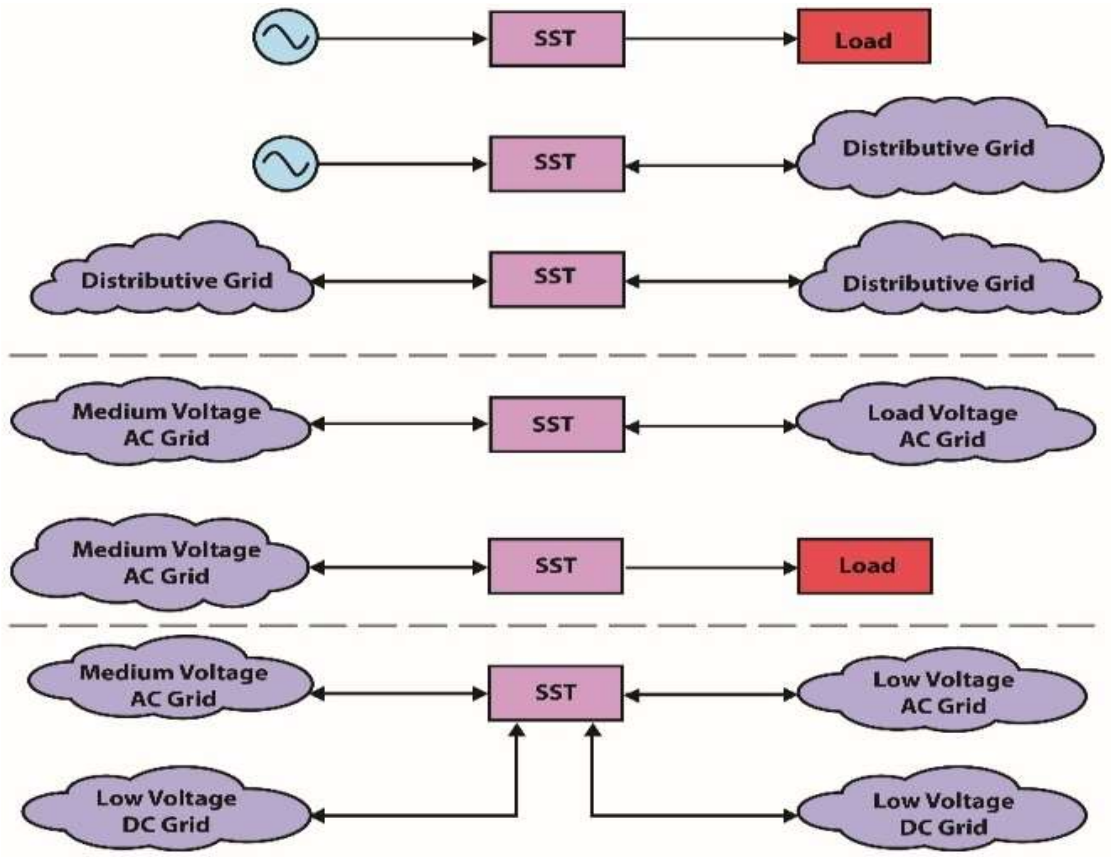


FIGURE 1.9: Schematic overview of SST applications.

For high power conversion, a dual active bridge (DAB) DC-DC converter is considered to be the most appropriate and promising solution, which is in fact a galvanically isolated DC-DC conversion device. Various characteristics and applications of isolated DC-DC converter includes: (1) Being modular, symmetric structure with high power density, is incorporated for multiport operations, (2) Extensively used to interface with the distribution grid on population level (i.e., with the 220 VAC, 50/60 Hz utility grid) [49, 50], (3) Energy or power storage schemes [51], (4) Fuel cells, and interfaces for multiple renewable energy sources (e.g. photovoltaic

(PV) modules [52], (5) Chargers for plugin hybrid electric vehicles (PHEVs) or battery electric vehicles (BEVs) [53, 54], (6) Bidirectional conversion capability supports the growth of smart interactive power NWs, where energy arrangements compose an energetic role for provisioning of numerous kinds of support to the grid (e.g., vehicle-to-grid (V2G) perceptions and (7) AC micro grids and inhabited DC distribution systems (DC nano-grids) [55].

1.7 Perceived Innovation

Low cost, high reliability and greater efficiency are a few attributes to evaluate a conventional low frequency transformer, which are documented for years. However, such conventional transformers contribute towards a number of adverse effects also. Some of these adverse effects contribute in terms of large size (bulky), huge weight, voltage drop under load, power quality susceptibility, harmonics sensitivity, environmental concerns (i.e. leaking of mineral oil).

With the recent advancement of the smart grid infrastructure coupled with increased incursion of distributed generations, there is a firm need to have active power electronic transformers (PET). These inventions and developments may increase and augment the performance of power quality, being a topic of hot research, is an innovative power electronics mechanism in fetching a quantum leap in iron-and-copper distribution transformer technology; thereby facilitating the future smart grid infrastructure in a better manner.

The second block of three staged SST (i.e., high frequency inverter) has been deliberated with focus on enhanced efficiency, low THD, less cost and better voltage regulation incorporating PWM technique.

1.8 Research Objectives

The research objective that follows from the problem statement is:

"Design a 15kV high frequency PWM inverter as a part of 11kV Solid State Transformer".

In order to materialize the problem, following requirements should be met:

- To replace a 100kVA, 11kV/381V Conventional traditional transformer with Solid State Transformer in a distribution system.
- To explore possible topology for SST, suitable for distribution system.
- To search for possible topology that could be used for high frequency inverter.
- To propose an efficient and requisite inverter with possible control strategy.
- To design high frequency DC-AC converter (Inverter) according to the specification.
- To model and simulate a proposed circuit of high frequency PWM inverter in an appropriate simulation environment as a fixed voltage.
- To assess the performance of high frequency power inverter based on its various requisite performance parameters.

1.9 Research Approach

To explore various solutions for the stated problems, it is mandatory to carry out the theoretical, analytical findings and lastly simulations to verify the results. It is mandatory to carry out the theoretical, analytical findings and lastly simulations to verify the results. Simulations would also be required to seek better insights into various scenarios of interest as well as comparisons with previously proposed techniques. The overall methodology will comprise as:

1.9.1 Preliminary Studies

A concrete theoretical basis carries a long way in executing meaningful research. In this aspect, a number of courses as course subjects/course work or otherwise studied before embarking upon research, coupled with research articles/allied materials on the subject is mandatory.

1.9.2 Research Scenario

1. The first aspect of research focused on various aspects of Power Quality (PQ) in this ever-increasing power demand and deliberation on the various issues confronting in this scenario. The power system disturbances which broadly include interruption, voltage sag, voltage swell, flicker, voltage and current unbalance, ringing waves, outage, transients and harmonics, etc. have been studied and comprehended.

2. The second aspect of research emphasized on the solution to address these disturbances in the prevailing advanced power electronic technology. The emerging technology of the transformer i.e. SST as a replacement to conventional transformer was evaluated in term of topologies, applications and its architecture focusing on switching devices. Based on the topologies, classification of SST was studied; in particular, the three stages with a DC link on both sides (i.e., primary and secondary side), was given due emphasis.

3. The third facet of research is the deliberation on three staged (five blocks/-parts) topology of SST with promising characteristic of flexibility and control. In this topology, DC link decouples from the HV/MV at the LV side, facilitating for control of an independent reactive power and input voltage sag ride through. SST comprises of rectifier block, high frequency inversion block, medium frequency transformer block, Low frequency rectifier block and lastly DC-AC conversion at low frequency.

4. Ultimate aim of our proposed research is to deliberate a power inverter (high frequency) as a part of SST with emphasis on efficiency and THD. A performance analysis with PWM technique will be carried out to determine the impact of such adopted technique.

5. The execution of research is carried out into several steps, highlighting different aspects/topologies of Solid State Transformer and high frequency PWM inverters. The steps from literature survey to conclusion and recommendations include:

    i. Literature survey

ii. Derivation of mathematical models

iii. Mathematical analysis of different sections/blocks of SST

iv. PWM inverter design

v. PWM inverter simulation

vi. Assessment of efficiency and THD of PWM inverter

vii. Conclusion and recommendations

1.10 Thesis Overview and Structure

This thesis consists of six chapters, allocated as: **Chapter 1** offers an introduction containing background, SST technologies, isolated DC-DC converter, power inverters, high/medium frequency transformer, applications of SST & Isolated DC-DC converter, perceived innovation, research objectives, research approach and lastly structure of the thesis.

Chapter 2 covers an extensive and elaborative literature review about the design of Solid State Transformer, Isolated DC-DC converter, high frequency Power Inverters and medium frequency transformer. Initially, the merits and demerits of the conventional transformer in contrast to SST are examined and established the credibility of developing SST as a replacement of conventional distribution transformer. Numerous configurations and systems regarding the design and development of SST favoring to our environment are considered in depth and lastly the three stage topology of SST is given due importance. Subsequently, the literature review of SST significant constituents (i.e. isolated DC-DC converter, high frequency power inverter design and high power transformer) is emphasized.

Chapter 3 presents the first contribution of this research thesis. First part of this chapter covers mathematical modeling of three stages SST, focusing on voltage equations concerning rectifier stage, isolation stage and lastly the output low frequency stage of SST. In second part of this chapter, the mathematical parameter evaluation of three stages SST in five block/parts division is analyzed, emphasizing on adoption of full bridge and half bridge topology for power inverters;

thereby proposing three methods. Later it outlines the modeling of inverter with transformer system and also highlights the salient differences between fixed load inverter & variable load inverter. Medium Frequency Transformer in design perspective as a planar transformer in PCB approach is also appraised. Performance parameters of inverter are also deliberated.

Chapter 4 comprises the second contribution of this research thesis. Firstly it highlights the model of the inverter in full bridge and half bridge configurations. Then it concentrates on the design parameter and fabrication of high frequency PWM inverter in half bridge topology perspective. Further medium frequency transformer in ferrite core design is deliberated briefly. Mathematical evaluation of performance parameters of the proposed power inverter model, encompassing the total harmonic distortion (THD) and efficiency are also deliberated concisely.

Chapter 5 presents the outcome received through simulation of the suggested design. It evaluates the anticipated and predicted performance of this design (i.e. inverter efficiency and THD). In a nutshell, the detailed simulation is carried out to show the effectiveness of the proposed PWM inverter.

Finally, this thesis ends with **Chapter 6**, where the major contribution of the work is presented. Some recommendations are suggested for the future to work in this field.

1.11 Summary

In this chapter, the contextual and background knowledge related to the field of Solid State Transformer is accomplished. Being an innovative technology that design will lead to the replacement of the thousands pound (8000-pound) expedient with a small board circuit, while shrinking to a shape more like a suitcase. This significance permits the SST to gain even more attention from different academics setups and industries who intend to use it for various applications with benefits. A detailed discussion on different topologies of SST, overview on transformer isolated DC-DC converter and then subsequently on power inverter devices (highlighting

their advantages and drawbacks) is presented. The significance of high/medium frequency transformer is also taken into consideration. Three stages SST is the most appealing and motivating type, where it can offer all required functionalities for substituting the classical transformer. Similarly on the same analogy, the half bridge power inverter topology is the most favorable for implementation as a part of transformer isolated DC-DC converter as per our system requirement due to mainly presence of half of supply voltage at the output. The subsequent chapter will highlight the motivation for three stages SST, isolated DC-DC converter, high frequency power converter and high/medium frequency transformer, highlighting their virtues and shortcomings in applications and benefits.

Chapter 2

Literature Review

In this chapter, an extensive and elaborative literature has been reviewed for better understanding and comprehension of the work done in the field of Solid State Transformer, DC-DC converter, high frequency inverter and medium/high frequency transformer. Various topologies and arrangements regarding the design of SST, Isolated DC-DC converter, high frequency inverter and medium frequency transformer favoring to our environment were deliberated in depth. After critical reviewing, three stage topology of SST was given due significance and weightage. Subsequently, tabulated literature review summary of the SST and its significant constituents i.e. isolated DC-DC converter design, high frequency inverter design and medium/high frequency transformer are also highlighted.

2.1 Solid State Transformer

Almost three decades back, Navy scholars and researchers anticipated that a Power Electronics Transformer or Solid State Transformer comprised of AC-AC buck converter is used for reduction of input voltage to a bare minimum value. Such proposal was followed by a comparable Electric Power Research Institute (EPRI) sponsored effort in 1995 and during 1997; W. McMurray took initiative in introducing a HF link AC-AC. In 1997, a high-power single stage AC-AC converter

was introduced (i.e. 1st topology of SST). A modified three-staged SST configuration was proposed in 1999. During 2011, SST was established as one of the ten most promising and skilled technologies by MIT technology evaluation, which is currently marketed by Future Renewable Electrical Energy Delivery and Management (FREEDM) Systems Center at North Carolina State University, Raleigh [56–60].

The design and fabrication of 10KVA PET containing three stages, such as rectifier stage, isolation stage, and lastly the inverter stage was deliberated. In this scheme, the end two stages in a sequence were dependent on input or rectifier stage. By virtue of peculiarities, this transformer was called as Solid State Transformer. More ripples in the input current and voltage were observed in design of 10KVA, 7.2KV to 240/120-V SST, which resulted into fluctuation in the output voltage with proportionate decrease in output power. The output efficiency was noted as 90% [61].

A modeling of SST and its uses in PQ improvement was undertaken where in response, the fabrication of 7.2KV-120V/ 240V Solid State Transformer was deliberated. Accordingly a three staged SST topology was implemented, in which Dual Active Bridge (DAB) converter with high efficiency was used. The specified requirements at high voltage frequency were met and optimized by theoretical analysis and experimental tests. The total efficiency of the SST technology recorded was 96.6%. The focal specifications and parameters taken into analysis include: (1) Switching frequency or operating frequency 3kHz, (2) High voltage winding 3.8kV (square wave), (3) Low voltage winding 400V (square wave) and (4) Power rating 6.7kVA. Such specifications are also tabularized in Table 2.1. The measured core losses were of 81Watt, whereas the transformer efficiency measured was close to 97% in the perspective of half to full load range [50]. During analysis, initially one 3.8KV to 400V, 3kHz, 6.7KVA transformer prototype was fabricated and tested with full load and voltage.

The leakage and magnetizing inductance were as per specification requirement with no impact of parasitic capacitance in the circuit. For 3.9kW load and7.0kW load, the efficiency of prototype transformer recorded was 96.9% and 96.8%, respectively.

TABLE 2.1: Specification of HVHF transformer SST system [62].

Parameter	Value
Amount of transformers	3
Switching frequency, f_s	3kHz
DC-DC converter topology	DAB
High voltage DC link, V_H	3.8KV
Low voltage DC link, V_L	400V
Power rating per transformer	6.7 kVA
Minimum insulation voltage	15kV (continuous)
Maximum allowed temperature rise	55°C (nature air cooling)

TABLE 2.2: Specification of designed solid state transformer system [63].

Parameter	Value	Parameter	Value
INPUT DATA			
Power Rating	10kVA	Input Voltage	3.6kV
Input Current	2.78A	High Voltage DC	5.7kV
OUTPUT DATA			
Output DC Voltage	200V	Output AC Voltage	120V
Output DC Current	20A	Output AC Current	50A

The design and demonstration of 3.6KVA-120V, 10KVA Solid State Transformer in Smart Grid applications was reported, where the writers focused on scheme and performance of SST as a lab prototype in smart grid application. Three staged SST topology was adopted in full bridge arrangement. Table 2.2 depicts the specifications of the premeditated SST system for delivery of the power from the 3.6KV AC port to both 120V AC port as well as 200V DC port for residential use with operating frequency of 3.6KHz. It was estimated that the impending efficiency of the SST technology will be much greater (i.e. >97%), provided it is besieged at a mega-watt level design [51].

Figure 2.1 illustrates a three-stage three phase Solid State Transformer. At the input front end stage, cascaded rectifiers are implemented, each having an output of 1.9kV DC. The DAB converter as DC-DC stage utilizes the small component

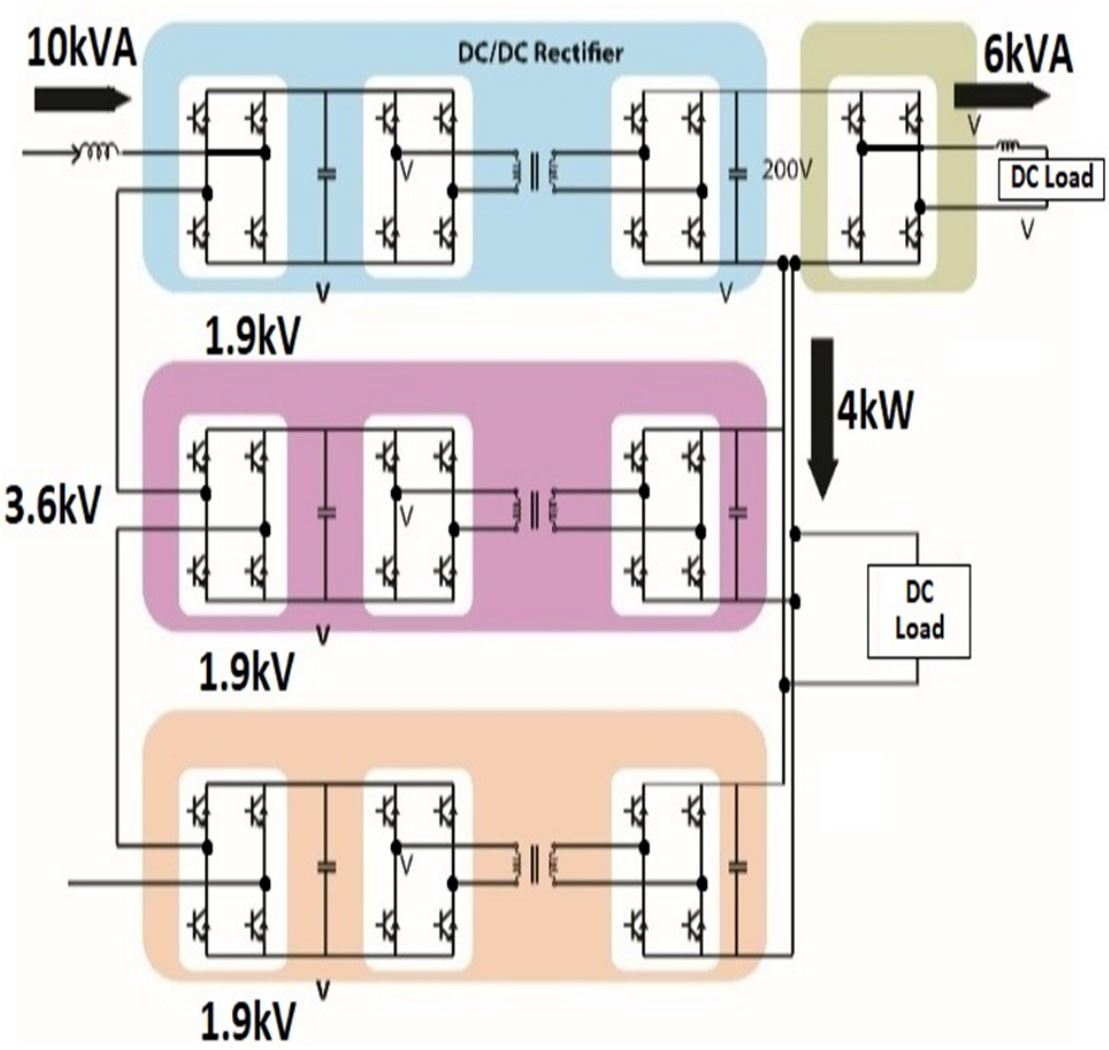


FIGURE 2.1: Three phase SST for smart grid applications [63].

number with improved efficiency and high power density. The parallel combination of the secondary sides of DC-DC converters is facilitated to compromise the low-voltage DC bus in DC micro-grid applications in establishment of a 200V DC with 4kW. The DC-AC inverter being last stage of SST is incorporated for interfacing with residential ac grid, producing 120V AC.

Figure 2.2 exhibits the calculated efficiency for SST prototype design. As Solid State Transformer is anticipated for smart grid applications and facilitate accessibility for AC as well as DC outputs; therefore the efficiency is also recorded for DC load as well as AC loads. It can be observed that during initial three recorded points, only attached DC load is facilitated to the SST, which progressively surges to 4kW with an efficiency of nearby 92%. For the last five recorded points, AC load is gradually increased to 6kW and keeping dc load as constant; the overall

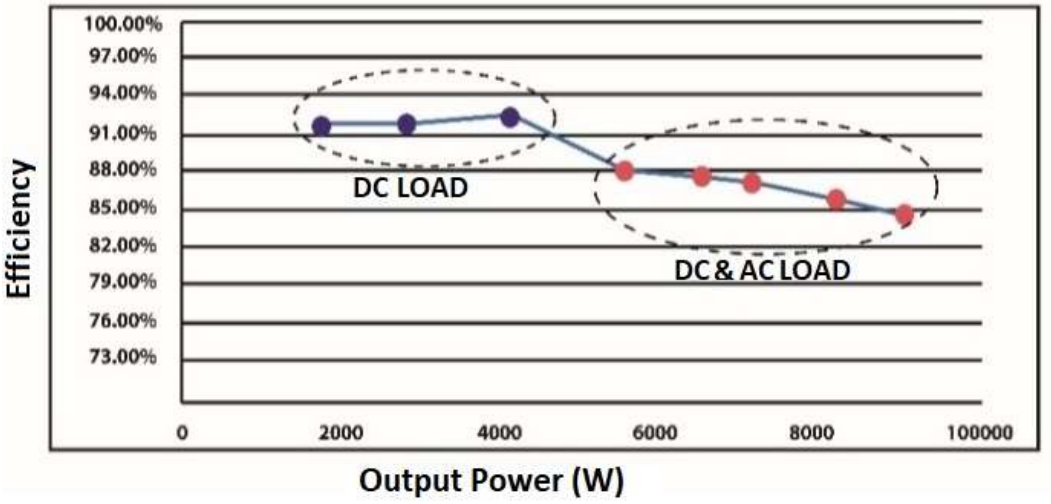


FIGURE 2.2: Efficiency of SST topology [63].

efficiency of the structure recorded in the ranges from 84% to 88% due to the additional DC-AC converter stage [51]. In designing of HVHF Transformer, the ferrite, Nano crystalline and amorphous materials were evaluated in terms of loss, saturation flux density, applications, power density and efficiency. The amorphous core peculiarities in this case provided the space for optimizing the efficiency and chosen as core material [64].

Subsequently a manuscript was presented on modeling & simulation of SST during first quarter 2016, where it was focused on concept and progression in the field of SST, highlighting its various topologies. Brief comparison of those various topologies has been provided. In the end, it was concluded that the conventional transformer is at demerits & disadvantages, because of heavy weight, reduced voltage regulation and saturation of core in case of non-linear load, etc. Almost all such bottlenecks and flaws can be eradicated by solid state power transformer. Such device carries the function of regulating the voltage, rejection of source or load disturbance, micro-grid integration and VAR compensation. In application and usage aspect, in the existing environment, the Power Electronic Transformer is not only confined to distribution level but with advancement of technology it has the ability to substitute the ancient version conventional transformer in near future [65]. In regards to the feasibility and adoptability of power switches in SST applications, an appraisal of 6.5kV 25A Si IGBT with 10kV Sic MOSFET was carried out. In analysis it was concluded experimentally that a 10kV MOSFET

is considered to be superior in frequency switching feature than 6.5KV MOSFET [66, 67].

Active Power electronic transformers (APET), constituting a significant portion of the smart grid was re-emphasized and established that it is a programmable device which can support varying frequency and voltage as per the requirement making use of power electronic converters for the same. Apart from provisioning of galvanic isolation, this transformer could have several applications in a smart grid. The disturbances occur in the system due to input voltage has no influence on the output ones, and vice versa; thereby the most significant aspect of PQ is enhanced in both input and output ports. The EMI level of the environment will increase by augmenting the number of applications of power electronic interfacing smart grid coupled with the compensation for both, active and reactive powers. In later stages [68], APET is incorporated as a typical building block for much complicated/multifaceted structures on HV side to guarantee the power quality.

The possibility of SST application on ships was evaluated, where the most significant features of SST in context of implementation in ship's electrical grids perspective was appraised. This execution can progressively result in lessening of the size of the ship's electrical power system and increment of power quality in grids with lot of reactive and nonlinear loads. In customary ac distribution system, SST has not yet been sparingly vindicated because of inferior proficiency in the AC-AC conversion and demand for supplementary safety expedients. On contrary, it is an auspicious and vital solution for future ships with the MVDC grid and High Voltage Shore Connection (HVSC) systems, due to its capability of the integration of sources/loads with diverse features into one joint grid, mostly energy storage systems. In brief, beside its greater complexity and complication coupled with price, SST technology can provide many more advantages in the marine power system and must be deliberated as a latent solution for enhancing the efficiency and environmental sustainability of future ships [69].

This paper abridged and evaluate the most vital and significant contributions in the field of SST for its control, topologies, construction features, power converter arrangements, and applications /uses. This appraisal also deliberates some novel

approaches for the classification of SSTs, which are not presently comprehended in the reported classification structures, anticipated in the state of art. A widespread discussion and detail on facets interconnected with to the scheme/design and employment of MFTs has also been deliberated in this article. This manuscript also suggests a simple and modest terminology for identification and standardization of the large number of definitions/descriptions and arrangements/configurations currently reported in the literature [70].

2.2 Isolated DC-DC Converter

This review is related to the power electronic conversion schemes, exclusively using a high frequency Link. Isolated DC-DC converter is one of the core circuit for high frequency link power conversion scheme in response to high efficiency and galvanic isolation, which follows generic structure given in Fig. 2.3 [71].

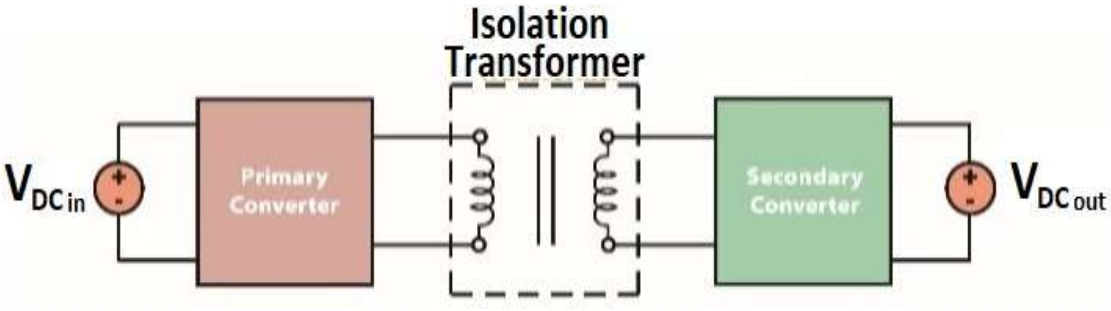


FIGURE 2.3: Transformer isolated DC-DC converter [71].

A new converter arrangement, exhibiting high power performance in digitally controlled device was deliberated. This device connects two half-bridge (HB) inverters in a manner for functioning as a full-bridge (FB) power juncture, incorporating phase-shifting control in zero circulating current. Nominal 50% duty cycle is used by each switch to operate and to attain ZVS over an extensively varying load. For extensive output voltage regulation, it can also operate in PWM. The efficiency of light-load can be enhanced by switching OFF one HB inverter in process. Here 1KW 385–48 V converters is fabricated to authenticate the perception and performances obtained in order to achieve 96% efficiency with high power density for both light and heavy weight [72]. Figure 2.4 exhibits phase shifted full bridge dc-dc converter.

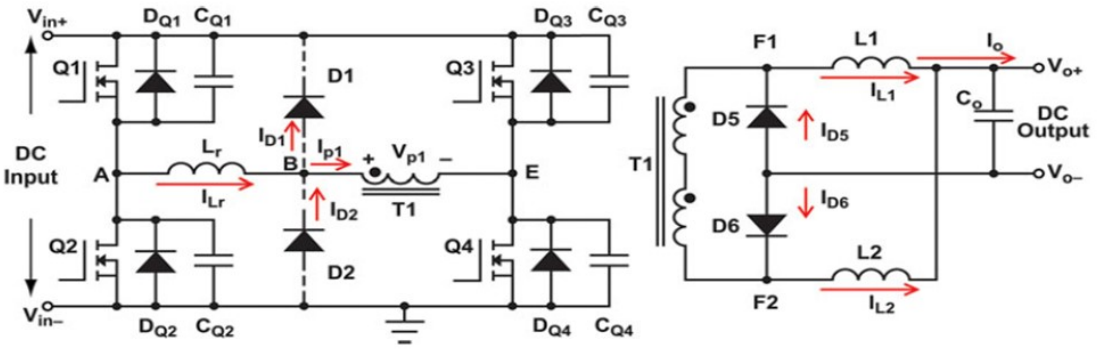


FIGURE 2.4: Phase-shifted full-bridge dc–dc converter [72].

An analysis of three level and two level dc-dc converters was evaluated and concluded that the three-level DC-DC converters in full bridge arrangement possess much more capability of augmenting light load efficiency as compared to DC-DC converters with two-level. Therefore, while designing converter, full bridge isolated type should be given preference and priority over all other types of converters in such scenario [73].

Estimation of losses (i.e., switching and core) in isolated DAB DC-DC converters was emphasized where in response, a conventional phase shift modulation technique was assumed to implement. After thorough analysis and derivation, this approach proposed a new model with switching as well as core losses. In addition, two equivalent resistances are also added in the primary of HF transformer in order to increase the power accuracy and efficiency, taking into considerations the operating conditions. Verification has been established that the switching losses and core losses are primarily realized by the phase shift ratio and the switching frequency [74].

3kW Bidirectional DC-DC Converter for Electric Vehicles (EVs) was proposed, where its prototype was executed to validate its theoretical study and performance which were substantiated by experiment results [75]. This anticipated converter consisted of a half bridge (HB) structure at the input (i.e., on primary side), a HF transformer, and then a dc-ac converter circuit at secondary (output) side. In comparison to full bridge BDCs, this converter was considered as a simple in construction with better anti-imbalance capability in transformer. This converter can be functioned in boost (i.e. step up mode) (29V-380V) as well as in buck (i.e.

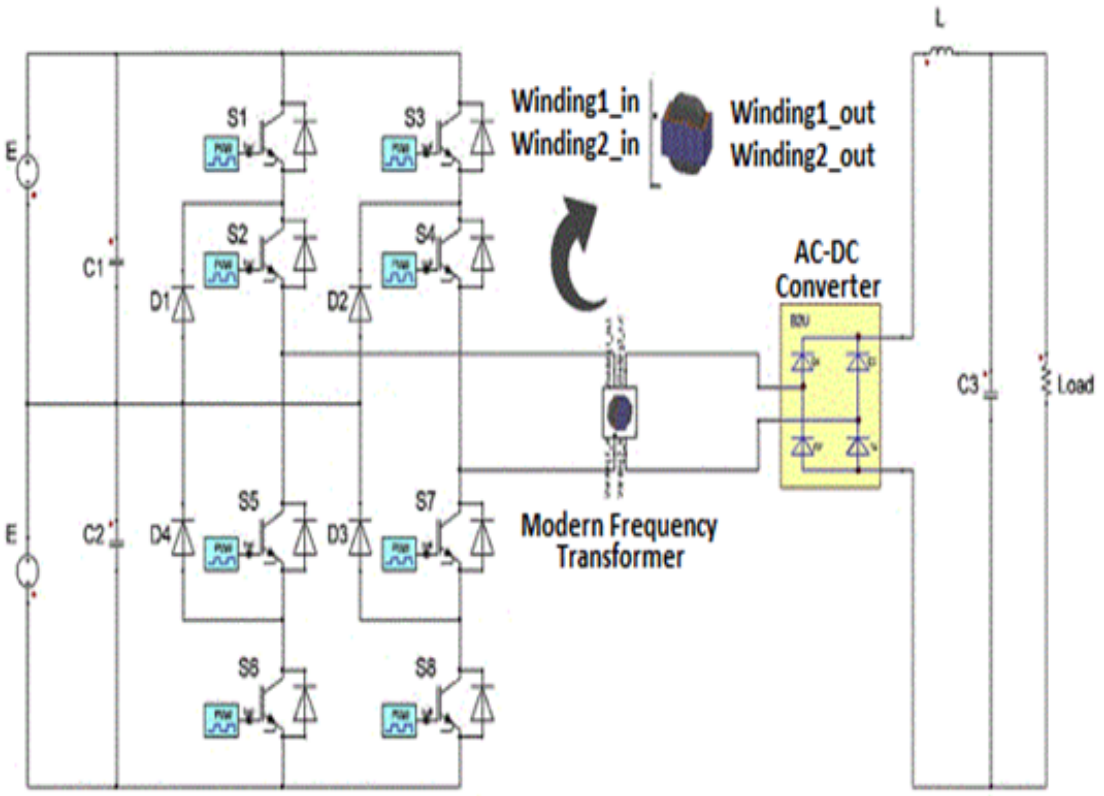


FIGURE 2.5: Isolated DC-DC converters circuit with three-level inverter [77].

step down mode) (380V-29V). In step down mode, the DC-DC converter attained the efficiency in excess of 90%, while in step up mode; it achieved an efficiency of 88.2% [76].

The design and performance study of isolated DC-DC converters in three level arrangements with nano-crystalline core transformer was anticipated, where an effort was made to design a 40V-120V/5kW isolated three levels DC-DC converter in high power and high conversion ratio applications. This design comprised of a single phase inverter (in three levels perspective), MF transformer and lastly a rectifier unit. This MF transformer (with medium frequency range 400Hz-20 kHz) enabled to facilitate high voltage conversion ratio coupled with galvanic isolation. The simulation aspect of this design revealed that the THD value of primary voltage (HF inverter) is reduced from 48% to 37%, whereas this value of primary current (HF inverter) is lowered from 32% to 28% incorporating three level inverter. Moreover, efficiency of such arrangement is increased from 81% to 92% [77]. Figure 2.5 highlights the three level isolated DC-DC converter circuit. Figure 2.5 highlights the three level isolated DC-DC converter circuit.

TABLE 2.3: Design parameters [79].

Parameter	**PS-PWM Converter**	**Proposed Transformer Isolated Dual Step down DC-DC Converter**
V_{in}, V_0	400V, 48V	400V, 48V
P_0, f_0	3kW, 50kHz	3kW, 50kHz
L_0	70μH	70μH
MOSFET	SPW47N60CFD	SPW47N60CFD
Diode	APT100S20BG	APT100S20BG
N_1:N_2	26:4	13:4
L_{lk}, C_i	11μH, None	2.5μH, 50μC

The design and development of a bidirectional isolated full bridge DC-DC converter in ultra-high (UH) efficiency was anticipated. This scheme allowed bi-directional flow of energy without incorporating additional or auxiliary component. In this topology, ZVS was used to achieve lower switching losses and a promising converter. The Simulink design of 1.7kW isolated bi-directional DC-DC converter revealed that in buck mode operation (for DC input) the peak efficiency measured was 80%, whereas in boost mode operation the peak efficiency measured was also 80% with application of input voltage of 52V. This anticipated high power bi-direction converter is very compact in size and has reduced power loss with reduced heat sink requirement. Further hardware design was also executed [78].

A new transformer isolated dual step down DC-DC converter with improved efficiency and with high step down (buck) function has been proposed, employing an extra capacitor at the primary side. This arrangement/design revealed certain limitations such like high circulating current, duty ratio loss, undue voltage spines across the secondary rectifier's diodes and EMI problems. On contrary, this converter can obtain high efficiency and reduced voltage stress, provided it is operated at a wider ZVS range with condensed switching losses. No transformer saturation problem was encountered in spite of mismatch in switch duty ratio. In verification perspective, a 3kW experimental and trial prototype was fabricated and tested. The circuit design parameters of both converters (i.e. Phase Shift-PWM converter

TABLE 2.4: Various DC-DC converter structures [80].

DC-DC Converter	Peculiarities and Characteristics
Isolated	• Reduction in noise as well as in problems related to EMI.
	• Considered appropriate in high power levels applications coupled with meeting mainly utility grid standards.
	• Must possess an exact and precise coupled magnetic design in soaring voltage gain applications.
Unidirectional	• Simple modulation and control, allowing one direction flow.
	• Reduced complexity and expenditure as compared to bi-directional.
Soft Switched	• ZVS and ZCS
	• Greater switching frequency, higher efficiency with improved Power Density.

and transformer isolated double step down DC-DC converter) are given in Table 2.3. The L_{lk} was selected to initiate ZVS around 25% of the full output power (i.e., 750W) [79].

A manuscript regarding specifications of step-up DC-DC converters was distributed where an inclusive and comprehensive appraisal of voltage-boosting techniques and configurations were conducted in a fashion to focus on technological advancement in DC-DC converters in a high voltage perspective. An appraisal of key characteristics of the evaluated structures was deliberated in which drastic comparison and relationship concerning isolated and non-isolated DC-DC converters was established. From study, it was confirmed that only isolated DC-DC converters can compliance to the standards of utility grid, and suitable for high power levels. In high power systems, the use of magnetic coupling (i.e. transformer) has proved to be beneficial in attaining high voltage gain. A bird eye view of key distinctiveness of some of the reappraisal of DC-DC designs is given in Table 2.4 [80].

In this manuscript, a comprehensive model of Dual Active Bridge (DAB) converter in grid-connected PV system application is deliberated. DAB converter comprises of two full bridges of balanced output that delivers phase-shifted transition ac

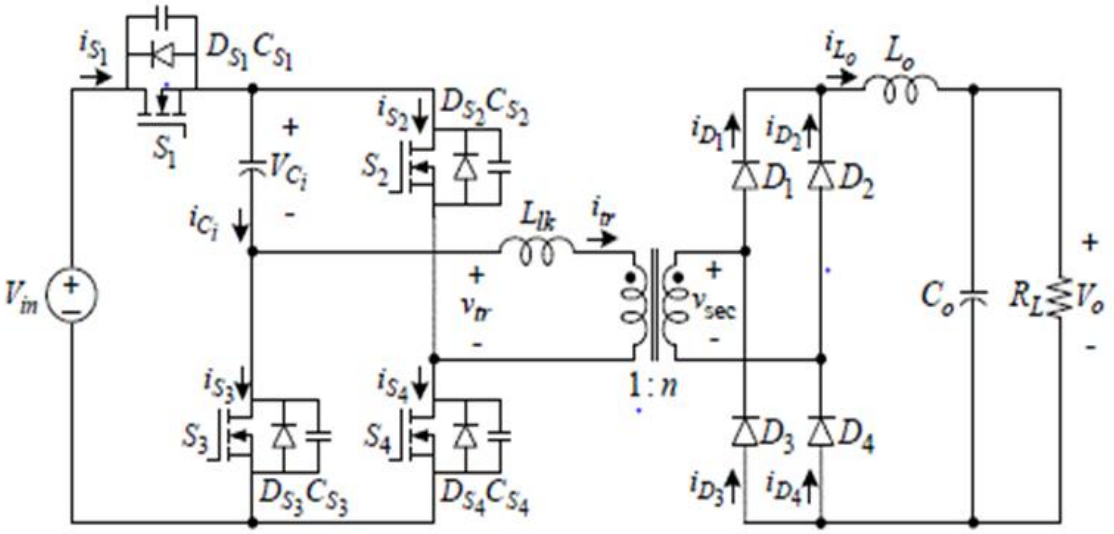


FIGURE 2.6: Proposed double step-down DC-DC converter [82].

square waves to the high frequency transformer primary and secondary sides. In this paper appraisal, the phase shift modulation approach is implemented in order to regulate and adjust the input voltage by controlling the phase shift angle. At the utility grid, the power factor (p.f.) attained is approximated to unity; thereby setting the reactive power current component to zero. Lastly numerous parameters/specifications like input/source voltage of DAB, phase shift angle, DAB secondary side voltages leakage inductor current and grid voltage/current are evaluated by simulation outcomes [81].

2.3 High Frequency Inverter

An isolated DC–DC converter module in HF transformer applications was proposed by Haifeng Fan and Hui Li. The proposed converter was primarily designed as a second stage for 20kVA SST with the perspective of high competence and efficiency over extended load collection. These modules of converter are arranged in a modular design to undertake the low-voltage MOSFETs, for low conduction losses. Further it highlighted the difference in performance between DAB and DHB which ultimately favored the DHB, being an economical with less number of switches requirement. 1KW, DHB converter module indicated the efficiency till 97.2% at 50kHz operation [82]. Proposed double step down DC-DC converter is shown in Fig. 2.6.

A comparative analysis of multi- level inverter and its PWM schemes was carried out, where it was highlighted that a very simple inverter can give the output of two or more voltage level depending upon the switching techniques established. Multilevel Inverter exhibits multiple advantages in electric utility applications and at industrial level for enhancement of power quality with reduced harmonics [83].

A three phase inverter with PWM control scheme was suggested, where its performance was analyzed in depth through simulation, implementing it in a prototype scenario. These three phase inverter designs were effectively implemented with improvement in the system effectiveness and efficiency. By altering the duty cycle of the inverter, the load impedance can be adjusted with source impedance, so that the efficiency may be improved in real time [84].

A design of DC-DC Converter incorporating H6 Bridge was reported, where six level solutions for single phase grid connected converters was deliberated. For provision of a two or more output voltage levels with decrease in switching power losses and EMI, the converter topologies made use of midpoint of dc link. In a practice, a five level inverter provides an improved efficiency up to 95%, which is more than the conventional DC-AC inverters. It is further emphasized that the output voltage with five levels is certain in case of unity power factor; otherwise the converter may produce only three voltage levels; thereby resulting in an increased total harmonic distortion and the switching loss [85].

Practical proposal of DAB converter as an isolated bi-directional power interface in SST uses has been proposed, wherein the DAB converter was deliberated with help of detailed mathematical model. For improvement of overall efficiency, a systematic approach was followed for coupling inductance and dead time duration. Moreover, with help of effective soft start algorithm, the inrush current through the switches was significantly suppressed at the startup state of the DAB converter. Experimental validation of a designed 3.3 KW prototype DAB converter was implemented for practical feasibility and functional [86]. During the same year, a literature survey on multilevel inverters and its related various parameters was conducted. It concluded that the MLI possesses three major topologies such as, capacitor clamped, diode clamped and cascaded. The object behind reviewing

was to focus on MLI's various types and their related operations in the power electronics field. This paper gave the survey of almost 10 papers related multilevel inverters technology [87].

The performance appraisal for diverse multilevel inverters application in renewable energy resources scenario was executed and focused that the cascaded multilevel inverters (required in high power applications) are extremely promising and attractive, having plenty of advantages as compared to traditional ones. Large number of levels in case of ML inverter definitely gives improved performance in the system. The experimental results also validated that the eleven levels inverter gives more efficient performance in terms of the PF, THD and its efficiency as compared to 7-9 level multilevel inverters. This study also highlighted the use of inverter in renewable energy system duly implemented in power system because of various advantages it merited. With increased number of levels, the inverter gives better performance in the system; therefore these are required for high power applications. In conclusion, this paper analyzed various levels inverters, drew comparison between 7, 9 and 11 levels multilevel inverters and evaluated their performance by simulating circuit in MATLAB/SIMULINK [88].

A design and development of 3 Phase PWM Inverter was presented in IJSRD Conference on Emerging Trends, Challenges and opportunities in Power Sector. It was emphasized that in an experiment, once a three phase ac power of 0.8V is provided to the inverter from the function generator, displaced by 120 phase shift, it resulted into an almost sinusoidal current wave. The amplitude modulation index was noticed as less than one and the frequency of carrier wave was 500Hz and 1kHz. The output was measured across the resistive as well as inductive load as described in [89].

A comparative study of multilevel inverter topologies was carried out, where it's some significant topologies (such as Diode-Clamp, Capacitor-Clamped, Cascaded multi-cell and generalized multilevel cells inverters) were deliberated. Applications of these topologies were studied and provided the appraisal of the power component requirement per phase leg, emphasizing on main switches and main diodes (as a requirement for the inverters to obtain the same number of voltage levels) and

advantages and disadvantages of these topologies. At the end it was concluded that the cascade H-Bridge possesses some advantages due to its easy extensibility to high number of level and implementation [90].

The multilevel converters review in application of SST was conducted and published, where an appraisal of potential topologies related to rectifier, inverter and DC-DC power converters was presented. A three level NPC converter branches fabricated with 3.3KV IGBTs exhibits an efficient solution both for MVC and DC-DC converter block. In MVC scenario, full bridge solution was planned in maximizing the operating AC voltage, whereas half bridge solution was preferred at MV side of DC-DC converter. Three phase DAB (with 3L-NPC half bridge) ensured the lowest part number, facilitating for achievement of very high DC gain. These systems are expected to display high efficiency, high switching frequency, and considerable reduction in converter passive elements volume, weight and cost. Current studies propose that three level topologies are promising solution for LVC. It is also emphasized that HB configuration produces half the output voltage than full bridge in order to reduce the turn ratio by a factor of 2 [91].

A 7-level inverter for provision of the output with compact number of switches was proposed. Such proposal was considered as an efficient and effective substitute for the conventional one. It also deliberated on suppressing the circulating current occurring due to phase shift pulse modulation, and verified by simulation process. With rise in frequency, the THD decreases [92].

The optimum scheme of a multiple-active-bridge DC-DC converter for Smart Transformer has been proposed, in which the author deliberated quadruple active bridge (QAB) as an elementary block to contrivance a modular smart transformer. Efficiency and development charges are the two most promising aspects considered in any system; therefore in fabrication scenario, the author was very much cautious to augment the efficiency. In order to meet the set goals and objectives, a multi-objective optimization algorithm was developed. Such algorithm has combined these parameters to have prime point for expenditure. From these experiments and development, an effort was made to design a 20 kW prototype, and then it was experimented. The test results of this design revealed an efficiency

up-to 97.5%. Further, the converter's dependability on various semiconductors technology is concerned, it was proved and substantiated that the Sic MOSFETs are taken to be much more beneficial, due to its small and lower energy losses. Accordingly, the use of Sic-MOSFETs has contributed in reduction of converter's losses to approximately 57%, as compared to the IGBT switches. Therefore, these outcomes established the promising viability of this skill and occurrence for such uses [93].

2.4 Inverter Bridge Topologies (Half Bridge and Full Bridge)

Review of multilevel converters in application of SSTs was carried out, where it was deliberated on AC-DC conversion and DC-DC power conversion topologies being applied in SST applications. It highlighted certain features of each solution with an emphasis on multilevel topologies linked to the medium voltage AC grid. These applications resulted in maintaining the improved efficiency, low loss & high switching frequency, reduction in converter passive element's volume/weight and reduction in overall system price. Further it also acquainted that a Half Bridge (HB) arrangement produced half of the output voltage as compared to full-bridge (FB) configuration, due to which the transformer turn ratio is reduced by a factor of two, ensuring the lowest part number, with a very high DC-gain [91].

A feasibility appraisal of DC-DC converters in both configurations (i.e. Half Bridge and Full Bridge) in high power applications was assimilated, where it was deliberated on DC-DC converter in half and full bridge arrangements for high-power (200kW) and high-voltage (3.6 kV) uses . The emphasis was laid on primary or input part of these topologies, in particular on practicability of the substitution of two HV IGBTs in full-bridge (FB) configuration with two HV film capacitors in half-bridge(HB) arrangement. Features and parameters resulted from the HB topology and FB topology analysis is illustrated in Table 2.5 [49]. A study on grid-connection half-bridge PV Inverter system for power flow controlling and active power filtering was conducted. It was reflected with due emphasis that in case of half bridge PV inverter, the quantity of active switches is less and reduced to half

in comparison to FB topology. This contribution results in a system simplification and reduction in cost [94].

A study on performance investigation regarding Full Bridge, Boost Half Bridge and Half Bridge systems in Phase Shift converter applications was conducted. The performance comparison of three topologies (i.e. FB, HB and BHB) was carried out in depth. The analysis contrasted on the characteristics and features such as cost, size, reliability, efficiency, switching loss, number of signals, power flow range, and complication aspects, etc [60]. Table 2.6 summarizes these normalized parameters.

TABLE 2.5: Comparison of half bridge and full bridge topologies (normalized values) [49].

Parameters	**Half Bridge (p.u.)**	**Full Bridge (p.u.)**
Input/Source Voltage	1.0	1.0
Output Voltage	0.5	1.0
Peak Collector Current	2.0	1.0
Average Collector Current	1.0	0.5
Collector Current (rms)	1.414	0.707
Inverter Switch Current	3.394	3.394
Active Switch Utilization	3.394	3.394

The harmonic reduction in a single phase half bridge inverter was addressed experimentally and verified that at normal condition, up-to 15^{th} harmonics there existed 44.999% THD in a single half bridge inverter. However, with the implementation of LC low pass filter, THD was reduced to 0.0183%. Therefore a vast improvement was resulted with use of LC low pass channel [51]. In published paper concerning feasibility study of 200KW HB and FB DC-DC converters using 6.5KV IGBTs, it was furnished that while drawing comparison of prices for 6.5KV/200A IGBTs and replacement price for procuring of power capacitors, the HB design carried real advantages for all ranges of switching frequencies than others. As per estimation, the HB provided a gain of 40% in comparison to two extra IGBTs in FB design [95].

TABLE 2.6: Normalized performance parameters [60].

Parameters	**FB (p.u.)**	**HB (p.u.)**	**Boost HB (p.u.)**
Cost	1.00	0.86	0.61
Size	1.00	0.91	0.67
Control Complexity	1.00	0.85	0.85
Current Ripples	0.98	1.00	0.10
Switching Power Loss	1.00	0.50	0.14
Power Transfer Efficiency	1.00	1.00	0.80
No. of Switching Devices	4.00	2.00	2.00
No. of Driving Signals	2.00	2.00	2.00

The importance of VSI as an efficient, reliable and higher dynamic responsive inverter has been highlighted [96]. Use of PWM technique resulted in reduced THD and improved spectral quality of the output. The performance appraisal of unipolar and bipolar PWM techniques for single phase VSI was undertaken and concluded from simulation aspect that the unipolar modulation has lesser THD (about 0.368%) as compared to bipolar with better power quality.

A topology for PET is proposed in a modular bi-directional Power Electronic Transformer which contained three parts, each basing on H-bridge configuration. A topology for PET is proposed in a modular bi-directional Power Electronic Transformer which contained three parts, each basing on H-bridge configuration. For 5kVA at 20kHz high frequency transformer, the power and efficiency measured for its sub parts is given in Table 2.7. The efficiency of HF inverter deduced and calculated from the data, approximated to 97.25% [97].

TABLE 2.7: Measured power [97].

Name	**Power in (W)**	**Power out (W)**	**Power loss (W)**	**Efficiency (%)**
CHB Rectifier	591	552	39	93.4
DC-DC Converter	552	509	43	92.2
CHB Inverter	509	476	33	93.5

A design and performance exploration of three level isolated DC-DC converter with the transformer (Nano-crystalline core) is being reflected and further elucidated the design of a 40V-120V; 5kW isolated three levels DC-DC converter for high power and high conversion ratio applications. The simulation results of this proposed structure revealed that the THD value in regards to primary voltage (HF inverter) is reduced from 48% to 37% whereas THD value of primary current (HF inverter) is reduced from 32% to 28% incorporating inverter with three level. Overall efficiency of the system has improved from 81% to 92% [98].

A manuscript on a Fully-ZVS, minimum RMS Current Operation of the Dual-Active H-Bridge converter using closed-loop has been presented. Three Degree of Freedom Control, was produced and investigated that by which of the means, the duty-ratios of two windings in HB legs pertaining to DAHB converter can be utilized in combination with phase shift control. The reliable annotations of circuit waveforms under optimum environments revealed that the closed-loop control-based, real-time rms current minimization approach is quite accessible. This technique does not require the information regarding the converter's voltage-gain; therefore dc voltage sensors are not included in the circuit (when active sources are engaged). Moreover the process at the optimal point at essential situations towards ZVS turn-on of all devices (through the power range of the converter) was also proven satisfactory. This technique provided a vibrant response of converter with substantial efficiency leads over the conventional square-wave control or 2D optimization approach, especially at light loads [99].

A new design of SST using an intelligent program has been proposed in order to get an optimum high frequency procedure, for attainment of maximum efficacy. This SST possessed three stages; the input stage, isolation stage (three levels half bridge convertor connected with HF transformer) and the output stage. This novel scheme has the lead of improving and augmenting PF, voltage swell, voltage sags, reactive power compensation, eradicating harmonic and protecting it with minimum volume, compared to the traditional transformer [100]. Appendix A illustrate the summarized literature appraisal of Solid State Transformer, DC-DC converter and high frequency inverter, respectively.

2.5 Emergent Growth – Isolated DC-DC Converter

A transformer isolated DC-DC converter stage in high frequency perspective is considered the utmost significant and vital element of SST system. Conventionally, the frequently used practical devices in practice are the high voltage IGBTs, basing on 3 level NPC topology; however 1.7kV IGBT with low cost can be incorporated for certain applications. With emergent of wide band gap devices, the DC-DC stage working frequency is escalating even up-to to 50kHz. DAB converter is experienced the most frequently used topology with high performance [101, 102].

LLC unregulated resonant Converter (DCX) is already in practice by ABB [102, 103]. System efficiency has improved gradually. From the magnetic aspect, owing to the enlarged working frequency, the Nano-crystalline and Mn Zn ferrite are the tremendous and frequently used core materials [104]. The transformer structures mostly adopted are still UU core shape [63, 105, 106] as well as EE core shape [107–109]. Litz wire is used in almost all the transformer windings, so that frequency current conduction loss can be reduced [110]. Most transformers are using dry type insulation method and ABB is already moving to oil immerse insulation due to its 15kV medium voltage application [111, 112].

2.6 Transformer as a Galvanic Isolator of the DAB and DHB

In present electronics arena, the medium voltage high frequency transformer (MVH FT) design has been attracted by global interest, which is considered to be a key and decisive fabrication as galvanic isolator of DAB and DHB. The performance dictated is constituent in the region of existed conventional 50/60 Hz transformer, the heaviest high power converters. By virtue of it's expected and review performance, the MVHFT is likely to substitute and replace the present weighty entity within future medium voltage and high voltage conversion structures. Such structure is the magnetic circuit, to be incorporated for minimizing and curtailing the mass of the magnetic circuit in order to obtain commendable reduction in overall

volume of the high power converters in accordance with the prevailing advancement in technology. With wide-ranging determinations to comprehend the mission of magnetic mass reduction, the methodology most universally implemented is that of increasing the frequency so as to cut down the volume, for the reason that frequency is inversely proportional to area product. The transformer with low frequency performs unsatisfactorily in certain electrical applications. Therefore in this context novel strategy have to be devised. To start with, the first and foremost issue to be deliberated with the MVHFT is the type of magnetic core to be undertaken. The features and characteristic to be anticipated for a core substantial are that it must have a high saturation flux density (Bsat), low core loss, and can constantly be operated at high temperatures [113].

In comparison to conventional transformer, the solid state transformer incorporates power electronic converters using high frequency transformer. The power switches such as MOSFET, IGBT etc. are used tremendously. The high frequency transformer plays a vital role in designing and functionalities. It examines and scrutinizes the efficiency aspect mainly reliant on the operating condition and selection of wire/core. Although the high operating frequency does contribute for the transformer compactness and density, but; there are many more limitations which have to be taken care of, such as insulation, power loss and the cost.

There are two types of losses which contribute in total transformer losses [114]; these include core losses (no load loss) and the winding or copper losses (load loss). High frequency transformers in SST primarily cater for the performance and overall efficiency; that is why, it is imperative, rather mandatory to pick up the suitable and right materials with optimization of the design for accomplishment of all necessities and rationales in the operating condition. Various types of core material characteristics are briefly summarized in Table 2.8 [115].

2.7 Critical Appraisal - Discussion

Literature Review in its critical perspective highlighted the comparison of the three topologies of SST coupled with the most viable and practical one for the SST

TABLE 2.8: Core material specifications [115].

Characteristics / Specification	**Nano-crystalline FT-3M**	**Ferrite 3F3**	**Super Alloy**	**Amorphous 2605SA**
Saturation flux density, B_{max} (T)	1.23	0.45	0.79∼0.87	1.57
Curie temperature, T_c (°C)	570	200	430	392
Maximum operation temperature (°C)	150	120	125	150

applications. It also emphasized the transformer isolated DC-DC converter with performance in comparison to DAB and DHB arrangement significantly. Lastly the DC-AC converter (inverter) in bridge configuration was deliberated profoundly.

2.7.1 Solid State Transformer Architecture

An identification of the most suitable and appropriate configuration competent enough in supporting additional and supplementary functionalities in contrast to a regular transformer was carried out. These functionalities included as: (1) On-demand reactive power support to grid, (2) Voltage regulation, (3) Power quality and (4) Current limiting and provision of DC bus. The configurations considered were bidirectional dictating a minimum requirement of substituting a regular existed transformer. A critical, influential and significant analysis of three main topologies for implementation of SST was deliberated and came to conclusion as per succeeding paragraphs.

A single stage SST topology is a configuration without a dc-link, which intensely restricts its operation in integration of renewable energy sources and energy storage devices. This deficiency of dc link also exhibits no arrangement for voltage regulation and reactive power compensation; hence no input PF correction. Therefore, single stage topology is not given due consideration in contestants of SST applications for future grid requirements. Two stages SST with high DC (i.e. HVDC) link is less applicable topology as it is devoid of isolation arrangement from the grid, thereby not complying with smart grid requirements. The removal of large ripple currents to achieve voltage regulation is the main challenge in this configuration and hence virtually not feasible in SST applications. The DC-AC converter fragment of this topology being a double phase inverter is common for high order SST topologies as well [116].

The most feasible and appealing practical topology of the SST is a three-stage configuration (segregated five blocks) (i.e. topology with high voltage (HV) as well as with low voltage (LV) DC links). These links are meant to enhance/enhance the ride through competence of SST; thereby allowing the improvement of power quality at input as well as output ends. This three stage topology offers all the preferred SST functionalities, simplifying the control design. The LVDC link contributes for all the anticipated SST functionalities including interfacing DER and DES. The structural design of this topology comprises of distinct rectifier, isolated DC-DC converter (i.e. high frequency inverter, HFMP Transformer and rectifier) and DC-AC converter stages. This topology offers tremendous merits/advantages over the rest of topologies including high flexibility, control performance and weighed as the most workable, practical and realistic solutions [116]. Table 2.9 gives overview of SST Topology comparison in all possible functional parameter perspective.

In appraisal of the proposed inverter design with the rest of the existed configurations/ topologies of inverters deliberated during literature survey, following have been deduced from the simulation test / trials as well mathematical evaluation. The significance of the half bridge configuration is emphasized in terms of its output voltage, the number of bridges, the driving switches and the design complexity. These are the few parameters which merit for the low cost and circuit simplification. The half bridge arrangement is adopted for the reasons as: (1) output voltage is half as compared to full bridge voltage requirement (i.e. step down) (2) number of bridges requirement is half as compared to full bridge topology (3) simplification of a power scheme layout (4) the reduction in complexity of control and protection circuit (5) significant saving/reduction in inverter price/cost and (5) the attainment of substantial and significant converter efficiency.

IGBTs semiconductor switches are adopted in the inverter system for the reason that these are easier to use, faster, and are available in higher voltage/current ratings. These devices carry the merits of both MOSFETs and BJTs. Like MOSFETs, possess high switching speed with high impedance and like BJTs, produce high gain and low saturation voltage.

Table 2.9: Solid state transformer topology comparison.

Functional Parameter	**Single Stage (AC-AC conversion)**	**Two Stage with LVDC link**	**Two Stage with HVDC link**	**Three Stage with both HVDC and LVDC links**
Input Power Factor Correction	No	Yes	Yes	Yes
DC Link Provision	No	Yes	Yes	Yes
Galvanic Isolation from grid	Yes	Yes	Yes	Yes
DES and DER Management	No	Yes	Yes	Yes
Feasibility in SST applications	No	No	No	Yes
Cost and Weight	Lowest	Lower	Lower	Low
Input Voltage Regulation	No	Good	Good	Very Good
Output Voltage Regulation	Poor	Good	Good	Good
Reactive Power Compensation	No	Yes	Yes	Yes
Circuit Implementation	Simple	Simple	Simple	Simple
Ride through capability of SST	No	No	No	Yes
Power Quality Improvement	No	Yes	Yes	Yes
Bi-directional Power Flow	No	Yes	Yes	Yes
Input Current Limiting	No	Yes	Yes	Yes

2.7.2 Transformer Isolated DC-DC Converter

The isolated DC-DC converter as an entity and the SST as a scheme; both these arrangements make use of a high frequency inverter at the input side of the HPMF transformer for the purpose of production of ac voltage. The transformer isolated converters (DAB or DHB) are used predominantly for provision of galvanic isolation, augment safety, boost noise immunity and prevent the transmission of voltage transients to the output. Therefore, DC-DC converters in transformer isolation scenario are taken into literature appraisal. With ongoing technological advancement in power electronics, the research in this field is very active and updated; where a number of research papers and articles are published as evident from papers as referenced as [76–78].

Power conversion using high frequency inverters are achieving improved consideration in scheming high frequency, power distribution arrangements. Power conversion using high frequency inverters are achieving improved consideration in scheming high frequency, power distribution arrangements. Researchers (academic/industrial) and investigators are carrying out extensive study on design of HF inverters in different configurations/topologies. In bridge arrangement, the vital structures proposed are Full Bridge and Half Bridge Inverter in step down mode and step up mode; where performance concerning efficiency and total harmonic distortion was deliberated through experimental results.

DHB and DAB are two popular, prevalent and well accepted configurations among the PS dual bridge DC-DC converter. Tables 2.10-2.12 facilitate the comparison of the operational conditions, advantages and disadvantages of these two types of converter (i.e. DAB and DHB) which highlight that: (1) In DHB arrangement, the transformer flux swing is merely half of that of the DAB arrangement if the same transformer effective cross sectional area and switching frequency are used and (2) In comparison to DAB, a DHB uses half of the number of switching devices and obviously the equivalent drivers. Eventually such uniqueness contributes towards more cheap and inexpensive solution. In this development, a part of the phase shift DHB is preferred for analysis [82].

TABLE 2.10: Evaluation of DHB and DAB [82].

Parameter	**DHB**	**DAB**
Transformer Turn Ratio (n)	V_{in}/V_{out}	V_{in}/V_{out}
Duty Cycle (D)	0.5	0.5
Transformer flux swing (ΔB)	$(V_{in}/2)D/nA_f$	$V_{in}D/nA_ef$
Switching Devices	4	8

Where V_{in} = Input Voltage, V_{out} = Output Voltage, A_e = Effective cross sectional area of transformer, f = switching frequency

TABLE 2.11: Advantages and disadvantages of DAB [82].

Advantages	**Disadvantages**
Usage of soft switching for all power switches	More number of switches than DHB
Alike control algorithm in both energy flow directions	No soft switching ability at light loads
Modular structure possible	-
Minimal voltage and current stress	-

TABLE 2.12: Advantages and disadvantages of DHB [82].

Advantages	**Disadvantages**
Usages of twice less switches than DAB	Bulky DC capacitors
Use of soft switching for all switches	Twice higher current in switches than in DAB
Simple structure and control	No soft switches at light loads
Modulator structure possible	-

2.7.3 High Frequency Inverter

Literature survey emphasized the importance of Half Bridge configuration in terms of output voltage, number of bridges and number of switches etc. The Half Bridge arrangement merits for the reasons as: (1) Output voltage is half as compared Full Bridge voltage requirement (i.e. step down), (2) The number of bridges required is also half as compared to full bridge topology, (3) Sufficient simplification of a power scheme layout and (4) Reduction in complexity of control and protection circuit coupled with the reduced converter price.

A number of the researchers have worked on design of inverter in full bridge configuration; whereas a very few have based their studies on half bridge topology. Table 2.13 illustrates the performance parameters comparison of full bridge and half bridge inverter topology.

TABLE 2.13: Comparison of inverter topology [59, 60].

Parameters	**Full Bridge Topology (Without capacitors)**	**Half Bridge Topology**
Cost	1	0.86
Size	1	0.91
Control Complexity	1	0.85
Current Ripples	0.98	1
Switching Power Loss	1	-5
Power Transfer Efficiency	1	1
No. of Switches	4	2
No. of Driving Signals	2	2
Complexity Factor	1	0.85
Output Voltage	$+V_s$, $-V_s$ (Full)	$+V_s/2$, $-V_s/2$
Transformer Turn Ratio for same output	No need to step up	Step up by 2
Average Collector Current for same output	0.5	1
RMS Current through inverter switch for same output	0.707	1.414
Total Inverter Switch Stress	Same	Same

2.8 Medium/High-Frequency Transformers

In the beginning of 20^{th} century, a numeral of limitations being used as traditional power transformers was observed in low frequency transformers. These restrictions mainly include as a relatively large size and high-power losses [117]. However, in 21^{st} century, the HF transformers have gained the utmost popularity in solid state

devices due to their relatively small volume and low weight, as compared to the low frequency devices, in addition to the ability to work with high-frequency switch-mode power supplies. The main areas of application of high frequency transformers are automotive and telecom industries.

One of the first high frequency transformers came into existence, was reported as the conventional wire wound structure. Unlike low frequency devices, the multiple strands winding called litz wires have become the major entities of the high frequency wire wound transformer. These strands are incorporated for reduction of the influence of skin and proximity effects on operation of the transformer. Moreover, ferrite has been given due significance and commended as a magnetic core material for the reason that it devises a comparative low core loss at high frequencies [118]. This structure has several drawbacks such as inability to fully integrate it to the power stage and relatively high contact resistance.

Planar transformer was invented in the 1980s [119], and in recent years its popularity has dramatically increased due to the numerous advantages of this structure. In case of the planar transformer construction, the traditional wire windings are substituted by printed circuit boards (PCB). As the conductors are thin copper foil, consequently the operating or switching frequency of planar transformers is not restricted by skin effect. The compensations of this topology include the low profile, exceptional thermal features, and easy integration in addition to the power converter circuit [120]. A planar transformer is shown in Fig. 2.7. However, the planar transformer also has the number of drawbacks such as cost, low maintainability (if damaged, the entire power stage needs to be replaced) and low range in which the leakage inductance can be controlled.

For the past decades, a lot of work has been done in the area of high-frequency transformer design. In reference [121], the authors developed the wire wound high frequency transformer for DAB converter that operates with switching frequency of about 500kHz. During the study, they found that since the converter operates at such high frequencies, to achieve zero voltage switching the required leakage inductance should be approximately 3μH. Hence, there is no more need in the lumped inductance that is usually used to maintain ZVS.

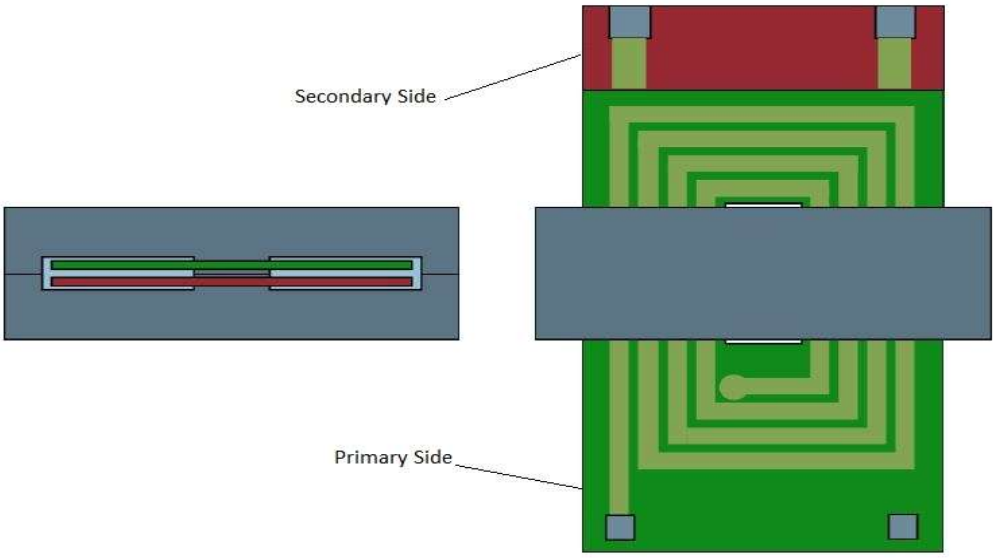


FIGURE 2.7: The model of the planar transformer [119].

In 2009, Zhang et al. [122] proposed the design of the planar transformer for aerospace application. The presented design results in a 36.3% reduction in size of the expedient as compared to the previously used transformer. Moreover, the core loss decreased from 2W to 1.59W and winding loss was reduced by 1.19W using interleaving layers method.

In [123], the authors presented a design optimization technique for high-frequency transformer, being part of DAB converter. The main goal of the study was to show that leakage inductance, phase-shift angle, skin and proximity effects are required to be calculated properly to minimize core loss. Furthermore, the study also established that the leakage inductance necessitated for ZVS can be implemented without using surplus inductor.

Fei et al. [124] proposed the novel design of the planar matrix transformer incorporated in LLC converter which includes the flux density reduction and design optimization. Matrix transformer represents the traditional magnetic core divided into the four core structures with primary winding connected in series and secondary winding connected in parallel. Distributing the secondary current with multiple cores helps to increase the output current capability of the transformer. The presented structure results in a decrease in flux density, equal to half that of the original model. Since the core loss is mainly determined by flux density, it was also decreased by 40%. Moreover, the proposed design methodology helps to

decrease the number of PCB layers from 12 to 4 and significantly reduce the cost of the transformer and its parasitic capacitance.

Lee et al. [125] presented a design optimization procedure for three phase dual active bridge converter to increase power density and efficiency. The design optimization involves the changing of transformer parameters such as the number of turns and the current density and then checking the transformer performance using FEA tool. Moreover, the authors created the objective function to estimate transformer efficiency, using magnetizing current, core loss, copper loss and total weight as function variables. The study shows that after all changes were made, two experimental prototypes demonstrated the efficiency of 98.95% and 99.01%, respectively.

Yan et al. [126] proposed a new transformer structure for 1.2kW LLC topology. New transformer has fully interleaved winding structure and novel integration technique where the rectifier and capacitors are directly integrated to the secondary winding to avoid increasing leakage inductance and ac resistance. The transformer model has been built and tested. The experiments show the total efficiency is equal to 96%.

Chattopadhyay et al. [127] provides the analysis of three limb high frequency transformer for DAB converter. The multi-limb transformers can be used to decrease inter winding capacitance in the transformer. In this paper, such aspects as design and simulation of the three-limb transformer has been discussed, also the equation for the leakage inductance and inter winding capacitance are provided.

The integrated transformer was proposed in [128]. It consists of UI or UU magnetic cores and two windings where the primary is made of a litz wire and the secondary one is made of a copper sheet. The proposed structure can help to control the leakage inductance (either make it very small or relative high by changing the position of the secondary side) of the transformer and can be easily integrated to the power stage. It also has better efficiency due to higher contact area and hence lower contact resistance. The integrated transformer is shown in Fig. 2.8. The drawbacks of this topology can be a higher cost as compared to the wire wound transformer and relatively small number of cores' sizes available at the market.

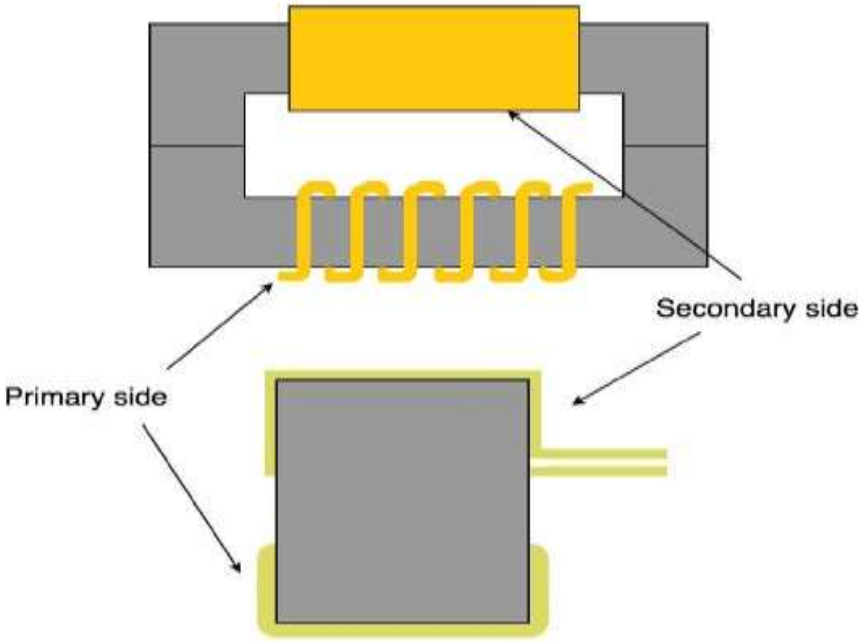


FIGURE 2.8: Integrated transformer [129].

A novel transformer for application of 12 and 24-pulse rectifier systems has been proposed with a size and volume decrease of 1/3 as compared to a conventional 50/60 Hz scheme. This reduced size has been realized by functioning the transformer core at operating frequency of approximately 990 Hz. It employed conventional grain oriented steel [129]. In [130], optimum volume and mass decrease of a 7kVA dry-type high frequency transformer has been anticipated, with the capability of withstanding high-voltage side insulation up-to 15 kV. This proposal necessitated moderately a high leakage inductance (nonexistence of leakage inductance may result for additional inductors, resulting in a greater volume, mass, and expenditure); hence meeting the leakage inductance requirement turned into essential issue. As the winding arrangement and the number of turns play a vital role in acquiring leakage inductance, therefore in adjusting and regulating the leakage flux, a two-winding configuration and numerous core materials were given due deliberation. In this phenomenon the windings on both sides are entirely disjointed, where one winding is completely enclosed up with the other winding. In this scenario, Metglas amorphous alloy cores driven out to as a paramount selection. The exact comparable design of a MV coaxial winding in the light of outcomes from a finite element method (FEM) and laboratory estimation has been proposed. This layout offers a consistent but evenly distributed electromagnetic flux with

virtuous electric and magnetic shielding. For 30KVA transfer, an overall efficiency of 99.5% has been achieved below 100∘C under the circumstances of oil-free and natural convection [131]. An optimization of a high frequency transformer with diverse objects (i.e. size, weight and expenditure) under certain limitations (such as given cooling performance, insulation needs, and designated semiconductors) has been anticipated in [132]. It was concluded that by virtue of a complete and comprehensive transformer design, it was conceivable to comprehend the optimum frequency with respect to volume, mass or efficiency for diverse schemes, coupled with analytically exploration of enhancements taking place from numerous core materials, wire edifices, geometries and cooling designs.

For achievement of maximum power density and efficiency, the optimization of a water-cooled high frequency transformer prototype has been anticipated [109]. In this design, an endeavor is made for the electric and thermal specifications and certain dimensions which deliberate clearance space as well as cooling system. The published material [112] demonstrated an optimization procedure for a 50kW, 5kHz high frequency transformer, which targeted to establish the maximum power density. Proficiency, isolation, thermal and leakage inductance necessities have been addressed taking into account thermal management. Reference material [133] anticipated a toroidal design model for a Metglas core incorporating a technique intended to optimize and augment the number of turns; whereas diminishing the (core plus winding) losses.

A comprehensive and detailed optimization technique for a 166 kW/20 kHz prototype has been deliberated, which was proved to be capable in attaining 99.4% efficiency at a power density of 44 kW/dm^3. In this design as a consequence to comparatively great-power rating, the cooling arrangement turned into a main contest and challenge. This scheme also delivered the critical and investigative elucidations for high-frequency losses, being segregated into skin and proximity losses [134]. The authors in [135] demonstrated an optimal design of 20/0.4kV high frequency transformer with objective of obtaining maximum efficiency, maximum power density and low weight. The utmost tolerable temperature rise was deliberated as an inequality restraint whereas the anticipated leakage and magnetizing inductance values were reflected as equality restraints. In this case an

efficiency and power density of above 99.70% were resulted.

2.9 Magnetic Core Materials

The selection of the magnetic materials for a device fabrication depends on numerous features such as cost, size, performance and the application. Nowadays, there are four materials that are typically used for magnetic cores production [136]:

2.9.1 Air

This factor attributes for the material that does not possess a core loss due to the deficiency of the physical core. The main drawback is that it is a poor conductor of the magnetic flux due to its low permeability.

2.9.2 Electric Steel

This feature is considered mostly for the low frequency transformers. It is produced by stacking together the number of the silicon steel lists. This process is called lamination. Using laminated cores can significantly reduce the eddy currents effect. The main reason for that is because in the laminated structure, the eddy currents are distributed in each particular thin metal sheet and therefore reducing their magnitude. Silicon steel possesses a great saturation flux density with appreciable permeability; thereby contributing its application for the low frequency transformers.

2.9.3 Powder Materials

The first nickel iron powder cores were produced in 1918 [136]. Powder cores are made of compressed powder materials such as moly perm alloy and powdered iron. One of the features and advantages of the powder materials contributes for their relatively low price. This factor enables powder material for broadly use in low frequency as well as high frequency applications.

2.9.4 Ferrite

The ferrite material was synthesized by Yogoro Kato and Takeshi Takei, researchers from Tokyo Institute of Technology in 1930 [137]. It eventually led to the foundation of the TDK – one of the largest manufacturers of the ferrite products in the world. Ferrites are the ceramic materials which are the combination of iron oxide and one of the metallic elements such as oxide, carbonate, manganese, zinc, nickel, magnesium or cobalt [128]. The two major categories of the soft ferrite are manganese-zinc (MnZn) and nickel-zinc (NiZn). Ferrite maintain excellent performance at high frequencies and have a high permeability (from 700 to 10000 [138, 139]). The main disadvantage of the ferrite core is low saturation flux density ($\sim$0.4T). Nevertheless, the value of flux density is usually significantly lower than saturation flux in the high frequency range applications.

Since the ferrite is the best suit for the high frequency application, it is used for all transformers especially in solid state transformer applications. Table 2.14 provides the characteristics of some magnetic materials [128].

TABLE 2.14: Characteristics of some magnetic materials [136].

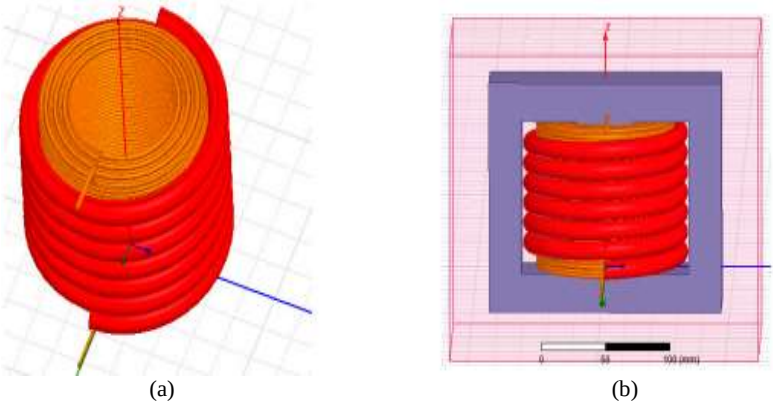
Material	**Composition**	**Flux density (T)**	**Permeability (μ)**
Magnesil	SiFe	1.5-1.8	1500
Supermendur	CoFeV	1.9-22	800
Silicon steel	SiFe	1.5-1.8	1500
Orthonol	NiFe	1.42-1.58	2000
Sq. Permalloy	NiFeMo	0.66-0.82	1200-100000
Iron powder	Fe	0.5-1.4	4-125
Amorphous 2605-SC	FeBFe	1.5-1.6	3000
Amorphous 2714-A	CoSiFe	0.5-0.58	20000
Ferrite (MnZn)	MnZn	0.3-0.5	700-15000
Ferrite (NiZn)	NiZn	0.3-0.5	15-1500

To counter the issues pertaining to skin and proximity effects are a solemn concern in designing MF transformers. Skin effects are resulted due to the inclination of high frequency currents flow on the outer surface of conductors. One of the

solutions to address the losses caused by the skin effect is the use of Litz wire, which is created by "interlacing" multiple smaller conductors organized to build an equivalent and comparable larger wire gauge.

As per the importance of the application of ferrite materials in modern and industrial power electronics application, the fabrication of ferrite core medium frequency transformer adopting ANSYS/ Maxwell platform is presented [140]. In contrast to sinusoidal signals of the same peak and frequency, ferrite core operation on square wave with 50% duty cycle results in 0%–15% lesser losses [141–143]. By virtue of these properties, the ferrite materials are considered most appropriate and favorable for various applications.

Specified design Maxwell model shown in Fig. 2.9 contains following parameter values for simulation: (1) Ferrite(P-Type) (9997 (nH/T^2), (2) Magnetic flux density (B) (3200 Gauss), (3) Core Area and Window Winding Area Product (1006.7857 cm^4), (4) Core Area (25 cm^2), (5) Window Winding Area (40.271429 cm^2), (6) Power (200KVA), (7) Frequency (25KHz), (8) Current Density (3.5 A/mm^2), (9) Primary/Input Voltage (20KV), (10) Input/ Primary Current (10.5 A), (11) Secondary/Output Voltage (500 V), (12) Output (Secondary) Current (400 A), (12) Number of Primary Turns (250 Turns), (13) Number of Secondary Turns (7), (14) Resistance of Primary Winding (0.299947 ω), (15) Inductance Primary Winding (26676.98 μH), (16) Resistance of Secondary Winding (0.34242 mω), (17) Inductance of Secondary Winding (400.904 μH), (18) Primary Winding Wire Area (4.399 mm^2) and (19) Secondary Winding Wire Area (122.23 mm^2).



(a) (b)

FIGURE 2.9: High frequency ferrite core transformer (a) Primary and secondary coil and (b) Complete transformer model (placed within an air medium) [140].

2.10 Standard Medium Frequency Transformer (MFT) Prototype

The research exertion in the area has significantly augmented in the past couple of years both in the industry and academia, resulting in numerous diverse MFT prototypes, as summarized in Fig. 2.10 and Table 2.15. Depending on the essential specifications, different ingredients, technologies and design choices in general are combined to best cope with the prevailing experiments. There are various potential substitutes for the technology coordination. Each design choice is coupled with several multi-physical characteristics, thus making the navigation through this design space rather complex.

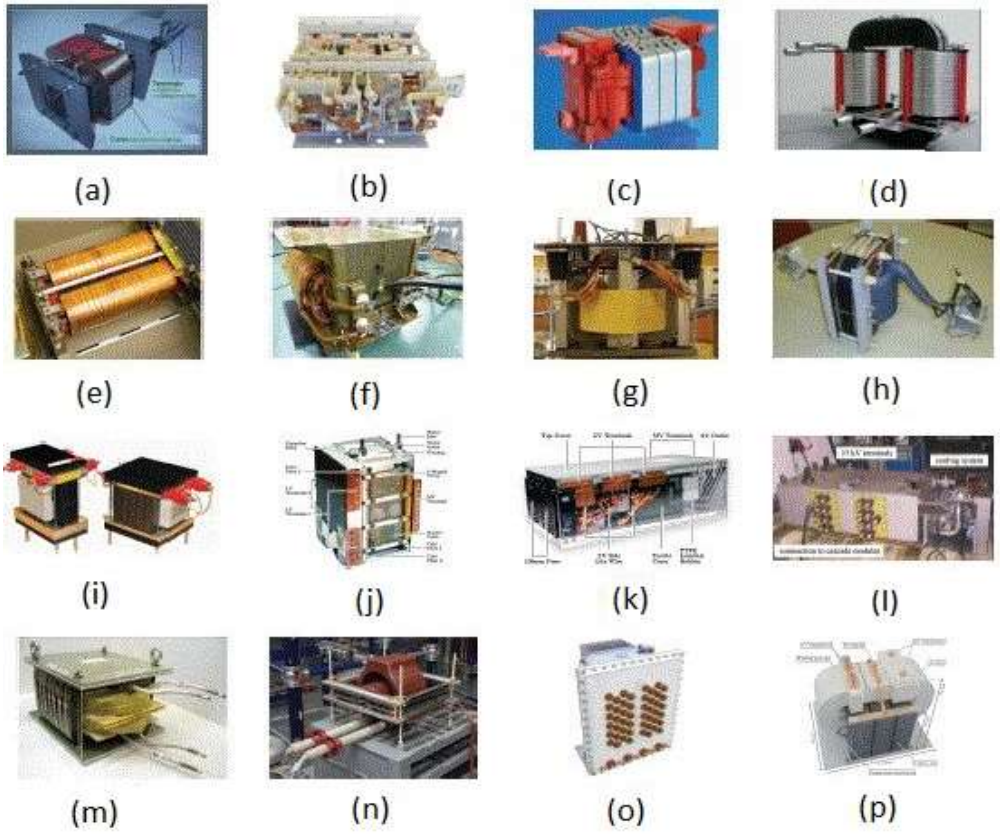


FIGURE 2.10: Standard MFT prototypes from the literature: (a) ABB: 350kW, 10kHz [144]; (b) ABB: 3 × 150kW, 1.8kHz [145, 146]; (c) STS: 450kW, 8kHz [147]; (d) FAU-EN: 450kW, 5.6kHz [140–142]; (e) IKERLAN: 400kW, 6kHz [143]; (f) IKERLAN: 400kW, 0.6kHz [143]; (g) KTH: 170kW, 4kHz; (h) BOMBARDIER: 350kW, 8kHz [148]; (i) CHALMERS: 50kW, 5kHz [149]; (j) ETHz: 166kW, 20kHz [150–152]; (k) ETHz: 166kW, 20kHz [150]; (l) ALSTOM: 1500kW, 5kHz [103, 153]; (m) EPFL: 300kW, 2kHz ; (n) ABB: 240kW, 10kHz [154]; (o) ABB CERN: 100kW, 15-22kHz [155]; (p) ETHz: 25kW, 48kHz [156].

Unlike LFTs operating with sinusoidal excitation at few standardized voltage levels, the specifications of the MFTs depend on the converter topology, voltage levels, and insulation requirements. The design specification depends on the specific application and custom operation; a time it is hard to make any type of standardization or fairly compare the given MFT prototypes. Moreover, with few exceptions, there is often very little or no information about any type of insulation testing. This need for customization has compelled the research in the direction of flexible design methodologies and advanced modeling that covers wider ranges of the associated phenomena resulting in several proposed MFT design optimization examples [149, 150, 156]. Similar to these, our perspective design should be to allow a simple identification of the best performing alternatives in respect to the specific desired MFT features (e.g. volume, mass, efficiency, etc).

In appraisal of the proposed inverter design with the rest of the existed configurations/ topologies of inverters deliberated during literature survey, following have been deduced from the simulation test / trials as well mathematical evaluation. Being a high frequency PWM inverter [3*(5kVDC/2.5KV wave AC)] in 100KVA solid state transformer applications, this design found to be producing virtually a square wave shaped voltage output with peak voltage of 2.5 kV in each phase which is a required input AC voltage to the ensuing stage (i.e. MFT).

In inverter optimization perspective, the various constraints/limitations which are given for due deliberations/achievement includes: (1) efficiency augmentation (2) reduction of cost/volume and (3) the delivery of stable output square wave AC. These restrictions were dealt / addressed in a befitting manner and ultimately came up with the impeccable design. These implement-ations proved to be valuable ones and led for acquiring the essential and indispensable results.

At 15kV DC input to the designed inverter (in a single phase perception), the calculated output power comes to the valuation of 27649.89827W using resistive load of 2000Ω. At this ouput the total loss (including snubber,conduction and switching loss) is estimated to be 490.1017 W as is evident from Table 5.4. Similarly, again at the 15KV input dc, the simulator input power comes to an estimation of 28140 W using resistive load of 2000 Ω with the input supply current of 1.867amperes.

TABLE 2.15: Specifications of several representatives MFT prototypes (given in Fig. 2.7).

Design Parameters	**(a)** [182]	**(l)** [180-181]	**(n)** [193]	**(c)** [183]	**(d)** [184-186]	**(h)** [188]	**(j)** [190-192]	**(p)** [195]
Construction Type	shell	multi win.	shell	shell	core	core	shell	Shell
p_r (kW)	350	1500	240	450	450	350	166	25
f (kHz)	10	5	10	8	5.6	8	20	48
V_1 (kV)	3	1.8	0.6	1.8	3.6	1	1	7
V_2 (kV)	3	1.65	0.9	1.8	3.6	1	0.4	0.4
Core Material	nano	ferrite	nano	nano	nano	nano	nano	ferrite
Conductor Type	coaxial	Litz wire	Litz wire	Litz wire	hollow tube	hollow tube	Litz wire	Litz wire
Conductor Material	(Al-in. Cu-out)	Cu	Cu	Cu	Al	/	Cu	Cu
Cooling	WF & A	OF	AF	OF & A	O	WF	WF	AF
Insulation	Solid	Oil	solid epoxy	solid & oil	oil	solid	solid tape	solid epoxy
Density (kV/l)	9.5	2.1	3.6	/	/	/	32.7	7.4
Density (kW/kg)	7	<1.5	5.7	9	11.8-18.8	7	16.6	4
PD Test (kV)	38	/	53	37	/	33	/	/
BIL Test (kV)	95	/	150	/	/	100	/	/

Where, W, A and O stand for water, air and oil cooling, respectively. F stands for forced cooling: nano is short from Nano- crystalline:

2.11 Gap Analysis

Most of the researchers (academic/industrial) have worked on design of inverter in full bridge configuration; whereas a very few have based their studies on half bridge topology. Very less information is available on half bridge topology in literature. In order to have a clear understanding of the problem statement it is more appropriate to have a gap analysis of the past work that has been carried out in the field of Solid State Transformer. In this connection it may be summarized as follows.

1. For identification of the most viable configuration of SST capable of supporting additional and supplementary functionalities in contrast to a regular transformer, a significant analysis of three main topologies for implementation of SST is undertaken:

    - A single stage SST topology is not considered suitable contestants in SST applications for the reason that it had no arrangement for input power factor correction [22].
    - Two stages SST with high DC (i.e. HVDC) link is not appropriate topology as this is devoid of isolation arrangement from the grid, hence it is not conforming to smart grid requirements. The DC-AC part of this topology is found to be a double phase inverter and is common for high order SST topologies as well [15, 22].
    - Three stage topology is considered to be the most feasible and appealing practical topology of the SST i.e. topology with high voltage (HV) as well as with low voltage (LV) dc links. These links are meant to enhance the ride through competence of SST; thereby allowing the improvement of power quality at input as well as output ends. This three stage topology offers all the preferred SST functionalities, simplifying the control design. This topology offers tremendous advantages over the rest of topologies including high flexibility, control performance and weighed as the most workable, practical and realistic solutions [116].

2. Isolated DC-DC converters are used to provide galvanic isolation, improve safety, enhance noise immunity and prevent the transmission of voltage transients to the output in the electrical fabrication. Transformer isolated DC-DC converter as an entity and the SST as a scheme; both these arrangements make use of a high frequency inverter at the input side of the HPMF transformer for the purpose of production of ac voltage. The transformer isolated converters (DAB or DHB) are used predominantly for provision of galvanic isolation, augment safety, boost noise immunity and prevent the transmission of voltage transients to the output. With ongoing technological advancement in power electronics, the research in this field is very active and updated; where a number of research papers and articles are published as evident from papers as referenced as [76–78].

3. Power conversion using high frequency inverters are gaining renewed attention in designing high frequency power distribution systems. Researchers and investigators are carrying out extensive study on design of high frequency inverters in different configurations. In bridge arrangement, the vital structures proposed include Full Bridge (FB) and Half Bridge (HB) Inverter in step down (buck) mode as well as step up (boost) mode [82]

4. DHB and DAB are two popular, prevalent and well accepted configurations among the dual bridge dc-dc converter. In case of DHB arrangement, the transformer flux swing and number of switching devices is merely half of that of the DAB arrangement if the same transformer effective cross sectional area and switching frequency are used. Eventually such uniqueness contributes towards more cheap and inexpensive solution. In this development, a part of the phase shift DHB is preferred for analysis [82]. In this development, a part of the phase shift DHB is preferred for analysis.

5. State of Art study emphasized the importance of Half Bridge configuration in terms of output voltage, number of bridges and number of switches etc. The Half Bridge arrangement merits for the reasons as: (1) Output voltage is half as compared Full Bridge voltage requirement (i.e. step down) (2) The number of bridges required is also half as compared to full bridge topology

(3) Sufficient simplification of a power scheme layout (4) Reduction in complexity of control and protection circuit coupled with the reduced converter price. Moreover in a design perspective, high frequency power inverter (being part of 2nd and 3rd SST topology) is the most significant and exciting block of SST, therefore it is preferred for research analysis with focus on enhanced efficiency, less cost and better voltage regulation incorporating PWM technique.

2.12 Problem Statement

The problem statement is given as:

"Design of an efficient high frequency Pulse Width Modulated Inverter as a part of 100KVA, 11KV/381V Solid State Transformer, in a half bridge topology scenario, in an appropriate simulation environment".

2.13 Research Objectives

The research objective that follows from the problem statement is:

"Design a 15 kV high frequency PWM inverter as a part of 11kV Solid State Transformer".

In order to materialize the problem, following requirements should be met:-

- To replace a 100kVA, 11kV/381V Conventional Traditional transformer with Solid State Transformer in a distribution system.
- To explore possible topology for SST, suitable for distribution system.
- To search for possible topology that could be used for high frequency inverter.
- To propose an efficient and requisite inverter with possible control strategy.
- To design high frequency DC-AC converter (Inverter) according to the specification.

- To model and simulate a proposed circuit of high frequency PWM inverter in an appropriate simulation environment as a fixed voltage.
- To assess the performance of high frequency power inverter based on its requisite performance parameters.

2.14 Summary

This chapter provided an appraisal of power electronics based SST circuits, isolated DC-DC converter circuits, DC-AC converter circuits on different configurations and high/medium frequency transformer surveyed in printed literature. It establishes the functional principles and parameters, efficiency improvement methods and harmonic eradication performances. This chapter is very much imperative in identifying and ascertaining the weaknesses and flaws coupled with strengths of each of the identified SST, isolated DC-DC converter, DC-AC converter and high/medium frequency transformer arrangements so far in practice. These facts are very useful in providing a comparative study of available SST and its significant constituents. In critical appraisal, it has been revealed that three stages SST, transformer isolated DC-DC converter, half bridge topology based PWM inverter and ferrite core transformer have specific advantages over the rest of the existed conventional configurations. Therefore, the analysis dictated to emphasize on three stage SST topologies, transformer isolated DC-DC converter, DC-AC converter and ferrite core transformer arrangements/topologies. Over the last couple of years, diverse inverter design techniques (i.e. switched-capacitor based) have been evolved. Some of these techniques are required to be completely examined and investigated in order to establish the most practical technique, incorporated in this dissertation.

Chapter 3

Analytical Modeling

This chapter deliberates on mathematical model of Solid State Transformer. Firstly it derives voltage equations for its three constituents in a dynamic model three-phase stationary reference frame. Consequently, mathematical parameters calculation of three stages SST in five block/parts division is undertaken, emphasizing on implementation of full bridge and half bridge topology in power inverters design; thereby proposing three choices. Further, it highlights the modeling of inverter with transformer system, differentiation between a full bridge inverter & half bridge inverter and comparison of fixed load inverter with a variable load inverter. It also deliberates on design of medium frequency power transformer elaborately. This chapter ends with the narration of significant performance parameters of inverter. The calculations, capacities and outcomes are subsequently executed in successive chapters.

3.1 Mathematical Model of SST

Consider a Solid State Transformer with three stage, i.e. consisting of AC-DC Converter stage,isolation stage and then low frequency DC-AC converter stage for evaluation as mathematical modelling and further analysis. For proper anticipation, mathematical model is established for steady state stability investigation for SST, neglecting transients of MF transformer. Here firstly, three-phase PWM

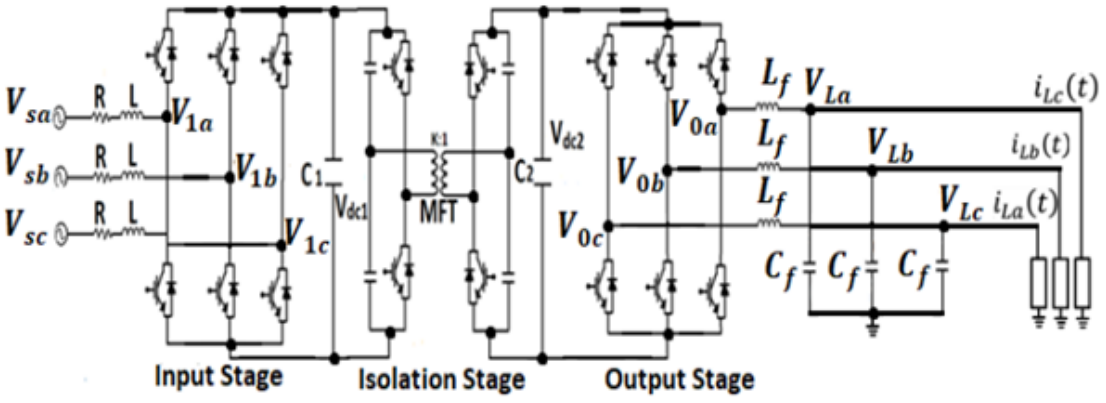


FIGURE 3.1: Configuration of SST for mathematical model [111].

rectifier converts grid voltages (three-phase) into corresponding DC voltage. The obtained DC voltage is then transformed into high frequency square wave with help of inverter in single phase perspective. This transformed MF square wave voltage is fed to the primary of MFT and at the output of its secondary ; this voltage is received in step down arrangement. Further this voltage is again rectified with help of rectifier and obtained DC voltage is directed to the low frequency output inverter. The obtained DC voltage is routed to the low frequency output inverter. Figure 3.1 is the detailed structure of SST for evaluation of mathematical model. Use of a DC-link provides advantages such as controllable voltage and current on both sides of the SST via pulse width modulation (PWM) technology.

Use of a DC-link provides advantages such as controllable voltage and current on both sides of the SST via pulse width modulation (PWM) technology. The voltage equations regarding rectifier stage, isolation stage and output low frequency stage of SST arrangement are appended as under [157]:

$$\begin{bmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{bmatrix} = \sqrt{2}V_s \begin{bmatrix} \sin\omega t \\ \sin(\omega t - 120) \\ \sin(\omega t + 120) \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} V_{1a}(t) \\ V_{1b}(t) \\ V_{1c}(t) \end{bmatrix} = m_1 V_{DC} \begin{bmatrix} \sin(\omega t - \theta_1) \\ \sin(\omega t - 120 - \theta_1) \\ \sin(\omega t + 120 - \theta_1) \end{bmatrix} \tag{3.2}$$

$$\begin{bmatrix} V_{0a}(t) \\ V_{0b}(t) \\ V_{0c}(t) \end{bmatrix} = m_2 V_{DC} \begin{bmatrix} \sin(\omega t - \theta_2) \\ \sin(\omega t - 120 - \theta_2) \\ \sin(\omega t + 120 - \theta_3) \end{bmatrix} \tag{3.3}$$

While transforming these relationships into differential equations of SST structure as matrix forms:

$$L\frac{d}{dt}\begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{1c}(t) \end{bmatrix} = \begin{bmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{bmatrix} - \begin{bmatrix} V_{1a}(t) \\ V_{1b}(t) \\ V_{1c}(t) \end{bmatrix} - R\begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{1c}(t) \end{bmatrix} \tag{3.4}$$

$$L_f\frac{d}{dt}\begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} = \frac{1}{k}\begin{bmatrix} V_{0a}(t) \\ V_{0b}(t) \\ V_{0c}(t) \end{bmatrix} - \begin{bmatrix} V_{La}(t) \\ V_{Lb}(t) \\ V_{Lc}(t) \end{bmatrix} \tag{3.5}$$

$$C_f\frac{d}{dt}\begin{bmatrix} V_{La}(t) \\ V_{Lb}(t) \\ V_{Lc}(t) \end{bmatrix} = \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} - \begin{bmatrix} i_{La}(t) \\ i_{Lb}(t) \\ i_{Lc}(t) \end{bmatrix} \tag{3.6}$$

$$\frac{d}{dt}\left(\frac{1}{2}CV_{DC}^2(t)\right) = [V_{1a}(t)V_{1b}(t)V_{1c}(t)]\begin{bmatrix} i_{1a}(t) \\ i_{1b}(t) \\ i_{1c}(t) \end{bmatrix} - \frac{1}{k}[V_{0a}(t)V_{0b}(t)V_{0c}(t)]\begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} \tag{3.7}$$

In the above relationships, k is transformation ratio of MFT and $C = C_1 + C_2/k)2$. L and R denote the inductor and resistor of the input stage. C_1 and C_2 represents dc capacitors of the input and output stages. L_f and C_f are used for filter inductor and capacitor of the output stage. V_{DC} shows DC-link voltage of the input stage. m_1 and m_2 exhibit the amplitude modulation indexes pertaining PWM AC-DC converter as well as three-phase PWM inverter, respectively. θ_1 & θ_2 resemble the modulation angles of PWM AC-DC converter and DC-AC converter, correspondingly. The input/grid ac voltages are depicted as V_{sa}, V_{sb} and V_{sc}. Output voltages are given as V_{La}, V_{Lb} and V_{Lc}. The input stage DC voltage is symbolized

as V_{DC}. V_{0a}, V_{0b} and V_{0c} are the output stage voltages. V_{1a}, V_{1b} and V_{1c} are AC voltages in the input stage Eqs. (3.1) to (3.4) exhibit the dynamic model of SST in three-phase stationary reference frame. To ascertain time-varying or time invariant equations, it is mandatory that the dynamic differential equations parameters should be altered into corresponding rotating reference frame, using Park transformer. In fact, there are two types of transformations as Park's transformation and CLARKE transformation. In Park's transformation, the three rotating phases abc are transferred to three equivalent stationary dq_0 phases (d-q reference frame). This transformation can preserve the active power (d-axis) and reactive power (q-axis) with the powers of the system in the abc reference frame by implementing an invariant version of the Park transform. CLARKE transformation converts the time-domain components of a three-phase system in an abc reference frame to components in a stationary $\alpha\beta_0$ reference frame. For a balanced system, a zero component is equal to zero. The equations and calculations in d-q rotating reference frame can be presented subsequently [158, 159].

$$\frac{d}{dt}\begin{bmatrix} i_{1d}(t) \\ i_{1q}(t) \end{bmatrix} = -\begin{bmatrix} i_{1d}(t) \\ i_{1q}(t) \end{bmatrix} - \omega \begin{bmatrix} i_{1q}(t) \\ -i_{1d}(t) \end{bmatrix} + \frac{m_1}{L} V_{DC} \begin{bmatrix} \sin\theta_1 \\ \cos\theta_1 \end{bmatrix} + \frac{\sqrt{2}}{L} \begin{bmatrix} 0 \\ V_s \end{bmatrix} \tag{3.8}$$

$$\frac{d}{dt}\begin{bmatrix} V_{DC} \end{bmatrix} = \frac{3m_1}{2C} \begin{bmatrix} i_{1d}\sin\theta_1 \\ -i_{1q}\cos\theta_1 \end{bmatrix} + \frac{3m_2}{2kC} \begin{bmatrix} i_{fd}\sin\theta_2 \\ -i_{fq}\cos\theta_2 \end{bmatrix} \tag{3.9}$$

$$\frac{d}{dt}\begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} = \frac{1}{C_f}\begin{bmatrix} i_{fd}(t) \\ i_{fq}(t) \end{bmatrix} - \frac{1}{C_f}\begin{bmatrix} i_{Ld}(t) \\ i_{Lq}(t) \end{bmatrix} - \omega \begin{bmatrix} V_{Lq}(t) \\ -V_{Ld}(t) \end{bmatrix} \tag{3.10}$$

$$\frac{d}{dt}\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = \omega \begin{bmatrix} -i_{fq}(t) \\ i_{fd}(t) \end{bmatrix} + \frac{m_2 \sin\theta_2}{kL_f} \begin{bmatrix} -V_{DC} \\ V_{DC} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} V_{Ld}(t) \\ V_{Lq}(t) \end{bmatrix} \tag{3.11}$$

Where

$$[i_{1d} i_{1q} i_{1o}]^T = K\,[i_{1\mathrm{a}} i_{1b} i_{1c}]^T, [i_{fd} i_{fq} i_{fo}]^T = [i_{f\mathrm{a}} i_{fb} i_{fc}]^T$$

$$[i_{Ld} i_{Lq} i_{Lo}]^T = K\,[i_{L\mathrm{a}} i_{Lb} i_{Lc}]^T\,[V_{Ld} V_{Lq} V_{Lo}]^T = [V_{L\mathrm{a}} V_{Lb} V_{Lc}]^T$$

In the above equations, q and d denote rotating reference frame. $[i_{1d},\ i_{1q}]$ and $[i_{Ld}, i_{Lq}]$ exhibit input currents and load currents respectively. $[i_{fd}, i_{fq}]$ and $[V_{Ld}, V_{Lq}]$

resembles filter inductance currents and output voltages correspondingly. The Park's transformation equation [160] may be symbolized as K and can be articulated by Eq. (3.12):

$$K = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin(\omega t) & \sin(\omega t - 120) & \sin(\omega t + 120) \\ \frac{3}{2} & \frac{3}{2} & \frac{3}{2} \end{bmatrix} \tag{3.12}$$

Configuration of Solid State Transformer structure consisting of input, isolation and output stages has been deliberated, where the input stage of SST structure has significance in the demolition of the disturbances. Therefore, the control of this stage is not only very important for the performance of SST structure but also for the power quality. The d-q reference frame is depicted in Fig. 3.2.

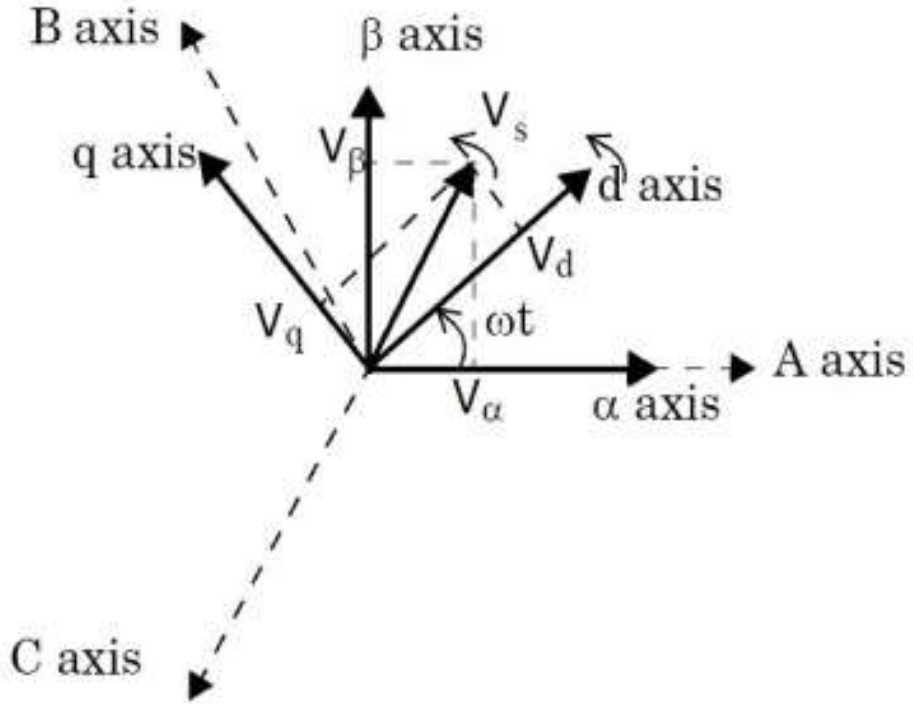


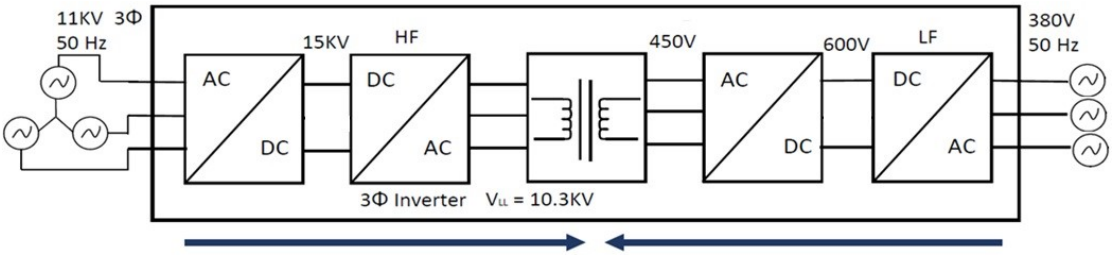
FIGURE 3.2: Three-phase signal to d_{q0} rotating reference transformation [157].

3.2 Stage Wise Parameter Calculation of SST

The first and former stride to replace 11KV/381V, 100KVA Conventional Line Frequency (distribution) transformer to a three stage SST is the stage-wise parameter analysis of three stages (five blocks) SST, which is appended subsequently:

3.2.1 Proposed Method-1

In this perspective, assumption is made on incorporating high frequency PWM inverter in full bridge arrangement at the primary of medium frequency transformer and low frequency inverter in full bridge topology at the secondary of medium frequency transformer. The detail analysis is shown in Fig. 3.3.



Rectifier

$V_{in} = V_{LL} = 11kV3\phi$

$V_{dc} = \frac{2}{\frac{2\pi}{6}}\int_0^{\frac{\pi}{6}} \cos wt\, d(wt)$

$V_{dc} = \frac{3}{\pi}V_{LL(Peak)}\frac{3}{\pi}\ [V_{RMS} \times \sqrt{2}]$

$V_{dc} = \frac{3}{\pi}[(11 \times 10^3)(\sqrt{2})]$

$V_{dc} = 14855.21922V$

$V_{dc} \approx 15kV$

PWM Inverter

$V_s = V_{dc} = 15kV$

$V_{LL(Peak)} = 14.5\ kV$

$\leftarrow (500\ V < V_{dc})$

$V_{LL(rms)} = \frac{14.5\ kV}{\sqrt{2}}$

$V_{LL(rms)} = 10253.04833\ V$

$V_{LL(rms)} \approx 10.3\ kV$

$I_{L(\text{rms})} = \frac{VA}{V_{rms}\sqrt{2}}$

$I_{L(rms)} = \frac{100kVA}{(10.3kV)\sqrt{3}}$

$I_{L(rms)} = 5.60\ Amperes$

$I_{L(rms)} = 6\ Amperes$

MFT

$V_{LL(P)(input)} = 14.5\ kV$

$I_{L\left(\frac{I}{P}\right)} = 6A$

$V_{LL\frac{i}{p}(rms)} = 10.253\ kV$

$V_{LL\frac{o}{p}(rms)} = 450\ V$

$(N{:}1)$

$(23{:}1)$

$(\boldsymbol{Step\ Down})$

Rectifier

$V_{dc} = 600V$

$V_{LL(Peak)} = \frac{\pi}{3}V_{dc}$

$V_{LL(Peak)} = \frac{\pi}{3}(600)$

$V_{LL(Peak)} = 628.318V$

$V_{LL(Peak)} \approx 630V$

$V_{LL(rms)} = \frac{630}{\sqrt{2}}Volts$

$V_{LL(rms)} = 445.477\ V$

$I_{LL(rms)} = \frac{VA}{\sqrt{3}}$

$= \frac{100{,}000}{\sqrt{3}V_{LL} \times 450}$

$= 128.30A$

LF Inverter

$V_{LL(rms)} = 380\ V$

$V_{LL(Peak)} = \sqrt{2}(380)V$

$V_{LL(Peak)} = 537.401\ V$

$V_{LL(Peak)} \approx 600\ V$

FIGURE 3.3: Analysis for proposed method-1.

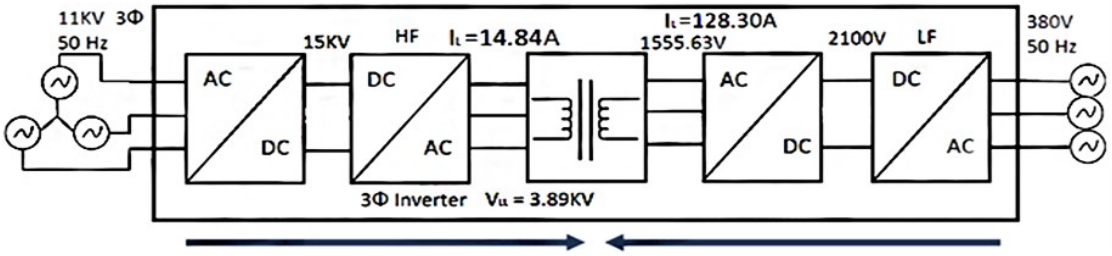
Mathematical analysis of Fig. 3.3 reveals that using full bridge topology at PWM inverter and also full bridge at low frequency inverter, the output voltage of PWM inverter comes to 10.253 kV with 6x bridges configuration utilizing 24 transistors as switching devices. In further elaboration, during the forward direction (as indicated by arrow head), the input voltage to the SST is 11KV. Since SST has been divided into five blocks, firstly this 11KV voltage is rectified by rectifier stage and at the output of rectifier (through mathematical formulae), 15KV DC voltages

is achieved at the input of PWM inverter. PWM inverter is taken into full bridge configuration containing 4x transistors per bridge. The line voltage at the output comes to 10.3KV. In the reverse direction from the end block (as indicated by arrow head) (i.e. LF inverter), the output voltage of 380V is produced, which contributes to line to line peak voltage (DC voltage) of 600V.This 600V DC is fed to rectifier (4^{th} block) of isolated DC-DC converter. AC voltage (line to line) of this rectifier comes out to calculated value as 450V. Now in analysis, in the middle block (i.e. MF transformer), the input voltage is 10.3KV and output voltage is 450V. Using voltage and turn ratio relationship ($N_P V_P = N_S V_S$), the turn ratio becomes 23:1 (step down).

3.2.2 Proposed Method-2

In this perception, assumption is made on incorporating high frequency PWM inverter in half bridge topology at the primary of medium frequency transformer and low frequency inverter in half bridge configuration at the secondary of medium frequency transformer. The detail analysis is shown in Fig. 3.4.

Figure 3.4 depicts the use of half bridge topology at PWM inverter as well as at low frequency inverter. To our concern, the output voltage of half bridge PWM inverter comes to 3.89KV with 3x bridges configuration utilizing six transistors as switching devices. The input 15KV to the PWM inverter will be distributed in three bridges, where every bridge will contain 2x high power capacitors as per practice. In further elaboration, in the forward direction (as indicated by arrow head), the input voltage to the SST is depicted as 11KV. SST has been divided into five blocks. Firstly this 11KV voltage is rectified by rectifier block and at the output of rectifier the 15KV DC voltages is achieved at the input of PWM inverter in half bridge configuration. The phase voltage at the output comes to an amount of 2250V and correspondingly, the line voltage becomes 3.89KV. In the reverse direction from the end block i.e. LF inverter (as indicated by arrow head), the output voltage produced is 380V, which contributes to line to line peak voltage (DC voltage) of 3.89V.This 600V DC is fed to the rectifier (4^{th} block) of DC-DC converter, thereby an amount of 1550V ac voltage (line to line) produced by this



Rectifier	**PWM Inverter**	**MFT**	**Rectifier**	**LF Inverter**
$V_{in} = V_{LL} = 11kV3\phi$	$V_s = V_{dc}$ $= 15kV$	$V_{LL(P)(input)} = 2.25\ kV$	$V_{dc} = 2100V$	$V_{LL(rms)}$ $= 220\ V$
$V_{dc} = \frac{2}{\frac{2\pi}{6}}\int_0^{\frac{\pi}{6}} \cos wt\ d(wt)$	$V_{phase(rms)}$ $= \frac{15}{6}kV$ $\leftarrow (250V$ $< V_{dc})$	$I_{L\left(\frac{I}{P}\right)} = 14.84\ A$	$V_{LL(Peak)} = \frac{\pi}{3}V_{dc}$	$V_{LL(Peak)}$ $= \sqrt{2}(220)V$
$V_{dc} = \frac{3}{\pi}V_{LL(Peak)}\frac{3}{\pi}\ [V_{RMS}$ $\times\sqrt{2}]$	$V_{LL(rms)}$ $= \sqrt{3}$ $\times 2250\ V$	$V_{LL\frac{i}{p}(rms)} = 3.89\ kV$	$V_{LL(Peak)}$ $= \frac{\pi}{3}(2100)$	$V_{LL(Peak)}$ $= 311\ V_{dc}$
$V_{dc} = \frac{3}{\pi}[(11\times10^3)(\sqrt{2})]$	$V_{LL(rms)}$ $= 3.89kV$	$V_{LL\frac{o}{p}(rms)} = 1555.63\ V$	$V_{LL(Peak)}$ $= 2199.11\ V$	$V_{LL(Peak)}$ $\approx 350\ V$
$V_{dc} = 14855.21922V$	$I_{L(\text{rms})}$ $= \frac{VA}{V_{rms}\sqrt{3}}$	$(N{:}\,1)$	$V_{LL(Peak)}$ $\approx 2200\ V$	$(39\ Volts$ $> V_{LL(peak)})$
$V_{dc} \approx 15kV$	$I_{L(rms)}$ $= \frac{100kVA}{(3.89kV)\sqrt{3}}$	(2.5: 1) Step Down	$V_{LL(rms)}$ $= \frac{2200}{\sqrt{2}}Volts$ $= 1555.63V$	
	=14.84A		$I_{L(rms)} = \frac{VA}{\sqrt{3}\times V}$ $= 37.11A$	

FIGURE 3.4: Analysis for proposed method-2.

rectifier is resulted. Now in the middle block i.e. medium frequency transformer, the input comes to an amount as 3.89KV, whereas the output is 1550V. Using voltage and turn ratio relationship ($N_P V_P = N_S V_S$), the turn ratio becomes 2.5:1 (step down).

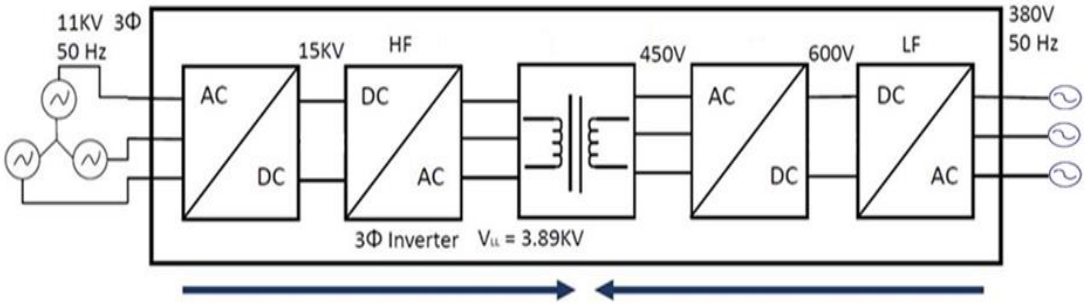
3.2.3 Proposed Method-3

In this proposal, supposition is made on incorporating high frequency PWM inverter in half bridge topology at the primary of medium frequency transformer and low frequency inverter in full bridge configuration at the secondary of medium frequency transformer. The detail block-wise analysis is shown in Fig. 3.5.

Analysis of Fig. 3.5 reveals the arrangement of using half bridge topology PWM inverter at input and full bridge topology LF inverter at output of MF transformer. To our anxiety, the output voltage of half bridge inverter comes to 3.89kV utilizing 6 transistors as switching devices. Initially, the input 15kV to the high frequency inverter will be distributed in three bridges, where every bridge will contain 2x high power capacitors. Each capacitor will hold 2.5kV; one capacitor will be used for positive half cycle, whereas 2^{nd} one for negative half cycle. Further in elaboration, in the forward direction (as indicated by arrow head), the input voltage to the SST is 11KV. SST has been divided into five blocks.

Firstly this 11KV voltage is rectified by rectifier block and resulted into an output of 15KV DC voltages (through mathematical formulae). PWM inverter is in half bridge configuration is the subsequent block. The phase voltage at the output of this block comes to 2250V and correspondingly the line voltage becomes 3.89KV. In the reverse direction from the end block (as indicated by arrow head) (i.e. LF inverter), the output produced is 380V.This voltage contributes to line to line peak voltage (DC voltage) of 600V.This 600V DC is fed to rectifier (4^{th} block) of isolated DC-DC converter. AC voltage (line to line) of this rectifier is calculated to be 450V. Now in the middle block (i.e. medium frequency transformer) the input is 3.89KV and the output is 450V.Using voltage and turn ratio relationship ($N_P V_P = N_S V_S$), the turn ratio has become 8.6:1 (step down). Now in the middle block (i.e. medium frequency transformer) the input is 3.89KV and the output is 450V.Using voltage and turn ratio relationship ($N_P V_P = N_S V_S$), Now in the middle block (i.e. medium frequency transformer) the input is 3.89KV and the output is 450V. The turn ratio has become 8.6:1 (step down). Table 3.1 illustrates the comparison of the three proposals.

Equations 3.1 to 3.12 are firstly taken from the state of art for voltage relationship for three stage SST model and then derived/adapted as per the constituents/entity parameters and stage arrangement being anticipated in our proposed scenario. Firstly taken from the state of art for voltage relationship for three stage SST model and then derived/adapted as per the constituents/entity parameters and stage arrangement being anticipated in our proposed scenario. However the analysis of the various parameters in sections 3.2.1, section 3.2.2 and section 3.2.3 have



Rectifier	**PWM Inverter**	**MFT**	**Rectifier**	**LF Inverter**
$V_{in} = V_{LL} = 11kV3\phi$	$V_s = V_{dc} = 15kV$	$V_{LL(P)(input)} = 14.5\ kV$	$V_{dc} = 600V$	$V_{LL(rms)} = 380\ V$
$V_{dc} = \frac{2}{\frac{2\pi}{6}}\int_0^{\frac{\pi}{6}} \cos wt\ d(wt)$	$V_{phase(rms)} = \frac{15}{6}kV$ $\leftarrow (250V < V_{dc})$	$I_{L(\frac{I}{P})} = 6A$	$V_{LL(Peak)} = \frac{\pi}{3}V_{dc}$	$V_{LL(Peak)} = \sqrt{2}(380)V$
$V_{dc} = \frac{3}{\pi}V_{LL(Peak)}\frac{3}{\pi}\ [V_{RMS} \times \sqrt{2}]$	$V_{LL(rms)} = \sqrt{3} \times 2250\ V$	$V_{LL\frac{i}{p}(rms)} = 3.89kV$	$V_{LL(Peak)} = \frac{\pi}{3}(2100)$	$V_{LL(Peak)} = 537.401\ V$
$V_{dc} = \frac{3}{\pi}[(11 \times 10^3)(\sqrt{2})]$	$V_{LL(rms)} = 3.89kV$	$V_{LL\frac{o}{p}(rms)} = 450V$	$V_{LL(Peak)} = 2199.11\ V$	$V_{LL(Peak)} \approx 600\ V$
$V_{dc} = 14855.21922V$	$I_{L(\text{rms})} = \frac{VA}{V_{rms}\sqrt{3}}$	$(N{:}1)$	$V_{LL(Peak)} \approx 2200\ V$	
$V_{dc} \approx 15kV$	$I_{L(rms)} = \frac{100kVA}{(3.89kV)\sqrt{3}}$ =14.84A	(8.6:1) **(Step Down)**	$V_{LL(rms)} = \frac{2200}{\sqrt{2}}Volts$	

FIGURE 3.5: Analysis for proposed method-3.

been derived, analyzed and calculated entirely by the scholar.

3.3 Modeling of Inverter and Transformer System

Primarily an inverter is used to convert DC to AC for provisioning of low voltage output. Figure 3.6 illustrates the converter with HF/MF transformer, in which DC voltage is transformed to square wave voltage with high frequency and then it is coupled to the input (primary side) of transformer.

From construction point of view, in assaying the size of the transformer, its volume or size is inversely proportional to the frequency [i.e. Volume $\propto (A_{core}A_{wdg})^{3/2} \propto$

TABLE 3.1: Comparison of PWM inverter parameters for three proposed methods.

Parameter	**Method-1 (Figure 3.3)**	**Method-2 (Figure 3.4)**	**Method-3 (Figure 3.5)**	**Remarks**
Input Voltage	15KV	15KV	15KV	Equal in all Methods
Output Voltage	10.3KV	3.89KV	3.89KV	Less for Methods-2,3
Output Current	6A	14.84A	14.84A	Less for Methods-2,3
No of Bridges	6	3	3	Less for Methods-2,3
No of switches	24	6	6	Less for Methods-2,3

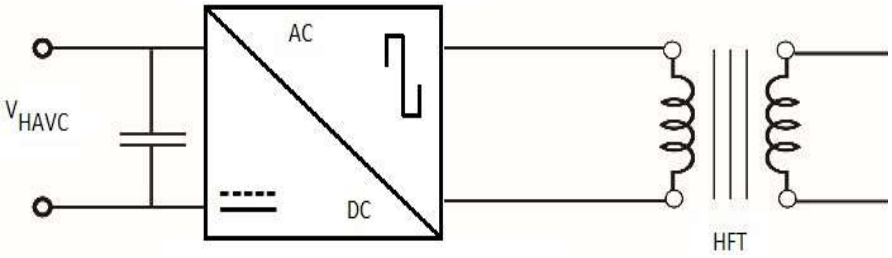


FIGURE 3.6: Inverter with HF/MF transformer [161].

$\frac{1}{f^{3/4}}$,] [161], the high frequency transformer is much smaller than the existed power frequency transformer; hence the transformer volume and stress factors are reduced significantly. Figure 3.7 illustrates the basic design of half bridge topology inverter, which can be noticed as a pattern of two back to back forward inverters, supplied identically by the same input voltage, each driving power to the load at each alternate cycle half cycle. The capacitors C_1 and C_2 are placed across the input terminals, such that the voltage across the primary winding always is half of the input voltage, $V_s/2$.

Before realizing the power conversion coupled with galvanic isolation aspects, the middle stage of SST, in particular its high frequency DC-AC converter has significant and influential effect on the working efficiency and power density of the complete system; therefore, its design is taken as one of the core contests for solid

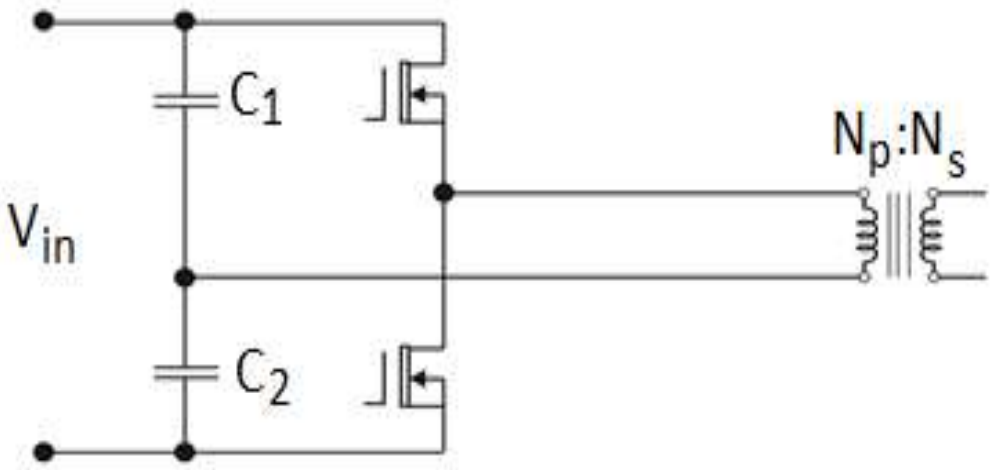


FIGURE 3.7: HB inverter configuration [161].

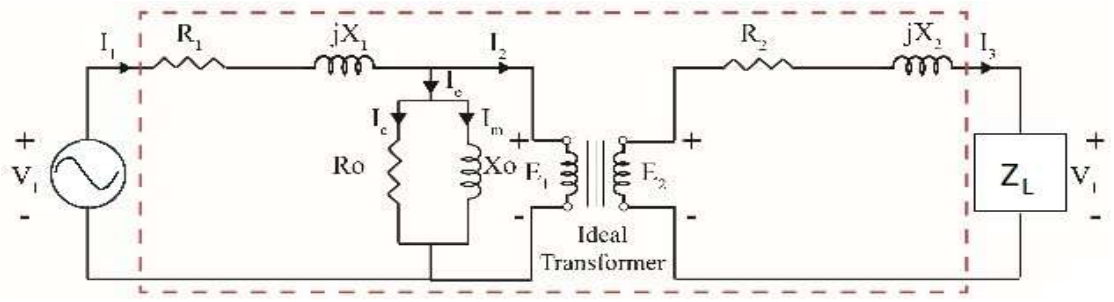


FIGURE 3.8: Schematic diagram of transformer [162].

state transformer operation. Before designing /developing the model for DC-AC Converter, it is anticipated that the power system is balanced, symmetrical and operates under three phase balanced condition, while neglecting converter losses. Parameters involved in the mathematical model include: V_{HVDC} = Voltage across Capacitor, I_2= Output current of MF Transformer Secondary, V_1= Output voltage of HF Inverter, V_2= Output voltage of MF Transformer Secondary, I_1= Output current of HF Inverter/ Input to Transformer Primary. The transformer feature depicted diagrammatically in Fig. 3.8, determined into an equivalent circuit, where the transformer resistance coupled with leakage reactance are anticipated to be external to the winding, set for only function of transforming the voltage. I_0(no load current) is simulated by pure inductance X_0,attaining the magnetizing component I_μ and non-inductive reactance R_0 taking the working component I_w ,being connected in parallel through the primary circuit, as shown in Fig. 3.9. Various expressions can be calculated as, $E_1 = V_1\text{-}I_1Z_1$, $R_0 = E_1/ I_w$, $X_0 = E_1/ I_0$ and $E_2/E_1 = N_2/N_1 = K$.

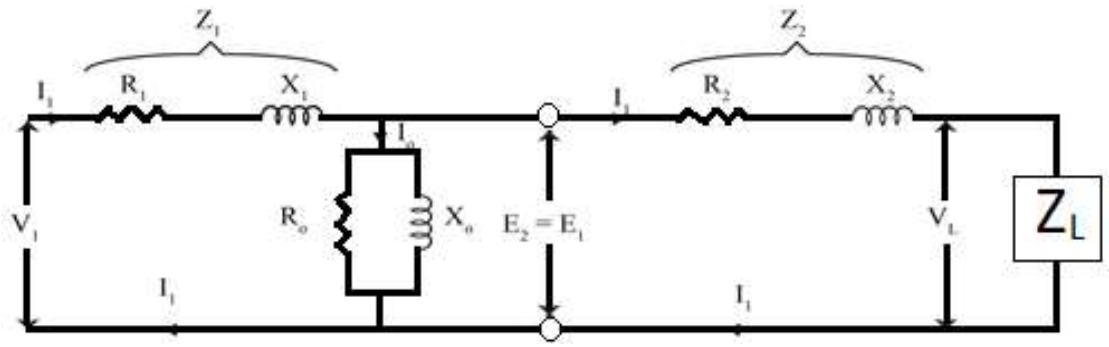


FIGURE 3.9: Total (exact) equivalent circuit of transformer [162].

To compose the transformer calculations and design simpler, it is preferred that the voltage, current and impedance components may be transformed either to the secondary or to the primary. Under this perspective, the calculation is undertaken in one winding, (i.e. primary winding which is quite convenient and easy to construct).Primary equivalent of secondary induced voltage is given as, $\acute{E}_2 = E_2/K = E_1$, whereas the primary equivalent of secondary terminal output voltage is given as, $\acute{E}_2 = V_2/K$. However, the primary equivalent of secondary current may be established as, $\acute{I}_2 = I_2/K$. For transferring secondary impedance to primary, then K^2 is used, (i.e. $\acute{R}_2 = R_2/K^2$, $\dot{X}_2 = X_2/K^2$, $\acute{Z}_2 = Z_2/K^2$). For shifting external load impedance to primary, same relationship is used. Total equivalent circuit of transformer achieved is depicted in Fig. 3.10.

Total impedance between two terminals, $Z = (Z_1 + Z_m) \,||\, (\acute{Z}_2 + \acute{Z}_L)$, where, $\acute{Z}_2 = \acute{R}_2 + j\dot{X}_2$ and Z_m is impedance of exciting circuit, $V_1 = I_1 Z$. The exact equivalent circuit is considered to be a somewhat cumbersome for circuit problem solution. Simplification can be attained by shifting the exciting circuit across the terminals beyond R_1, then in this case, $X_0 = V_1/I_\mu$, as depicted in Fig. 3.10.

More simplification can be obtained by excluding I_0 altogether as shown in Fig. 3.11; where it depicts approximate equivalent circuit of transformer referred to primary. For mathematical modeling of inverter, the R_{01} altogether is omitted in the circuit of Fig. 3.12 and the most simplified electrical equivalent circuit is shown in Fig. 3.13.

After simplification and analysis, Fig. 3.14 depicts the simplified circuit of DC-DC converter.

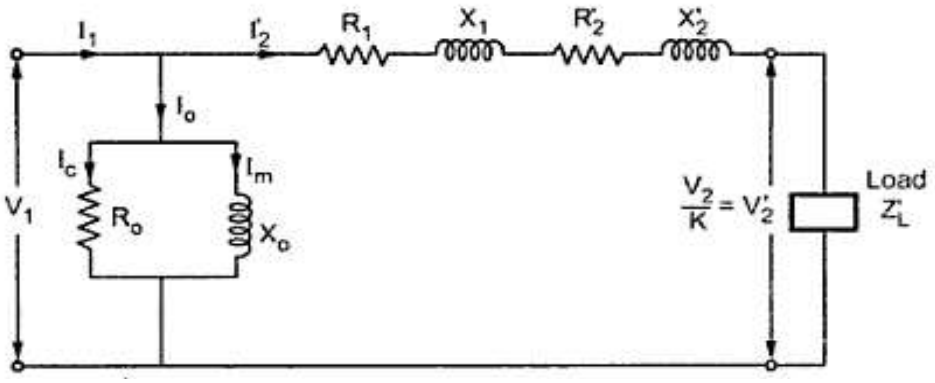


FIGURE 3.10: Simplified equivalent circuit of transformer [162].

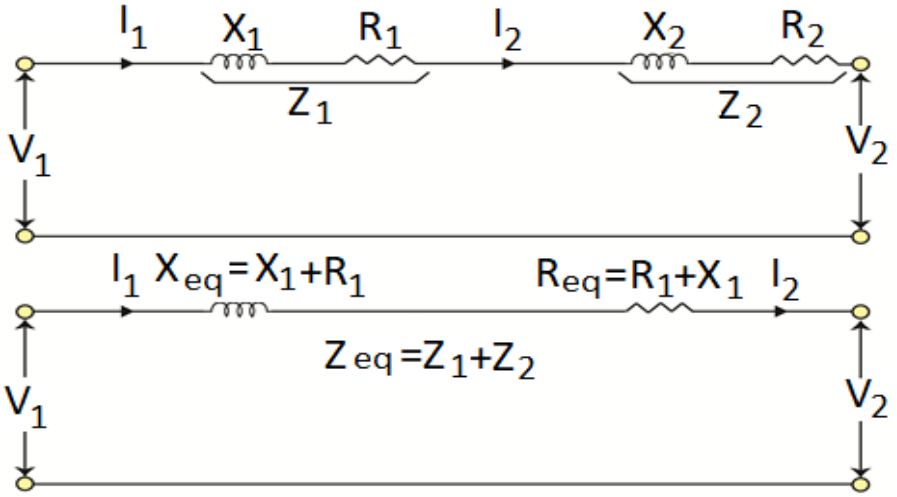


FIGURE 3.11: Approximate equivalent circuit of transformer [162].

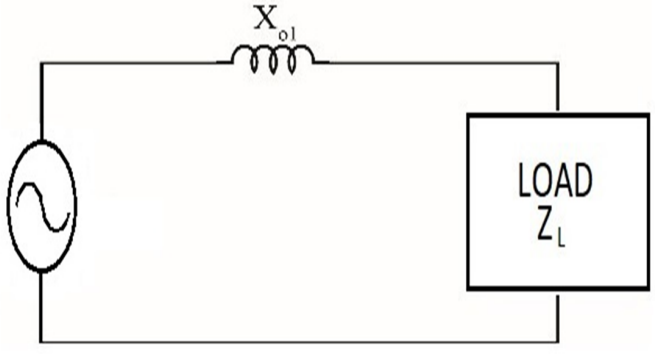


FIGURE 3.12: Approximate transformer circuit [163].

To determine the parameters, some of the relationships are given due emphasis. For the purpose, abandoning any loss, the instantaneous power balance is given as:

$$v_s(t)i_s(t) = v_0(t)i_0(t) \tag{3.13}$$

For inductive load and comparatively high switching frequencies, the load current

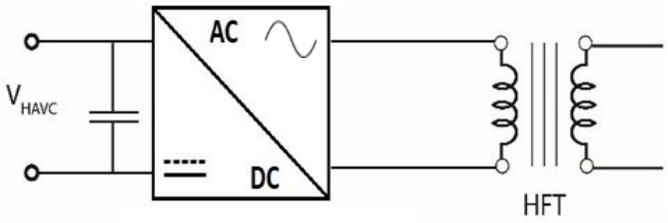


FIGURE 3.13: Most simplified electrical circuit of inverter [164].

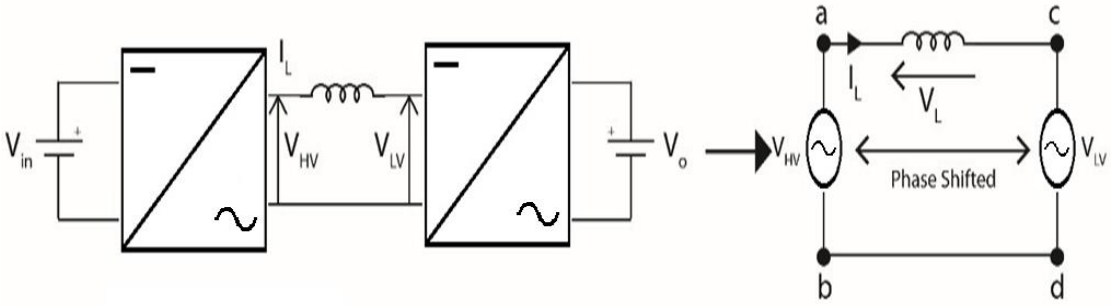


FIGURE 3.14: Simplified circuit of DC-DC converter [164].

and the output Voltage are considered sinusoidal, as the DC supply voltage remains constant, $v_s(t) = V_s$ and DC supply current is given as:

$$i_s(t) = \frac{1}{V_s}\sqrt{2}V_{01}\sin(\omega t)\sqrt{2}I_0\sin(\omega t - \Phi_1) \tag{3.14}$$

or

$$i(t) = \frac{V_{01}}{V_s}I_0\cos(\Phi_1) - \frac{V_{01}}{V_s}I_0\cos(2\omega t - \Phi_1) \tag{3.15}$$

Where, V_{01} is the fundamental RMS (effective) output voltage and can be determined as:

$$V_{01} = \frac{2V_s}{\sqrt{2}}\pi$$

However, for practical purpose, $V_{01} \approx V_0$, I_0 is the fundamental rms load current (independent of phase) and Φ_1 stands for the load impedance angle at the fundamental frequency given as:

$$\Phi_1 = \tan^{-1}\frac{\omega L}{R} \tag{3.16}$$

In single phase half bridge inverter perspective, input source (DC) current to inverter.

$$I_s = \frac{V_{01}}{V_s}I_0\cos(\Phi_1) \tag{3.17}$$

Output voltage of inverter/input to transformer, $V_1 = V_0 = V_s/2$, output current at transformer secondary,

$$I_0 = \frac{V_0}{R_L} \tag{3.18}$$

and

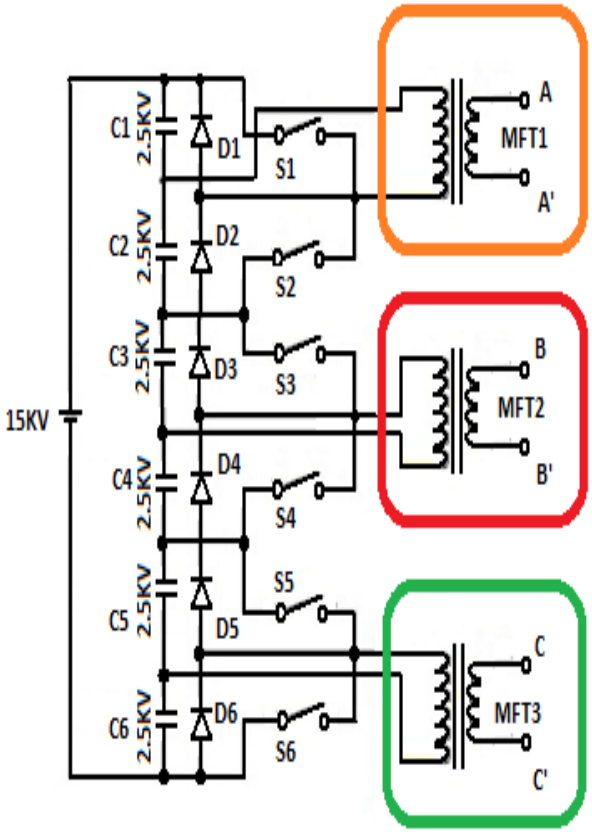
$$I_0 = \frac{V_0}{R_L + j\omega L} \quad \text{for inductive load} \tag{3.19}$$

As per voltage divider rule,

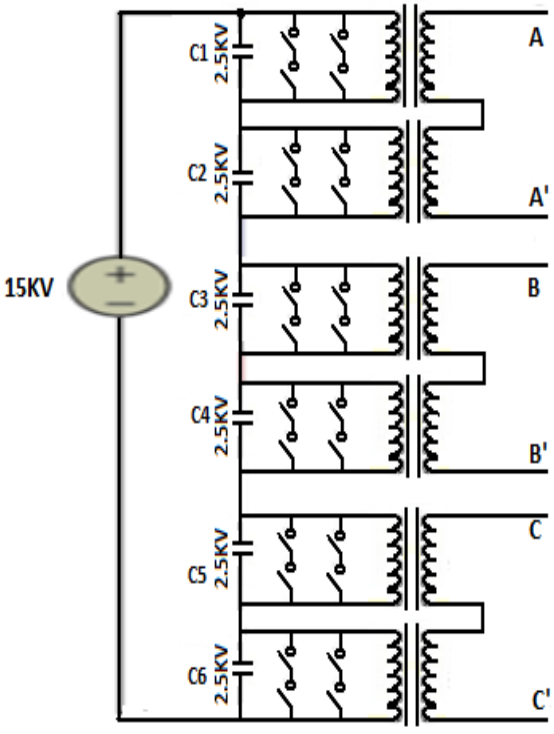
$$V_0 = V_L = \frac{R_L}{R_L + j\omega L} V_{in} \tag{3.20}$$

3.4 Full Bridge Inverter vs. Half Bridge Inverter A Comparison

PWM inverter consists of mainly two arrangements in bridge perspective: (1) Full-bridge high frequency inverters and (2) Half-bridge high frequency inverters. In inverter design scenario, these two arrangements are evaluated in the light of their performance parameters such as cost, size, current ripple or total harmonic distortion (THD), transformer turn ratio, switching power loss etc. The most promising and key difference between a half-bridge and full bridge arrangements lie in the measurement of output voltage. For half bridge configuration, in a single phase, it contains two switches and each of its capacitor has an output voltage equal to half the supply voltage (i.e. $V_{out} = V_s/2$). In addition, the switches complement each other i.e. if one is switched ON, the other one goes OFF. In case of full-bridge design, it is the same output voltage as the dc supply voltage (i.e. $V_{out} = V_s$). Table 3.2 depicts performance parameters of Full Bridge and Half Bridge inverter design and compares operational conditions, whereas Fig. 3.15 illustrates their structural design. For design of Full Bridge Inverter (1Φ), four choppers are used where when two transistors are turned ON simultaneously, the input voltage Vdc, is appeared across the load (i.e. $V_0 = V_{dc}$). Similarly, when other two transistors in bridge are turned ON at the same time, the voltage across the load appeared as inverted/reversed (i.e. $V_0 = -V_{dc}$).



(a)



(b)

FIGURE 3.15: Inverter circuits (a) HB inverter (3Φ) (b) FB inverter (3Φ).

TABLE 3.2: Comparison of parameters (1Φ) [165].

Parameter	Full Bridge	Half Bridge
Cost	1	.86
Size	1	.91
Control Complexity	1	.85
Current Ripples	.98	1
Switching Power Loss	1	.5
Power Transfer Efficiency	1	1
No. of Switches	4	2
No. of Driving Signals	2	2
Complexity Factor	1	.85
Output Voltage	$+V_s$, $-V_s$ (Full)	$+V_s/2$, $-V_s/2$ (Half)
Transformer Turn Ratio for same output	No need to step up	Step up by 2
Average Collector Current	.5	1
RMS Current through inverter switch	.707	1.414
Total Switch Stress	same	same

For analysis and design, IGBTs are used as a switches .The inverter basically contains a power circuit and PWM control circuit to generate the gate pulses to trigger the IGBTs. According to the duty cycle of the gate pulses, these IGBTs can be turn on and off. PWM plays a vital role in controlling power electronic controller such as rectifiers, DC-DC converter, and inverter, etc. Some of the advantages the PWM technique offers as the power loss are very low in the switching devices coupled with less generated noise and minimization of harmonics. Moreover the output voltage can be easily controlled.

3.5 Fixed Load Inverter vs. Variable Load Inverter-A Comparison

A power inverter basically is an electronic device used to transform a DC voltage into AC voltage of variable (requisite) frequency with fixed or variable magnitude.

A power inverter may be entirely electronic or a blend of mechanical effects (like a rotary device) and electronic circuitry. The two mainly employed inverter technologies in Power System applications are PWM inverter and Resonant Inverter. PWM Inverters regulate by adjusting the "ON-time" of the transistor in controlling the width of the pulses in the switching arrangement scenario and are used for the variable load. The resonant inverters are electrical converter based on resonant current oscillation and is used for fixed load i.e. ideally suited for constant load power applications. Main function of these inverters is to reduce switching losses of the devices. Variable load inverters (i.e. PWM inverter) offer many advantages, which includes: (1) Very low Power loss in switching devices with less generated noise and (2) Minimization of harmonics and controllability of output voltage.

3.6 Medium Frequency Power Transformer

Medium-frequency power transformer (MFPT) is taken a one of the key and significant rudiments for high power isolated DC-DC converter in power applications such as the future all-DC offshore wind farms, tractions and solid-state transformers. The transformer portion of an isolated DC-DC converter serves two main purposes. First, the transformers will step-down (reduce) the voltage of the primary (input) side to the secondary (output) side. In this thesis, the same function will be assisted by the transformers in stepping down the voltage from primary side of the transformer to the secondary side of the transformer. The provision of galvanic isolation between inside and outside of the transformer attributes for the second purpose of the transformer. In high frequency perspective, it acts like an AC switch thereby offering the indispensable scaling and then achieving electric isolation to facilitate high voltage and current transfer ratios. In high frequency applications, the magnetic constituents are permitted to be of reduced size; thereby resulting in decrease in inverter volume. This profound factor contributes for high frequency transformer superiority over low and short frequency one.

3.6.1 Medium Frequency Transformer Structure

A transformer has three major components which include the core, the primary or inside winding and the secondary or outside winding. All three components are vital in both transformer construction and transformer selection. A transformer

should be able to provide the desired results while minimizing the various associated losses to maintain the overall efficiency of the scheme. The transformer core can be made from two broad classes of materials. The first class of cores is made from various alloys of iron. The core can be constructed from alloys, which are made principally from iron and small volumes of other elements containing chrome and silicon [166]. These cores are used in applications with frequencies generally below 2kHz due to eddy current losses that increase with higher frequencies. This class of cores can also be furnished from powdered iron and powdered iron alloys. The powdered iron cores are fabricated from small iron particles electrically isolated from each other for provision of greater resistivity than laminated cores. Powdered iron cores have lower eddy current losses than laminated cores and can be used with higher frequencies. The second type of cores is built using ferrites materials, which are basically oxide mixtures of iron and other magnetic elements [162]. Ferrite materials possess large electrical resistivity but low saturation flux densities. Also, ferrite cores have only hysteresis losses. By having no eddy current losses, ferrite cores are ideal cores for high frequency applications. The primary and secondary windings are usually built using copper conductors due to the high conductivity and malleability of copper. The copper wires have a DC resistance that will create power losses, and the high frequencies can cause the power losses to increase greatly for AC power applications due to skin effects [166]. The AC power losses can be calculated after calculating the DC power losses and adjusting the results for skin effects [166]. The skin depth of various frequencies is shown in Table 3.3. The inverter portion of the DC-DC converter will operate at several thousand Hertz, and the problems associated with skin depth will require Litz wiring [162]. Litz wiring twists many smaller copper conductors together to alleviate the skin depth concerns while providing sufficient conductivity to prevent excessive resistance [166]. The term "Litz" came from the German's word "Litzendraht" and means braided/stranded wire [167]. Litz wire consists of a number of small twisted strands isolated from each other and collected together. The litz and solid wires are shown in Fig. 3.16 accordingly.

In SST application, the medium transformer is lighter in weight with smaller size as compared to the existed line frequency transformer. There are two key devise

TABLE 3.3: Skin Depth Effects in Copper Conductors [166].

Frequency	50 Hz	5KHz	20KHz	500KHz
δ	10.6 mm	1.06mm	0.53mm	0.106mm

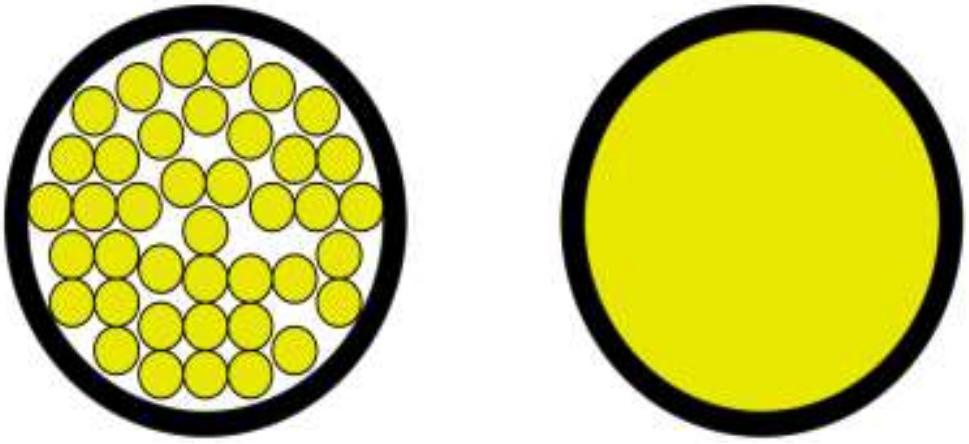


FIGURE 3.16: The wires which are used in the transformer: (left side) litz wire and (right side) solid wire [167].

issues of HV-HF transformer which are inductance optimization and high voltage insulation. To address the inductance requirement issue, a high value leakage inductance with respect to switching frequency of converter is incorporated for proper operation which merits for an important and significant advantage/gain of HV-HF transformer development. The second requirement of high voltage isolation is catered by FEM (Finite Element Method) analysis. Several materials can be considered in transformer design in high power and high frequency perspective, including ferrite, Nano-crystalline and Amorphous [167, 168]. A few types of core material characteristics are briefly summarized in Table 3.4 [136]. Ferrite core has experienced with low loss quality coupled with low saturation flux density (0.5T). Therefore, it is considered appropriate for applications and uses, where operating/switching frequencies exist in the assortment of tens to hundreds of Kilohertz.

3.7 Design Process

Before starting the design of the transformer, the input data should be determined. The input data basically depends on the power capabilities of the output device which is connected to the transformer's output. The operating frequency of the

transformer depends on the input voltage source. In case of a power converter, the operating frequency is usually equal to the switching frequency of the power device. One of the best magnetic materials which can deal with high frequencies is the power ferrite.

In the design perspective, the transformer design basically includes the calculation of area product and then picking suitable transformer core, determining the area of primary and secondary winding, computing the number of turns on the primary and secondary sides, calculating the copper and core loss. A step-by-step design procedure is established for three different transformer types: wire wound, planar and integrated. Generally, the design and fabrication procedure for all transformers is the identical and same, except the part where the winding area needs to be worked out. In case of wire wound structure, it is enough to find the area of the wire and then determine the gauge number. At the same time, for the planar transformer, one more calculation needs to be done in order to find the length of the PCB trace. The whole design structure is based on the equations given in [136]. The initial parameters that are required for the design are mentioned below:

1. Input voltage, V_{in}
2. Output voltage, V_{out}
3. Output power, P_{out}
4. Frequency, f
5. Current density, J
6. Efficiency, η
7. Magnetic flux density, B_m
8. Core material (ferrite, electrical steel and so on)
9. Core configuration (U, E cores)

When designing a high-frequency transformer, one of the main parameters that should be taken into consideration is the skin depth (δ), which is the distance

below surface of the conductor where the current is distributed. If the diameter of the conductor exceeds the maximum wire diameter that corresponds to the skin depth ($D_{skin\ depth}$), it causes large copper loss in the transformer's winding. The skin depth is calculated using the following relationship:

$$\delta = \frac{6.62}{\sqrt{f}} \times K\ (cm) \tag{3.21}$$

TABLE 3.4: Core material specifications [169, 170].

Type of Magnetic Material	**Nano-crystalline**	**Fe-Amorphous**	**Ferrite**	**Silicon**
Manufacturer	Vacuumschmelz	Metglas	Ferroxcube	JFF
Material	Vitroperm500F	2605SA1	3C93	10JNHF600
Saturation flux density, $B_{max}T$ @250°C	1.23	1.56	0.52	1.87
Curie Temperature, T_c°C	600	395	240	700
Max. Operation Temperature, °C	120	150	140	150
Thermal Conductivity (W/Mk)	10	10	4	19.6
Density (g/cm^3)	7.3	7.18	4.5	7.53
Lamination Thickness (mm)	0.023	0.025	0.028	0.1
Core fill Factor	0.7	0.83	1	0.9
Magnetostriction (ppm)	0.5	27	0.6	0.1
Core Loss@ .3T, 20kHz (W/kg)	10	43	8	80

$$D_{skin\ depth} = 2\delta\ (cm) \tag{3.22}$$

$$A_w = \frac{\pi \times D_{skin\ depth}}{4}\ (cm) \tag{3.23}$$

A transformer's output current I_{out} is another important parameter in a transformer. Using I_{out}, the wire area for the secondary side can be determined. The output current can be found as follows:

$$I_{out} = \frac{P_{out}}{V_{out}}\ (A) \tag{3.24}$$

The apparent power of the transformer P_t is basically the sum of the input (P_{in}) and output (P_{out}) power of the transformer:

$$P_t = P_{out} + P_{in} = P_{out} + \frac{P_{out}}{\eta}\ (W) \tag{3.25}$$

One of the main parameters that determine the power handling ability is the area product (A_p), which is the product of window area (W_a) and core area (A_c):

$$A_p = W_a \times A_c \tag{3.26}$$

It is used by engineers to determine the appropriate core size. Equation (3.26) can be rewritten as follows:

$$A_p = \frac{P_t \times 10^4}{K_f \times B_m \times f \times K_u \times J} \ (cm^4) \tag{3.27}$$

where, K_f is waveform coefficient (equals 4 for square waveform and 4.44 for sinusoidal waveforms), B_m is the maximum flux density of the core, J is current density and K_u is a window utilization factor. The maximum flux density, B_m can be calculated by [166, 171]:

$$B_m = \left(10^8 \times \frac{\rho \lambda^2 I_{total}^2}{2K_u} \times \frac{MLT}{W_a A_c^3 MPL} \times \frac{1}{\beta K_{fe}}\right)^{\frac{1}{\beta+2}} \tag{3.28}$$

where, $\rho = 1.724 \times 10^{-6}$ is the resistivity, $\lambda = D \times T \times V_{in}$ is applied volt-seconds, D is the duty cycle, T is the period, I_{total} is the total current, K_u is the winding fill factor, β is the core loss exponent, and K_{fe} is the core loss coefficient.

Once A_p is found, the transformer core can be selected from the manufacturer's datasheet. Moreover, the following core parameters need to be taken from the datasheet for further calculations: mean length turn (MLT), core area (A_c), window area (W_a), surface area (A_t), magnetic path length (MPL) and core weight. Since not all parameters listed above are given in the datasheet, they need to be calculated.

The MLT of the wire wound and planar structures can be found as follows [122]:

$$MLT_{wire} = 2 \times (a + c) + b \times (2 + \pi) \tag{3.29}$$

$$MLT_{planar} = 2b + 2c + 2.82a \tag{3.30}$$

where a, b and c are core dimensions that can be found in the Figs. 3.17 and 3.18.

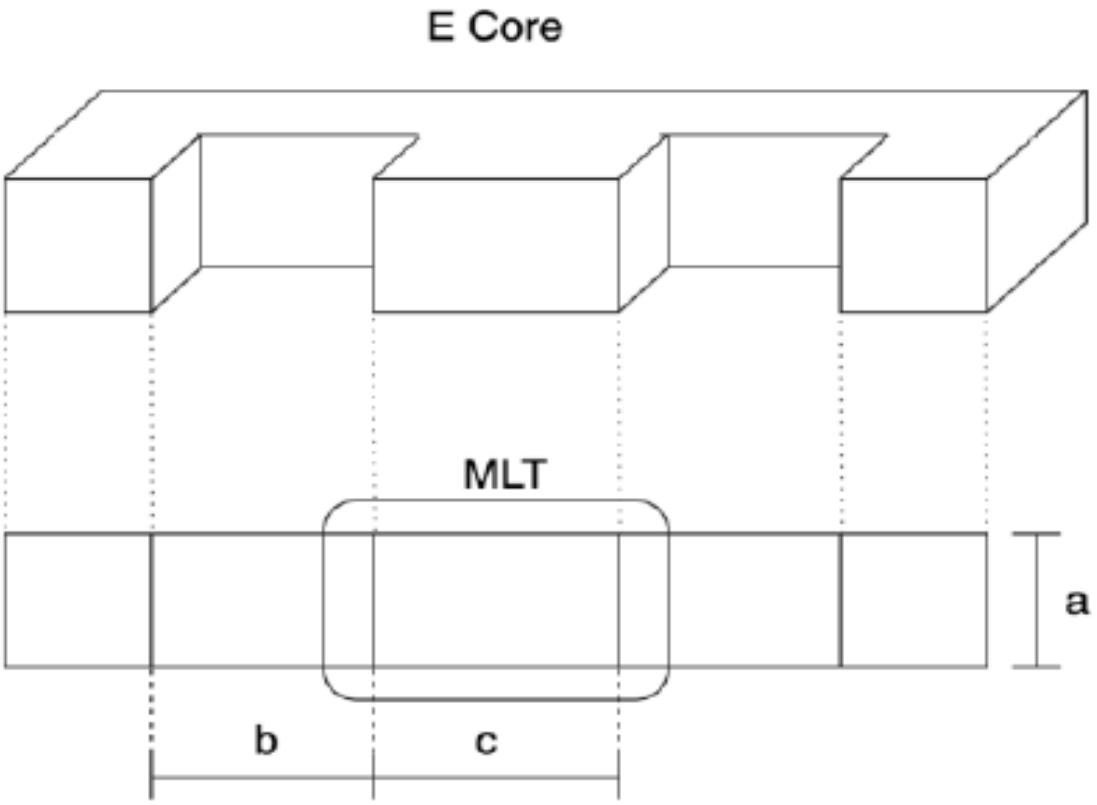


FIGURE 3.17: Mean length turn of the wire wound transformer [122].

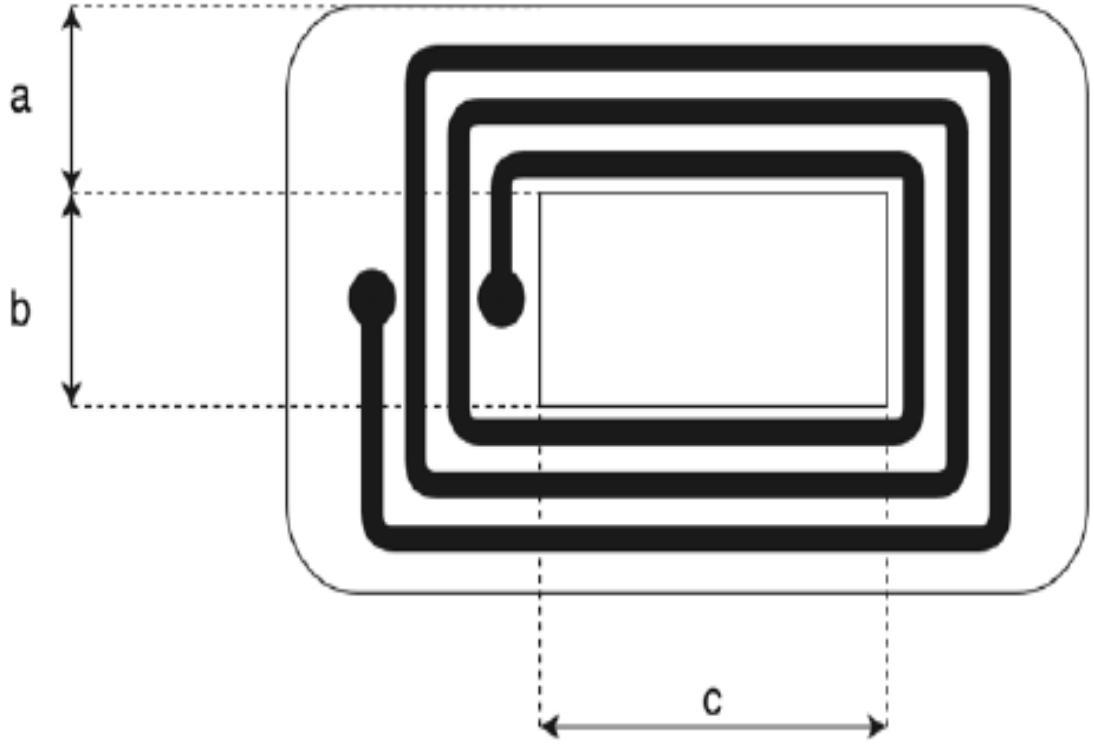


FIGURE 3.18: Mean length turn of the planar transformer [122].

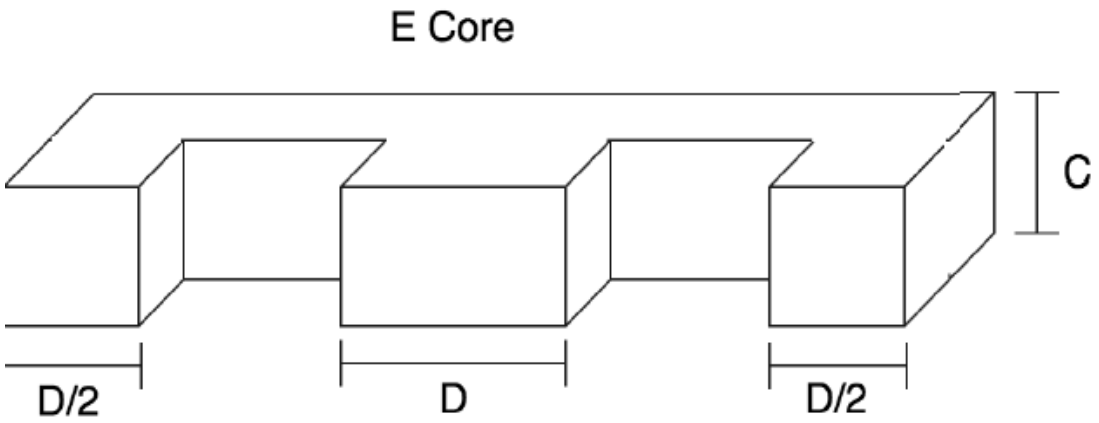


FIGURE 3.19: The E core's dimensions for determining the cross-section area A_c [122].

One of the main parameters in the datasheet is cross-sectional area of the core. It is used to calculate important parameters such as leakage inductance and magnetizing inductances. It can be found by the following equation:

$$A_c = C \times D \tag{3.31}$$

where C and D are the core dimensions which are shown in the Fig. 3.19. Surface area (A_t) of the transformer core can be found using Eqs. (3.32)-(3.35) wherem dimensions of the core are shown in Fig. 3.20.

$$\text{End} = \text{Height} \times \text{Length} \tag{3.32}$$

$$\text{Top} = \text{Length} \times \text{Width} \tag{3.33}$$

$$\text{Side} = \text{Height} \times \text{Width} \tag{3.34}$$

$$A_t = 2 \times \text{End} + 2 \times \text{Top} + 2 \times \text{Side} \tag{3.35}$$

The window area of the transformer can be calculated as follows:

$$W_a = A \times B \tag{3.36}$$

The number of primary (N_p) and secondary (N_s) turns can be found by using Faraday's law:

$$N_p = \frac{V_{in \times 10^4}}{K_f B_m f A_c} \tag{3.37}$$

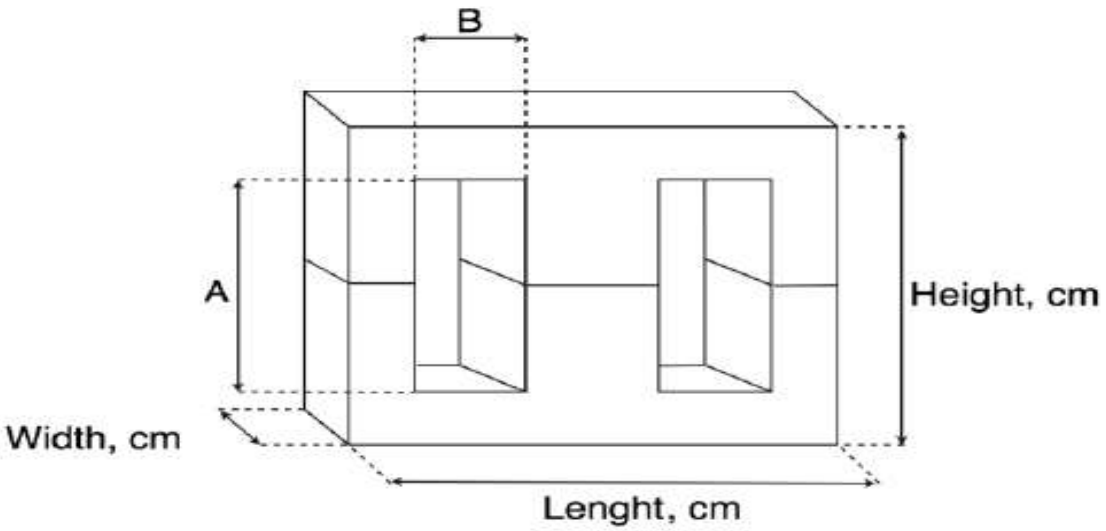


FIGURE 3.20: Dimensions of the core needed to find surface (A_t) and window areas (W_a) [122].

$$N_s = \frac{N_p V_{out}}{V_{in}} \tag{3.38}$$

Primary current (I_p) of the transformer can be found in the following:

$$I_p = \frac{P_0}{V_{in} \times \eta} \ (A) \tag{3.39}$$

where η is the desired efficiency of the transformer.

The next important parameters which need to be calculated are the wire area of primary (p) and secondary (s) conductors. They can be calculated by using Eqs. (3.40) and (3.41):

$$A_{wB}(p) = \frac{I_p}{J} \ (cm^2) \tag{3.40}$$

$$A_{wB}(s) = \frac{I_{out}}{J} \ (cm^2) \tag{3.41}$$

Designers should be careful when choosing the current density value (J). For example, if the current density is chosen to be very high, it will cause additional winding loss.

After wire the areas are calculated, those values are used to find the appropriate wire gauge number (AWG), which can be selected from the table given in [172]. Since a high-frequency transformer is being designed, as opposed to a low frequency transformer, it is highly recommended to use litz wires instead of solid wires. From

[173, 174], it is known that the litz wires reduce skin effect losses and consequently winding loss because they consist of multiple isolated strands and each strand has the diameter which is equal or smaller than $D_{skin\ depth}$.

In the case of the planar and integrated transformers, by knowing the gauge number, the trace length of the copper sheet/PCB can be determined using the following equation:

$$\text{Legth of the trace} = \frac{\text{Wire area}}{\text{Skin depth}} \tag{3.42}$$

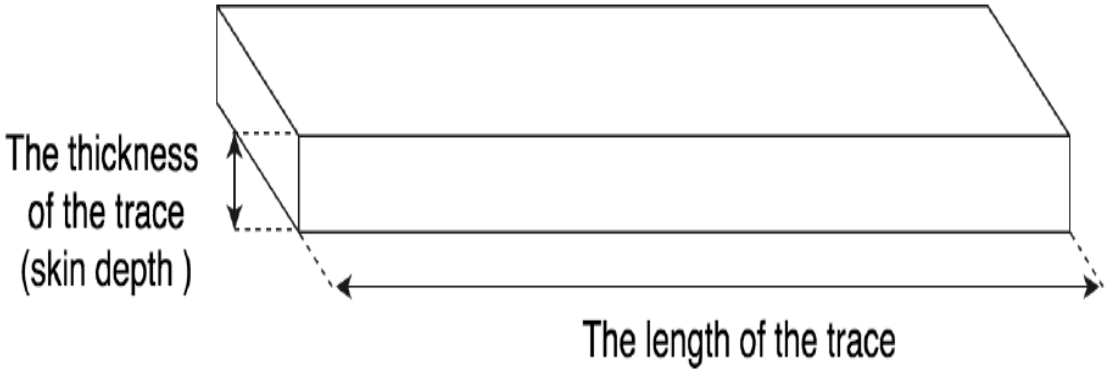


FIGURE 3.21: Dimensions of the PCB/copper sheet trace [173].

The primary (R_p) and secondary (R_s) DC winding resistances are used to calculate copper/windings loss in the transformer. They can be calculated as follows:

$$R_p = MLT \times N_p \times \frac{\mu\Omega}{cm} \times 10^{-6}\ (\Omega) \tag{3.43}$$

$$R_s = MLT \times N_s \times \frac{\mu\Omega}{cm} \times 10^{-6}\ (\Omega) \tag{3.44}$$

where $\mu\Omega/cm$ is the winding resistance of the conductor, which can be obtained from [172].

The final stage of the design is the determination of the loss existing in the transformer. These losses are broken up into two components: core losses and winding losses. The primary (P_p) and secondary (P_s) winding loss and total winding loss ($P_{winding}$) can be found as follows:

$$P_p = I_p^2 \times R_p\ (W) \tag{3.45}$$

$$P_s = I_0^2 \times R_s \ (W) \tag{3.46}$$

$$P_{winding} = P_p + P_s \ (W) \tag{3.47}$$

The core loss density in mill watts per cubic centimeter ($\mathrm{mW/cm^3}$) can be found as:

$$\frac{mW}{cm} = a \times f^x \times B_m^y \tag{3.48}$$

Coefficients a, x and y depend on the magnetic material which is used for the transformer core and can be derived from the core loss curve in the manufacturers datasheet.

The core loss of the transformer can be found by multiplying core loss density by core volume, V_{core}:

$$P_{core} = \frac{mW}{cm^3} \times V_{core} \ (W) \tag{3.49}$$

The total loss of the transformer (P_ϵ) can be calculated as the sum of winding and core loss:

$$P_\epsilon = P_{winding} \times P_{core} \ (W) \tag{3.50}$$

The watts per unit area, ψ is used to estimate the core loss density and can be calculated by dividing total loss by the surface area:

$$\psi = \frac{P_\epsilon}{A_t} \ (W/cm^2) \tag{3.51}$$

Finally, the last part that has to be done when designing the transformer is a temperature rise calculation. There are two allowable temperature rises above the ambient temperature: 25 and 50 degrees Celsius. The figure below shows the relationship between total surface area of the core (A_t) and total power loss (P_ϵ) for both 20°C and 50°C.

The temperature rise of the transformer (T_r) can be found as follows:

$$T_r = 450 \left(\frac{P_\epsilon}{A_t} \right)^{0.826} \tag{3.52}$$

If it turns out that the calculated temperature rise is higher than desired one, the design process needs to be started from the beginning by picking another core with

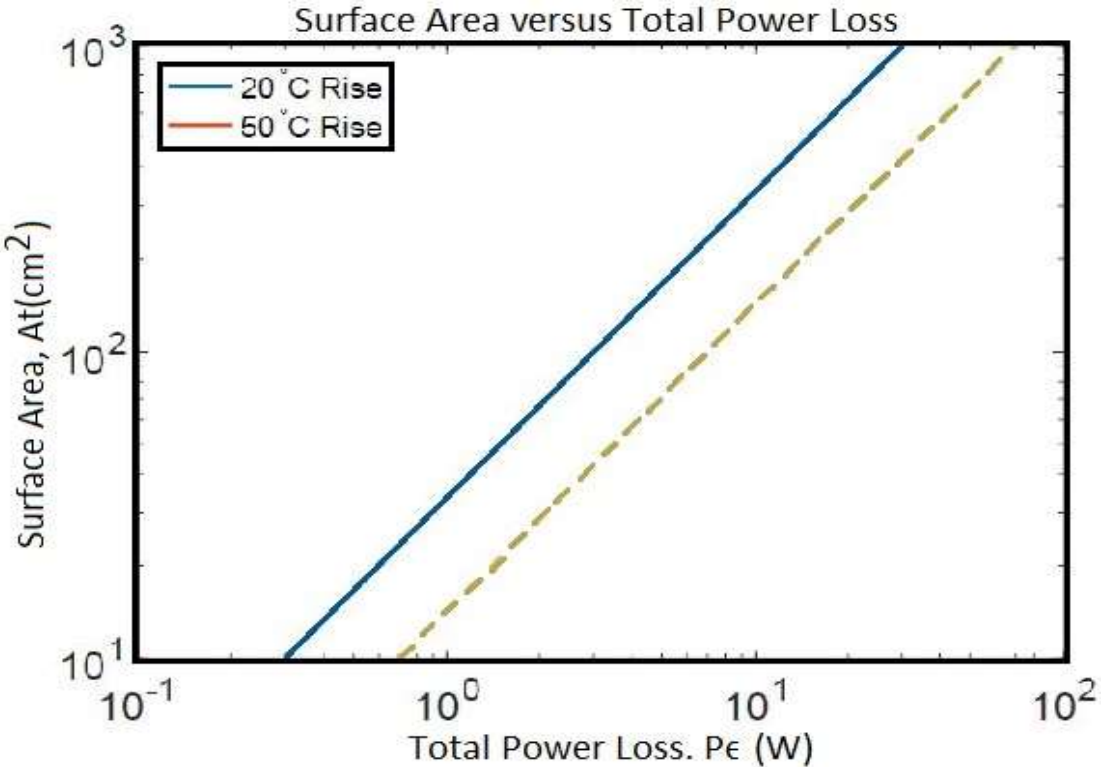


FIGURE 3.22: Surface area versus total power loss [173].

a higher surface area.

The design process is based on the above stated equations. The main challenge at this step is to choose the appropriate core size. Choice of core size is vital as an undersized core can cause a high temperature rise and fast saturation of the magnetic material as the current increases. Conversely, choosing a large core can cause the system to be cumbersome, which is not desired since the main advantage of the high-frequency operation is the size reduction of all power components. After the design is done, three transformer cores 0P46527EC for the wire wound, 0R49938EC for the planar and U46/40/28 for the integrated structures are chosen from the manufacturer datasheet. The core's data is given in Table 3.5.

The planar transformer consists of a planar core 0R49938EC from Magnetics Inc. and two printed circuit boards (primary and secondary) [173, 174]. The PCB windings are shown in the Fig. 3.23. The wire wound transformer consists of the EE core 0P46527EC [175], primary winding has AWG 12 and secondary winding has AWG 8. For both windings, type 2 litz wire was used to reduce the skin effect. Operating at frequency from 10kHz to 20kHz, the recommended wire guage for

TABLE 3.5: Transformer's core data [172].

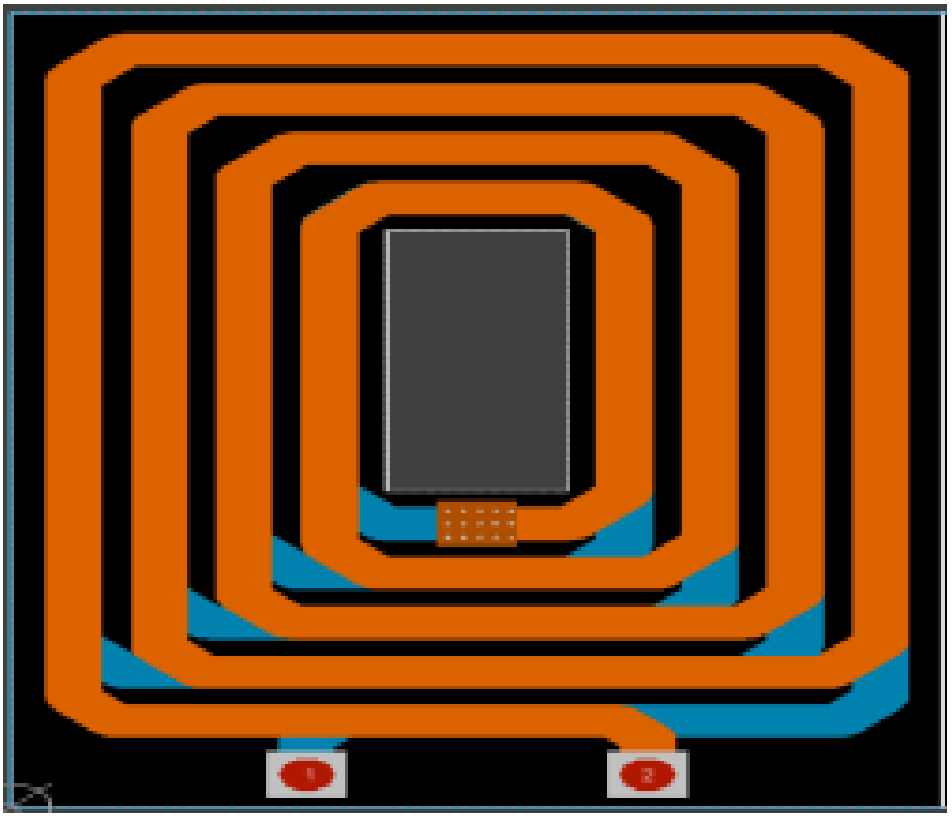
Core name	**0P46527EC**	**0R49938EC**	**U46/40/28**
Area product, A_p (cm^4)	25	46	40
Mean length turn, MLT, cm	12	20.4	11
Cross-section area, A_c (cm^2)	5.4	5.44	3.92
Window area, W_a (cm^2)	5.37	9.57	9.18
Surface area, A_t (cm^2)	156.74	190	142.68
Magnetic path length, MPL, cm	14.7	14.8	18.2
Core weight, W_{tfe} (grams)	410	400	364

litz ire construction is 33 AWG [176]. The integrated transformer has AWG 12 for the primary side and 1 mm thick copper sheet for the secondary side. The cores that were selected have an area product that is higher than calculated one due to the temperature rise issues.

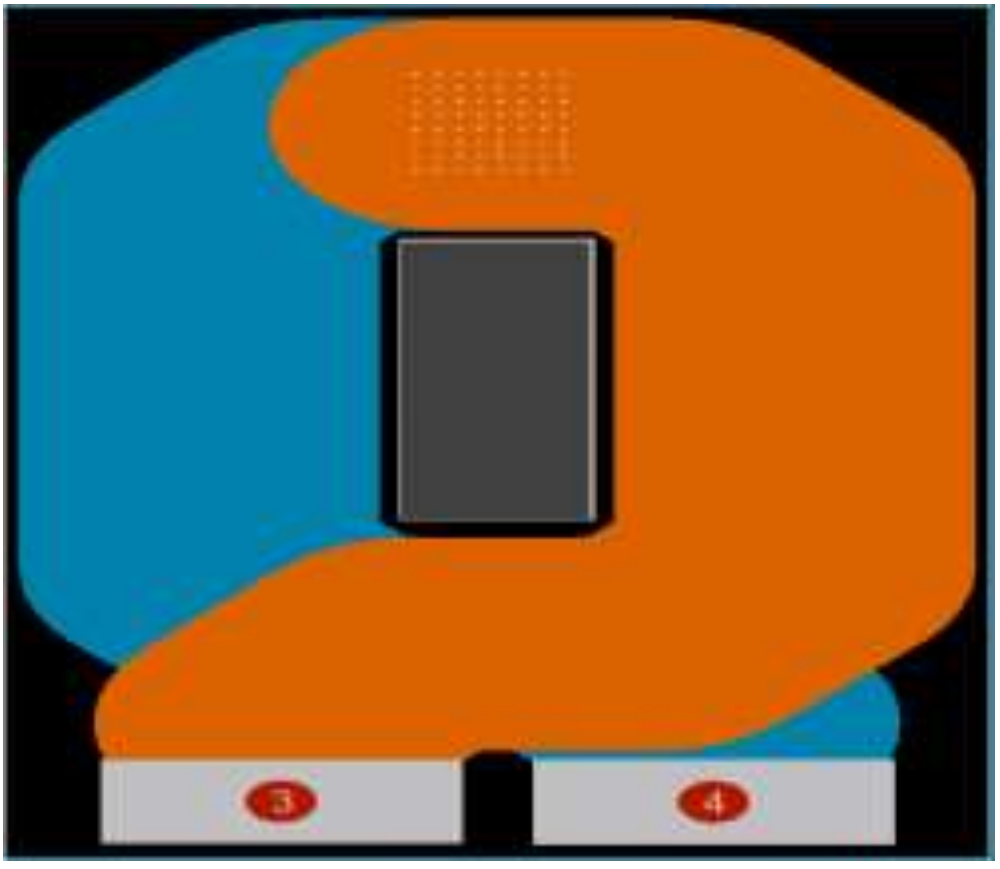
3.7.1 Planar Transformer

The planar transformer was invented in 1980s and during the next decade became very popular among the designers and manufacturers because of their thermal characteristics, low profile and cheap and simple production. The windings in the planar transformer are employed on the printed circuit board (PCB), which can be one or multiple layers as per requirement of the system under consideration. The typical PCB winding for the planar transformer is shown in Fig. 3.24. Copper sheets can also be used when building the planar transformer. Especially for the secondary side, this usually has just one turn. The copper sheet has the same advantages as the PCB in terms of proximity and skin effect minimization. Moreover, the cost and production time of the copper sheet is usually lower those for the PCB. The typical copper sheet used in the planar transformers is shown in Fig. 3.25.

Along with the litz wires, the PCB winding has also advantage of reduced skin effect because the thickness of each trace is made such that it is smaller than or equal to a skin depth. To better cope with the proximity effect, the interleaving method can be implemented when designing the PCB.



(a)



(b)

FIGURE 3.23: (a) Primary and (b) secondary PCB windings [174].

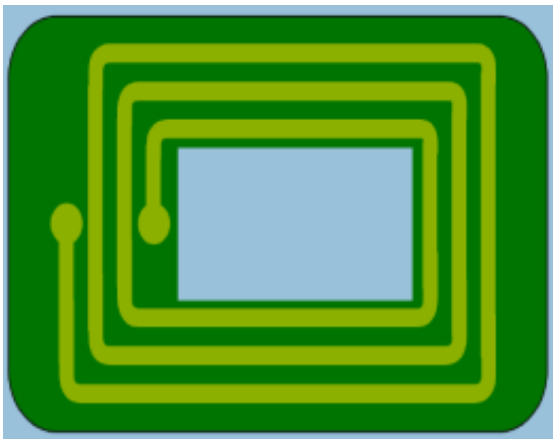


FIGURE 3.24: The printed circuit board [175].

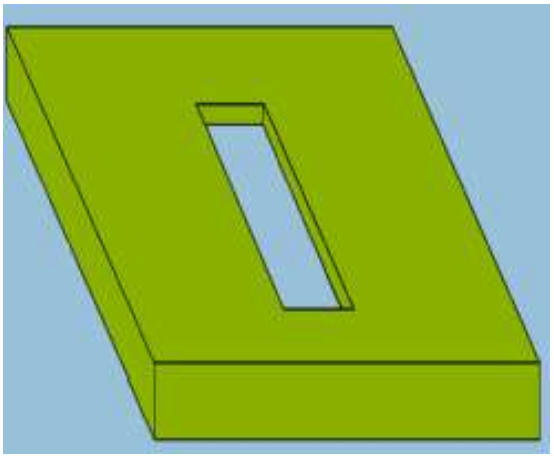


FIGURE 3.25: The typical copper sheet [175].

Higher power density with a lower profile in regards to HF transformer design can be achieved if a planar transformer is encased and encapsulated using coils inside and within multilayer printed circuit board (PCB) as compared to conventional wire-wound transformer, particularly in manifold module system applications. In this approach transformer windings are etched and engraved within the PCB and therefore are totally reoccurring. For reduction of corona and partial discharge, the solid insulation excluding air is utilized by the planar transformer so that SST liability can be improved. In Fig. 3.26, a transformer prototype containing a pair of PC40 PQ107/87/70 ferrite cores customized, for obtaining considerable lesser profile while maintaining the anticipated cross sectional area is presented. After having necessary improvement, according to an estimation the transformer total window height is reduced from 56 mm to 4.55 mm, with the turn ratio 15:12 (step down) [177].

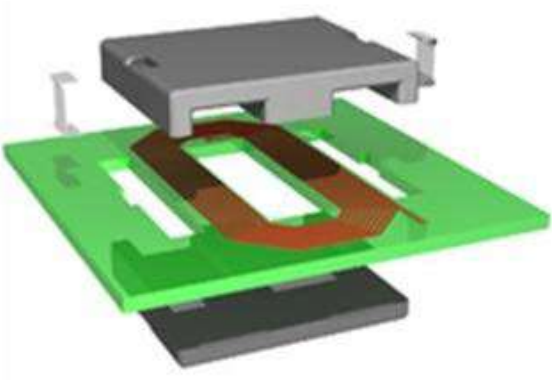


FIGURE 3.26: The planar transformer [177].

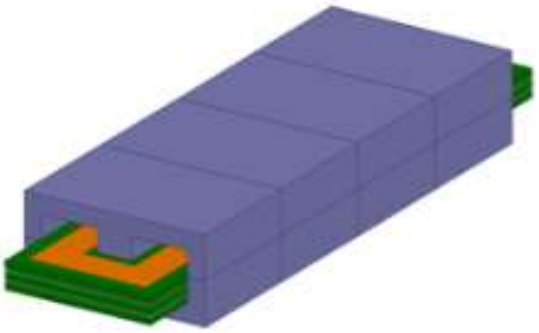


FIGURE 3.27: Multiple core PCB transformers [178].

The multiple cores are incorporated wherein the cores are to be settled in a fasion so that a larger area is obtained as shown in Fig. 3.27 [178]. A transformer with ferrite core resembles as ferrite core transformer. It makes use of a ferrite core owing to the increase value of magnetic permeability. In high frequency applications, these types of transformers are proved to be useful in offering extremely low losses. Such merits make these transformers viable in switch mode power supply (SMPS), SST and RF related applications, etc. Various type of shapes and sizes of ferrite core transformers are available reliant on the application/requirement. Mainly it is found in electronics application instead of electrical use. E core is the most common shape in the ferrite core transformer and Fig. 3.28 exhibits such type of ferrite core transformer in E core shape [149].

3.7.2 Exploration of Transformer Core Losses

The core loss may be premeditated using following empirical relationship:

$$P_{cl} = V_e C_m f^x B_{ac}^y \tag{3.53}$$

FIGURE 3.28: Ferrite core transformer in E-core shape [149].

Where, V_e illustrates the transformer effective core volume; C_m, x, and y are the dealt as coefficients related to the core material; Bac represents the maximum flux density and is articulated as:

$$B_{ac} = \frac{V_T D}{2 N_p A_e f} \tag{3.54}$$

Here, N_p indicates the number of primary turns, V_T stands for applied voltage on the primary side of transformer and D is the duty cycle, which is 0.5 for both the arrangements. It has been noticed earlier that in case of DAB arrangement, $V_T(\text{out}) = V_{in}$ and for DHB (Half Bridge) arrangement $V_T(\text{out}) = V_{in}/2$. It is also validated that the converter with half bridge arrangement possesses much lesser/lower core loss as compared to the converter with full bridge configuration whilst incorporating the same switching frequency as well as the same transformer core effective cross-sectional area. It is also validated that the converter with half bridge arrangement possesses much lesser/lower core loss as compared to the converter with full bridge configuration whilst incorporating the same switching frequency as well as the same transformer core effective cross-sectional area. Such fact has been verified from prototype transformer whose deliberated core loss at 176°F (800°C) in regards to V_T and f reveals that for high frequency (i.e., 50kHz) operation, the core loss for DAB with $V_T = 500$V is almost 10.56W; where as in case of DHB the core loss with $V_T = 250$V is 1.778W. As the frequency and V_T are inversely proportional to each other; therefore lower the core loss is. Numerous techniques exist to estimate the core losses, out of which, the famous are Steinmetz Equations. These equations are depicted in Table 3.6 [173].

TABLE 3.6: Steinmetz equations [173, 179].

Method	Waveform	Power Equation
Original Steinmetz equation (OSE)	Sine	$K.f^{a}.B_{m}^{\beta}.D^{\beta}$
Modified Steinmetz equation (MSE)	Non-sine	$\left(\frac{8}{\pi}\right)^{\alpha-1} K.f^{a}.B_{m}^{\beta}.D^{\beta-\alpha+1}$
Improved generalized Steinmetz equation (IGSE)	Non-sine	$2^{\alpha+\beta}.Ki.f^{a}.B_{m}^{\beta}.D^{\beta-\alpha+1}$

3.7.3 Evaluation of Leakage Inductance for MF Transformer

Leakage inductance in fact is an inductive element existed in a transformer as a result of deficient and imperfect magnetic linkage of one winding to another. For illustration, any magnetic flux which will not function for linkage of primary winding with the secondary winding will result in inductive impedance in series with the primary winding; hence such type of "leakage inductance" is assumed on a schematic diagram as an additional inductance before ideal transformer primary winding.

Recently, in high power applications, an appreciable and increased interest has been noticed in the field of electronics for developing isolated dual active bridge (DAB or DHB) converters [180]. Such equivalent circuit design contains two square voltage waveforms on two sides (primary/secondary) of the transformer. This arrangement results in application of full voltage on the inductance, L for shaping the current to act as a power transfer component [181]. For achievement of zero-voltage switching (ZVS), a phase shift angle between the bridges, ϕ must be greater than a certain given value so that the lowest series inductance value be obtained as is evident from below calculations as:

$$L_{min} = \frac{V_{DC1} V_{DC2} \Phi_{min} (\pi - \Phi_{min})}{2 P_{out} \pi^{2} f_{s} n} \tag{3.55}$$

Where V_{DC1} and V_{DC2} indicate the input and output DC voltages of the DC-DC converter respectively; Φ_{min} is the minimum possible required phase shift between the primary voltage and secondary voltage of the MF transformer stressed as the

significant part of the DAB converter. Pout represents the output power, n is the turns ratio of the transformer and f_s is the operating frequency (i.e. switching frequency) of the medium frequency transformer. The inductance in series with primary may be depicted as an integrated leakage inductance, $L\sigma$ in HF transformer, in order to reduce the number and size of components, hence contributing towards achievement of higher power densities. However,the insufficient and less value leakage inductance may lead to soft switching shift,thereby adversely affecting the converter efficiency. Similarly,the higher values of such leakage inductance may cause unnecessary reactive power circulation within the converter. This action ultimately become a source to decrease the efficiencyas well as output active power of the converter, coupled with expanding the soft-switching region to some extent. In this context, it is not appreciable , rather undesirable.

To estimation, the required series inductance (i.e. leakage inductance) for DC-DC converter can be calculated as:

$$L_s = \frac{V_H}{sd\pi^2 f_s P_0}.|\Phi|(\pi - |\Phi|) \tag{3.56}$$

Where, L_s represents the required leakage inductance; V_H is input high voltage; d parameter is given as $(V_H N_L / V_L N_L)$ and ranges as 0.9-1.1; f_s is operating or switching frequency (2kHz); P_0 denotes the DAB output power and Φ is the phase-shift angle between two H-bridges [182].

In the present case, V_H = 7500V; $\Phi = 20°$ (i.e., $\pi/9$) for estimation, $d = 1$; f_s (Switching Frequency) = 2kHz.

P_0 (Power rating per transformer = 6.7KVA

$L_s = [7500(\pi - \pi/9)]/([2 \times 1 \times \pi^2 \times 2000 \times 6700]) = 27.6mH$

For P_0 = 378.125KW, L_s = 0.50mH

3.8 Performance Parameters of Inverters

Normally, an inverter is analyzed operationally based on most significant aspects such as: (1) Total Harmonic Distortion (THD) and (2) Efficiency [88, 183, 184].

Measure of harmonic distortion in system is termed as THD. Conceptually it is a capacity and appraisal of closeness in shape between a waveform and its fundamental component. It may be deliberated as the ratio of the powers of all harmonic components to the power of the fundamental frequency. THD is an imperative in numerous types of systems, where low THD contributes for an enhanced PF, lesser peak currents, and higher efficiency.

Mathematically, THD may be expressed as:

$$\text{THD} = \frac{1}{V_{01}} \left(\sum_{n=3,5,7}^{\propto} V_{on}^2 \right)^2 \tag{3.57}$$

In terms of current:

$$\text{THD} = \frac{I_H}{I_F} \tag{3.58}$$

is

$$\text{THD}(\%) = 100 \times \sqrt{\frac{P_2 + P_3 + P_4 + \cdots + P_n}{P_1}} \quad \text{where} \quad P_n \text{ is in Watts}$$

Similarly for measurement data in volt, then

$$\text{THD}(\%) = 100 \times \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}{V_1}} \quad \text{where} \quad V_n \text{ is the RMS Voltage}$$

[**Note:** $P(W) = 0.001 \times 10^{p/10}$, Where P is in dBm, $V_{RMS} = V_{pk}/\sqrt{2}$]

Broadly, efficiency is a measurable and reckonable notion, which is quantitatively elaborated by the ratio of output to input. In this exploration, input power is the power quantity, which is provided by the rectifier stage while the output power is the power quantity delivered at output of the inverter. Therefore, the efficiency of an Inverter is given as:

$$\eta_{inv} = \frac{P_{AC}}{P_{DC}}$$

Where P_{AC} is AC power output measured in watts and P_{DC} is DC power input in watts. Inverter efficiency is predominantly determined by the inverter topology,

the power transistors, switching frequency, switching type and filters. Particularly, the losses in the power switches are considered to be a function of the DC input voltage. High feature sine wave inverters are evaluated at 90-95% efficiency, whereas the lower quality modified sine wave inverters are less efficient 75-85%. High frequency inverters are commonly more proficient than low-frequency ones.

3.9 Efficiency Enhancement Techniques - Brief Overview

Efficiency of a high voltage inverter of an isolated DC-DC converter stage of SST is of prime importance in wake of the escalating energy cost and its continuous and uninterrupted operation. Techniques adopted for the purpose are: (1) Phase-shifting of a converter with a fixed value inductor (e.g. 90μH) and subsequently with adaptive inductor incorporating ZVS, thereby getting measured efficiency up-to 97%, using 50KHz bidirectional DC-DC converter module, operating in ZVS mode only within a limited region and (2) Zero Voltage Switching (ZVS), incorporating a snubber circuit placed across semi-conductor components in order improve the performance. There exist a variety of snubbers, but the most practicable and appropriate ones are : (a) RC-snubber [166] and (b) RCD turn-off snubber [185]; however as per Undeland [186] an arrangement with parallel capacitors depicts lossless snubber to obtain ZVS with measured efficiency till 98%. (3) Partial Power Decoupling Technique for operating efficiency DC- AC converter in response and reaction to the boost-type power decoupling scheme and (4) Appropriate choice of inverter switches duty cycle from variation range.

3.10 Summary

The dynamic mathematical model of solid state transformer was presented in this chapter. This model presented for each SST constituent in voltage parameters perspective. Subsequently, the mathematical parameter calculations of five parts (rectifier on higher voltage side , high frequency PWM inverter, medium frequency

transformer, rectifier on lower voltage side and lastly low frequency inverter) of SST were anticipated. Execution of full bridge and half bridge topology arrangements in inverter design were highlighted; thereby proposed three various eventualities. From analysis of these eventualities, it was concluded that half bridge topology favored the need in terms of lesser number of components, cost and efficiency etc. Subsequently, it deliberated the modeling of inverter with transformer system and gave a skeleton overview of the key differences between full bridge and half bridge configurations in parameter perspective. Main differences between fixed load inverter and variable load inverter were also stressed. Medium Frequency Transformer in construction perspective was also appraised, in particular as a planar transformer adopting PCB approach. Performance parameters were also deliberated. These evaluations are being implemented in the succeeding chapter for high frequency PWM inverter design.

Chapter 4

Design Philosophy

This chapter discusses in detail the research design process of the Pulse Width Modulated Inverter in Solid State Transformer applications. It has mainly relied on the research problem to guide on the methodological choice. Firstly it highlights the design methodology of the inverter in half bridge configuration, specifying topology and power devices. Then it deliberates on mathematical modeling of the Inverter in a single phase as well as three phase half bridge topology scenario. Harmonic analysis of the inverter is also given due consideration. In wake of design process, this chapter concentrates on specification and design parameters, leading to the ultimate design of the requisite PWM Inverter. Later, this design is evaluated mathematically as a single phase as well as three phases in the light of various performance parameters. Besides, the design and the approaches implemented to enhance the efficiency, validity and reliability, the inverter losses are also enlightened in detail. Snubber circuit is also given due consideration from construction perception, highlighting its various types. This chapter ends with the analytical evaluation of the inverter losses covering switching losses as well as conduction losses.

4.1 Design Overview

With the progression of power electronic technology, the implementation of inverter applications presents new challenges and experiments in the transformer design owing to high-frequency, and high current/voltage operations. The foremost deliberations for designing a high frequency PWM inverter in half bridge

arrangement were investigated, analyzed and explored in chapters-2 and chapter-3. Those contemplations established the basics for the anticipated high frequency PWM inverter design methodology for 100KVA Solid State Transformer and now are presented in this chapter. Half bridge topology configuration possesses specific advantages over the rest of the existed conventional configurations, especially with a perspective of the parameters such as low cost, low size being less than 80%, low control complexity, lesser number of switches with low power losses and above all, half of the output voltages, as a major requirement for our projected system. Along-with other requirements, the emphasis is also laid for achievement of an efficient and optimum inverter which should deliver stable square wave output with requisite peak voltage of the specific value at rated power in all three phases, which is in fact, the input to the subsequent stage i.e. MFT. To ensure the voltage stability of this design under static load, the efficiency performance parameter may well be evaluated for different value loads. During this trial there should not be the significant deterioration/fall of the outcome with respect to input. The specification and parameters/values of the electronic components of design may be assorted as per mathematical evaluation and research objective. Due to the presence of fewer number of semiconductor switches in half bridge topology, the losses encountered should be lesser and the output may not be affected. There are almost three types of losses occur in inverter fabrication namely as snubber losses, switching losses and conduction losses. The snubber losses are considerably constant which are measured/ calculated as output power minus input/source power.

4.2 Design Methodology

Three phase inverters are mainly used to provide three-phase loads using separate single-phase inverter. To acquire three phase inverter voltages, the gate signal of each single-phase inverter ought to be advanced / delayed by 120 degree with respect to each other. Medium frequency transformer (MFT) secondary windings might be connected either in star or delta configuration, whereas primary windings should be isolated (quarantined) from each other. In practice, for fabrication of three-phase bridge inverter, the two types of conduction are considered, primarily dependent on the control signal incorporated to drive the six transistors with

120 degree or 180 degree conduction. In case of 120 degree conduction, only two switches/transistors conduct at the same time such that each switch conducts for 120 degree and remains OFF for rest of the cycle (i.e. 240 degrees). This means that only two switches remain "ON" at any instant of time. However, in case of 180 degrees conduction, the three switches remain ON (i.e. conductive) at any instant of time. From operation point of view , in case of half bridge inverter (i.e.1Φ), once one switch is turned on(i.e. operational) for duration of half of time period in one phase , the instantaneous voltage perceived at output across the load equals to, $\mathbf{V_0 = V_s/2}$. Correspondingly, if the only second switch is turned on for operation in the same phase for duration of half of time period, then at the output across the load , the load voltage appears to be measured as , $\mathbf{V_0 = -V_s/2}$. In inverter operation, the output voltage can be improved using a regulator/controller itself in the inverter circuitry. With help of this controller, a continuous dc input voltage is received into the inverter. In this fashion an unflappable ac square wave output voltage is retrieved by controlling the ON and OFF duration of the inverter entities. In order to accomplish inverter design with maximum power density in paramount efficiency, a number of configurations, constituents, parameters that contribute towards the manifestation of the design have to be deliberated extensively where weight, expenditure, simplicity of construction/design and efficiency etc. are prominent. In the circuit construction perspective, the power switches, DC supply, DC-link capacitor, snubber circuits and miscellaneous parts such as control & protection board etc. are obvious. Therefore to lead to design /development of three phase PWM inverter, there is a dire need to work out the methodology to design the requisite inverter keeping in view the desirable and constraints etc.

4.2.1 Topology Implementation

To discourse the constraints, the foremost parameter to be addressed is the selection and implementation of the requisite inverter design topology/configuration. In this study, the evaluation of two inverter bridge topologies i.e. Half bridge topology and Full bridge topology is undertaken. The importance of half bridge configuration is emphasized in terms of output voltage, number of bridges and

number of switches etc. attributing towards low cost and simplification of the circuit. The Half Bridge arrangement merits for the reasons as: (1) Output voltage is half as compared Full Bridge voltage requirement (i.e. step down) (2) The number of bridges required is also half as compared to full bridge topology (3) Sufficient simplification of a power scheme layout (4) Reduction in complexity of control and protection circuit coupled with the reduced converter price. Hard switching with PWM technique is opted to control the power converter.

4.2.2 Assortment of Power Devices

With increase of semi conductor's technology, the applications of inverters are being extending in various areas. In case of single phase inverter, the waveform of output voltage is delivered using PWM technique. This arrangement contributes for attainment of the output voltage/output current to be rectangular with reduction of the voltage THD. Moreover the converter efficiency of the system reported as appreciable at full load. Improved efficiency at rated power means a smaller heat sink and enhanced reliability. The fabrications with IGBT switches in higher blocking voltages may result in reduced conduction losses. To estimation, the switching energies pertaining to 6.5 kV IGBTs found to be existed in the order of 20% and 50% greater as compared to 4.5 kV and 3.3 kV IGBTs switches correspondingly. IGBTs carry out their function in two states; thereby producing two types of losses, which include the switching losses and conduction losses in those states. In this perspective the conduction, switching and blocking (or reverse leakage) are main contributors to these losses in a power semiconductor. In our cases for design perception these losses are snubbed. In this methodology, the electrolytic capacitors and power switches are the two most delicate and insubstantial constituents which are considered prone to wear-out failure. This aspect will be given due attention in design methodology. The component mechanical strength, pragmatic electrical load, temperature variations, control and switching techniques etc. are few aspects which dictate the reliability of these constituents. In utmost result, these features may result in degradation of component materials in long-term operation. Since the converter device failure rate is dictated by the

aging of components, therefore such components ought to be substituted according to a well formulated maintenance strategy. Figure 4.1 depicts IGBT circuit diagram symbol, whereas the Figure 4.2 deliberates simplified equivalent circuit [187]. In the IGBT, the losses are divided into four regions. First region is the

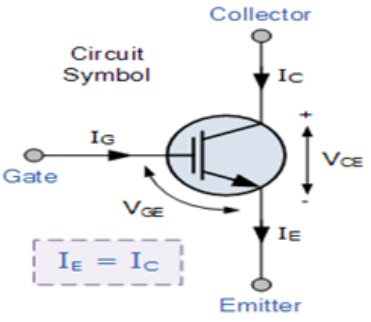


FIGURE 4.1: IGBT circuit diagram Symbol

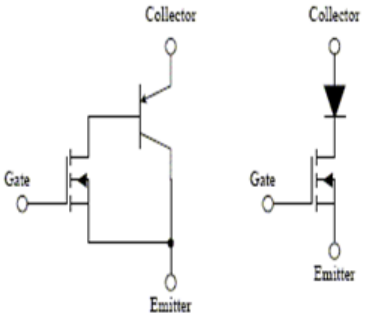


FIGURE 4.2: IGBT Simplified Equivalent Circuit

on-state power loss. It occurs when the IGBT is on. There is therefore a voltage drop across the IGBT. Second, the power loss appears due to the leakage current in the reverse mode. It can be considered insignificant because the leakage current is very small. Third and fourth regions show the switching losses. These losses take place once the IGBT turns on or off. In these two latter cases, the voltage or current of the IGBT cannot instantaneously become zero. The switching losses happen therefore in these cases.

4.3 Mathematical Modeling of Inverter

Methodical model is a paramount instrument for estimation of dynamic performance and stability limits using diverse structure considerations. Mathematical model of the inverter should be established before undertaking the design aspect. The IGBT with reverse diode, in accordance with the Thevenin theorem, are represented by a voltage source. This allows using a fixed equivalent circuit for open and closed states of the transistor.

4.3.1 Single Phase Half Bridge Inverter

A half bridge inverter in a single phase perspective is considered to be one of the easiest, simplest and modest inverters(dc-ac converter), comprised of a DC

Voltage source, two electrolytic (polar) capacitors, two power switches, two diodes and the load as depicted in Figure 4.3. Figure 4.4 highlights the output load voltage waveforms, where the output voltage is given as, $\mathbf{V}_0 = \frac{V_{in}}{2}$

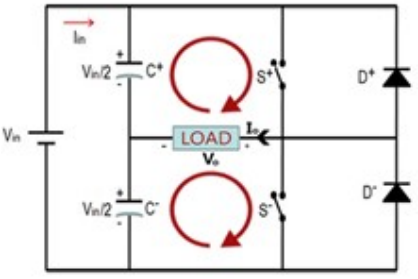


FIGURE 4.3: Single-Phase Half-Bridge Inverter

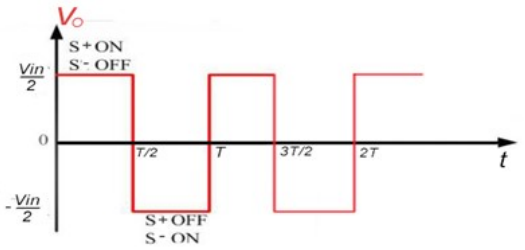


FIGURE 4.4: Output load Voltage Waveform

In operational analysis, during a switching time period (T), the switches S+ and S- are switched on and off successively being conducted for a half cycle (i.e. 180 degrees). During first instance, when the upper switch S^+ is ON, and the lower switch S^- is OFF, then the load voltage V_o across the load is $V_{in}/\mathbf{2}$. Nevertheless, when upper switch S^+ is OFF, but lower switch S^- is ON, the load voltage V_o equals to $V_{in}/\mathbf{2}$. As per principle, for the pure resistive load, the load current $\mathbf{I}_o$ will have the same waveform and phase as attained by the output voltage $\mathbf{V}_o$. The switches S^+ and S^- are considered to be the self-commutating switches. The switch S^+ will conduct when the input voltage is positive and current is negative, whereas, the switch S^- will conduct when the input voltage is negative, and the current is positive. On the same analogy, the diode D^+ will operate when the input dc voltage is positive and current is negative, diode D^- will operate when the input dc voltage is negative, and subsequently the current is positive. In practice, a **dead time** between ON and OFF (t_d) for S^+ & S^- is required to circumvent /avoid short circuit or "shoot-through" faults. This ultimately leads to produce and yield to a quasi-square wave output load voltage. For the resistive load, the output current waveform will be a replica of the voltage waveform as presented in Fig-4.3. For any sort of Load, the output Voltage waveform will remain the same, however the current waveform entirely depend on kind of the load. The two large power capacitors are inserted for provision of a neutral point N, in such a fashion that each capacitor conserves and maintains a fixed voltage

$\mathbf{V}_{in}\mathbf{/2}$. As it has been visualized that the injection of current harmonics by the operation of the inverter is considered to be of a low order harmonics that is why it necessitates for insertion a set of large power capacitors (i.e. C^+ and C^-).

- **Case-1 (*When the switch S^+ is ON and the switch S^- is OFF*):** When the switch S^+ is ON and operative for a time period from **0** to $\mathbf{T/2}$, the diodes D^+ and D^- are in reverse bias condition and the switch S^- is OFF.

  With the application of Kirchhoff's Voltage Law (KVL)

$$\frac{V_{in}}{2} - V_o = 0$$

$$\text{Therefore} \qquad V_o = \frac{V_{in}}{2} \tag{4.1}$$

  Using Ohm's to determine the output current

$$I_o = \frac{V_o}{R} = \frac{V_{in}}{2R} \tag{4.2}$$

  Where R stands for resistive load.

- **Case-2 (*When switch S^- is ON and the switch S^- is OFF*):** When switch S- is ON and operative for a time period from **0** to T/2, the diode D^+ and D^- will be in reverse bias condition and S^+ switch will be OFF.

  By the application of Kirchhoff's Voltage Law (KVL)

$$\frac{V_{in}}{2} + V_o = 0$$

$$\text{Therefore} \qquad V_o = -\frac{V_{in}}{2} \tag{4.3}$$

  Using Ohm's to determine the output current,

$$I_o = \frac{V_o}{R} = -\frac{V_{in}}{2R} \tag{4.4}$$

  Where R stands for resistive load.

Table-4.1 exhibits the switching states of a single-phase half-bridge inverter.

TABLE 4.1: Switching States

$\mathbf{S}^+$	$\mathbf{S}^+$	$\mathbf{V}_0$
ON	OFF	$+V_{in}/2$
OFF	ON	$-V_{in}/2$

It is evident from the Table 4.1, when the switch S^+ is ON (i.e. conductive) during positive half cycle of the output voltage, the output voltage will become, $\mathbf{V}_o = \mathbf{V}_{in}/\mathbf{2}$ and similarly when the switch S^- is ON (i.e. operational) for negative half cycle, the output voltage becomes, $\mathbf{V}_o = -\mathbf{V}_{in}/\mathbf{2}$. As a principle, both the switches should conduct alternatively otherwise there might be a chance of short circuiting and ultimately will result in failure of the circuit. Moreover, for the resistive load, the current waveform follows the voltage waveform, whereas in case of reactive load it is not the same. For reactive load, the feedback diodes operate and conduct when the voltage and current are of opposite polarities.

4.3.2 Three Phase Inverter (Formed by Three Single Phase Inverters):

A three phase bridge inverter is deliberated as a structure / scheme which convert DC power input into equivalent three phase AC output power. As per analogy of single phase inverter, this three phase inverter is also provided with the DC input supply from a source or from a rectifier. This three phase structure can be established by connecting three single phase half bridge inverters in parallel. In this arrangement, the configuration is termed as a three phase inverter designed by three single phase inverters. A careful and vigilant reflection of this arrangement divulges that this power circuit fabricated from a three phase bridge inverter is equivalent to three half bridge inverters structured side by side. This arrangement requires six switches and six diodes as shown in figure 4.5. As per practice there are mainly two promising types of patterns for gating the switch. In one of the patterns, each switch conducts/operates for 180 degrees, whereas in other pattern, each switch conducts/operates for 120 degrees. However, in both these conductions, the gating signals are applied at 60 degrees interval of the output load

voltage waveform. Three-phase counterparts/equivalents of the single-phase half bridge inverters are explained in Figures 4.5. Single-phase voltage source inverters cover low-range applications, whereas the medium to high power applications are performed by three-phase voltage source inverters. The prime and foremost aim of establishing these configurations is to deliver a three-phase voltage source with the fixed amplitude of the voltages. Inverter output voltage is considered to be of a discrete waveform, comprising of harmonics, which are not usually anticipated in modeling. For each phase in this arrangement, the procedure of mathematical modeling used for half bridge inverter in a single phase is same for rest of the phases in the inverter, which is deliberated subsequently. It is worth mentioning that all phases of the inverter are 120 degree out of phase.

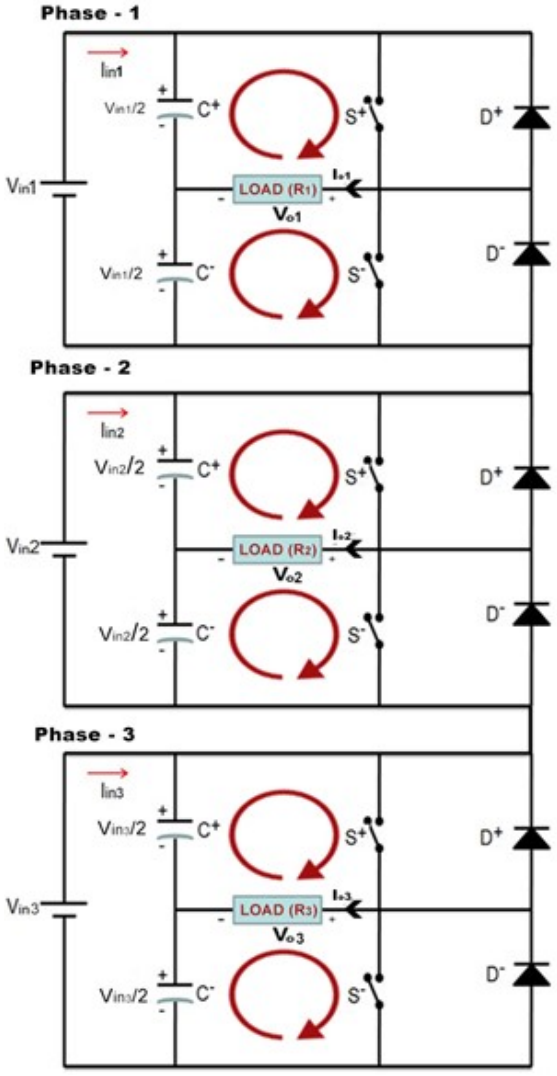


FIGURE 4.5: Three-phase half-bridge inverter formed by three single phase inverters

- **For Phase-1**

  For Phase-1, if output voltage is represented by V_{01}, input voltage by V_{in1} , load resistance by R1 and output current by I_{01}, then as per analogy of single phase half bridge inverter, various relationships is given below:

  For positive half cycle (i.e. switch S^+ is conducting)

$$V_{01} = \frac{V_{in1}}{2} \tag{4.5}$$

$$I_{01} = \frac{V_{01}}{R_1} = \frac{V_{in1}}{2R_1} \tag{4.6}$$

  Similarly for negative half cycle (i.e. switch S^- is conducting)

$$V_{01} = -\frac{V_{in1}}{2} \tag{4.7}$$

$$I_{01} = -\frac{V_{01}}{R_1} = -\frac{V_{in1}}{2R_1} \tag{4.8}$$

  In relation to other two phases, the output voltage with phase difference will be as $\mathbf{V}_{01} < 0^0$.

- **For Phase-2**

  For Phase-2, if output voltage is represented by V_{02}, input voltage by V_{in2} , load resistance by R_2 and output current by I_{02}, then as per analogy of single phase half bridge inverter, various relationships are given below:

  For positive half cycle (i.e. switch S^+ is conducting)

$$V_{02} = \frac{V_{in2}}{2} \tag{4.9}$$

$$I_{02} = \frac{V_{02}}{R_2} = \frac{V_{in2}}{2R_2} \tag{4.10}$$

  Similarly for negative half cycle (i.e. switch S^- is conducting)

$$V_{02} = -\frac{V_{in2}}{2} \tag{4.11}$$

$$I_{02} = -\frac{V_{02}}{R_2} = -\frac{V_{in2}}{2R_2} \tag{4.12}$$

In relation to other two phases, the output voltage with phase difference will be as $\mathbf{V}_{02} < 120^0$

- **For Phase-3**

  Similarly for Phase-3, if output voltage is represented by V_{03}, input voltage by V_{in3} , load resistance by R_3 and output current by I_{03}, then various relationships are:

  For positive half cycle

$$V_{03} = \frac{V_{in3}}{2} \tag{4.13}$$

$$I_{03} = \frac{V_{03}}{R_3} = \frac{V_{in3}}{2R_3} \tag{4.14}$$

  Likewise, for negative half cycle

$$V_{03} = -\frac{V_{in3}}{2} \tag{4.15}$$

$$I_{03} = -\frac{V_{03}}{R_3} = -\frac{V_{in3}}{2R_3} \tag{4.16}$$

  In relation to other two phases, the output voltage with phase difference will be as $\mathbf{V}_{03} < 240^0$

Based on the modeling of the single phase inverter in half bridge topology, this modeling also offers a standard and unified modeling approach for DC-AC converters.

4.4 Analysis of Inverter

Primarily, a single-phase square wave half bridge inverter yields a squared shaped output voltage for a single-phase load. This arrangement possesses very simple and easy control logic. Power switches involved in design are required to function at much lower frequencies as compared to the other classifications of the inverters power switches [188]. As per history, the first generation of the power inverters

with thyristor switches, were essentially considered as square wave inverters. This is because of the reason that the thyristor switches can be turned ON and turned OFF for duration of only a few hundred times in a second [189]. Whereas, the practical switches like IGBTs etc., are taken much faster and can be used at switching frequencies of several kilohertz. Fig 4.6 illustrates a single-phase inverter in half bridge topology perspective, which is taken for further deliberation:

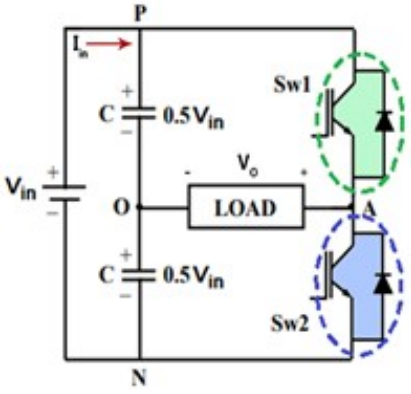


FIGURE 4.6: Single phase half bridge inverter

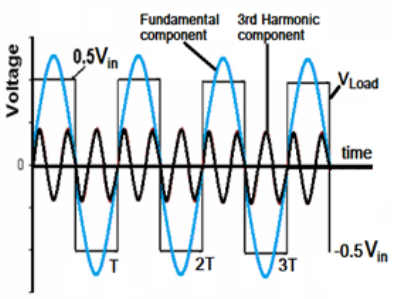


FIGURE 4.7: Square wave load voltage Output by half bridge inverter

This Single phase half bridge inverter topology is being evaluated in the supposition of ideal circuit environments. Consequently, it is also anticipated that the supply dc voltage (V_{in}) is fixed and the switches are perfectly lossless. In operation of half bridge inverter, the supply dc voltage is divided into two equal parts through loss-less potential divider constituted by capacitors. Furthermore, this topology comprises of one leg (one pole) of the switches. Each of these switches encompasses an IGBT switch across which a diode is placed in anti-parallel fashion. These switches also possess the capability of operating/conducting bi-directional current; however, there is requirement of blocking of only one voltage polarity. The intersection point of the switches in each pole will act as a one output point for the load. It can be visualized from Fig 4.6, that the single-phase load is connected between the mid-point of the input dc supply (i.e. intersection point of the capacitors) and the intersection point of the two switches, which are labeled as 'O' and 'A' correspondingly.

To comprehend the phenomenon in a befitting manner, the switches (i.e. Sw1 and Sw2) are taken to be controlled mechanical switches, which operate as per

response of the control signal of the switch. If these switches are made operational alternately, with duty ratio of each switch kept equal to 0.5, such arrangement will yield the load voltage (V_0) of a square wave shape with a peak magnitude equal to the half of the input voltage ($V_{in}/2$). Fig.4.7 illustrates a characteristic load voltage waveform output of half bridge inverter. The load voltage (V_{AO}) attains a magnitude of $+0.5V_{in}$, when Sw1 is turned on, whereas, on turning ON the sw2, the magnitude reverses to -0.5 V_{in}. As a principle, for a universal load, the switches should not be operated simultaneously, because such simultaneous conduction of both the switches will ultimately lead to a short circuit across the dc bus, which will result in rapid rise of switch currents. In case of application of inductive load, one of the switches must conduct on permanent basis in order to maintain the continuity of load current and make sure that the load current should not change abruptly in spite of very high switching frequency.

4.4.1 Harmonic Analysis

In this subsection, the harmonic analysis of output load voltage and load current waveforms pertaining to single phase half bridge inverter is undertaken. The load voltage waveform presented in Figure.4.7 can be mathematically expressed in terms of its Fourier's components as:

$$V_{A)} = V_o = \sum n = 1, 3, 5, 7, ..., \infty \frac{2V_{in}}{n\pi} sin(nwt) \tag{4.17}$$

Where 'n' indicates the harmonic order and $\omega/2\pi$ stands for frequency (f) of the square wave, measured in hertz. In certain cases, 'f' also represents the inverter switching frequency (f_{sw}). Equation-(4.35) clearly depicts that the square wave inverter load voltage contains only the odd harmonics whose magnitudes are inversely proportional to their harmonic order. Therefore, $\mathbf{2}/\pi\ \mathbf{V}_{in}$ is taken as the peak amplitude of the fundamental frequency component and $\mathbf{2}/\mathbf{n}\pi\ \mathbf{V}_{in}$ is taken as the peak magnitude of the nth harmonic voltage (n being odd integer). In power applications, the fundamental component of load voltage is hardly of any practical/experimental use and the rest of other higher order harmonics are considered to be unwanted distortions. In power electronics, majority of the practical

loads is deliberated to be inductive with intrinsic low pass filter (LPF) type. Execution of such practice reveals that the inductive load current waveforms possess fewer higher order harmonic distortions in contrast to the corresponding distortion observed in the square-wave voltage waveform. In order to investigate and elaborate this fact, a time domain exploration of the load current for R load is being presented subsequently.

4.4.2 Time Domain Exploration of Load Current

In this sub-section, a time domain exploration of the load current waveform (for Resistance Load R) in steady state environment is undertaken and elaborated. In a steady state environment, the load current waveform repeats in consecutive cycles, therefore here, only one square wave time period has been considered. Let time t=0, be the time when the square wave positive half cycle commences and similarly, I0 be the load current observed at this particular instant. Correspondingly, at t=0.5T, be the instant, the square wave negative half cycle commences, which ranges till t= T. In this context, the effective circuit equation for the voltage positive half cycle can be given as:

$$R_i = 0.5V_{in}, \qquad for \quad 0 < t < 0.5T \tag{4.18}$$

Similarly the equation for the negative half cycle can be written as

$$R_i = -0.5V_{in}, \qquad for \quad 0.5T < t < T \tag{4.19}$$

, where T (=1/f) is the time period of the square wave.

The instantaneous current 'i' during the first half of square wave may be obtained by solving Eqn (4.15).

$$\text{Accordingly}, i(t) = \frac{0.5V_{in}}{R} \qquad for \quad 0 < t < 0.5T \tag{4.20}$$

The current at the end of the positive half cycle becomes the starting current for the negative half cycle.

The circuit equation for the next half cycle may now be written as:

$$i(t) = -\frac{0.5V_{in}}{R} \qquad for \quad 0.5T < t < T \tag{4.21}$$

The evaluation of the magnitude of the various harmonic components of load current waveform is being reflected subsequently, while considering the analysis of frequency domain.

4.4.3 Voltage and Current Ratings of Inverter Switches

In this sub-section, the voltage rating and current rating of switches are deliberated briefly. The operation of switches in each leg/arm is performed in a complementary fashion, i.e. once the upper switch of a leg is ON (i.e. operative), the lower switch of the same leg will be OFF (i.e. in-operative) and vice versa. This inoperative condition will result in blocking of the complete dc bus voltage. In such circumstances, it will not be unjustified to say that switches must be rated/valued based on the capability of blocking even the worst-case instantaneous magnitude of dc bus voltage. In practical scenario, the inverter switch voltage rating is weighed to be legitimately higher as compared to the worst-case dc voltage, for the reason of accountability for production of stray voltages appeared across stray inductances and diode turn-on transient voltage etc.

It has been experienced that for a well-established inverter structure, approximately 50% margin is considered to be the prime switch voltage rating over dc-bus voltage. Operationally, during half of the current cycle, load current is carried by each switch of the inverter, therefore basing on this action; the rating of the switches must be carried out on the capability for withstanding the peak magnitude of instantaneous load current. Due to limitation of the nature of switches structure (i.e. very small thermal time constant), their withstanding capability against the overheating effect is not extended for more than a few milliseconds. Since the inverter switch module is comprised of a diode and controlled switch, therefore the division of current between the controlled switch and diode will be established on the aspect of the load power factor taken at operating frequency. In a broader practical scenario, the controlled switch and diode should be rated and valued on the aspect of the carriage of peak load current.

4.5 Inverter Designing

Designing of small size, low weight inverters is attributable to the combination of SST and sophisticated power electronics. In wake of design methodology, this section focuses on designing a PWM inverter in a half bridge configuration in SST applications. This scheming of inverter definitely establishes a platform for learning power conversion concepts and the differences in input and output circuits. First of all, let us deliberate on specification and design parameters in the subsequent segments.

4.5.1 Design Specification & Parameters

Based on the derived formulae and practical deliberations, the design of a 15KV high frequency PWM inverter in half bridge topology perspective is anticipated. The generated data supporting the design is given in Tables 4.2.

TABLE 4.2: DC-AC Converter (Inverter) Design Calculations

Parameter	Symbol	Value	Remarks
INPUT (Data to be given)			
Inverter input DC voltage	$V_{DC} = V_{in}$	15KV	-
Rated Power	Prated	100KVA	-
Output Voltage of inverter (Phase to Neutral)	V_{ph}	2.50KV	
Output Voltage of inverter (Line to Line)	V_{L-L}	4082.43KV $\approx$ 4KV	$V_{LL} = 2V_p\sqrt{\frac{2}{3}}$
Peak Voltage of each phase (VAC)	Vp	2.5KV	
Operating frequency	f_0	25KHz	
Switching frequency	f_{sw}	50kHz	
Transformer Turn ratio (K)	N_1/N_2	7:1	
Load Resistance (R_L)	R_L	Static Load	-
Nominal switch time period	D	50% (180 degree conduction)	
HV Switching Device	Silicon IGBT (proposed)	6.5KV	
Diode	Silicon Diode (Proposed)	6.5KV	
Input Capacitors	Electrolytic or Polymer film capacitor (proposed)	3KV	

4.5.2 Proposed Inverter Design and Description

In this sub section, the designing of proposed inverter is deliberated. Firstly a pictorial designing of a single phase half bridge inverter comprised of two switches,

two capacitors and a single supply voltage. is depicted in Figure. 4.8. From the figure, it is evident that the two capacitors act as voltage divider which divides the input voltage into two equal halves. The action of switches in a phase is complementary to each other (i.e. one switch is conducting, the other will be off). At any specified time, both the switches in the same phase, would never be conductive, otherwise this situation will lead to the short circuiting of the supply voltage and ultimately result in failure of the entire setup. Therefore, such situation should be circumvented at all times.

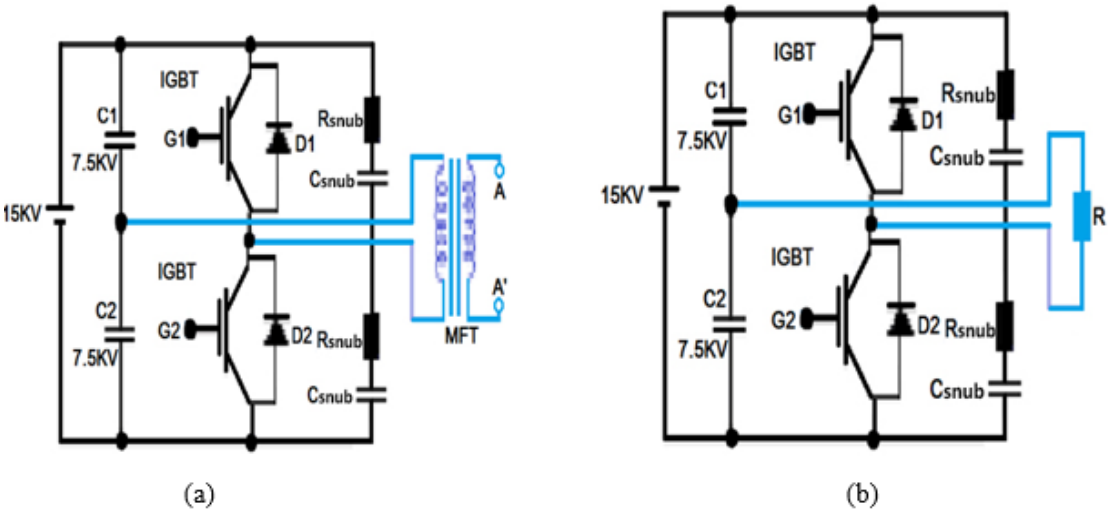


FIGURE 4.8: (a), (b) Single Phase half bridge inverter Design

Fig. 4.9 shows the synoptic of the driving electronics for the implementation of conversion of the dc voltage into square wave AC voltage. Three phase power inverter consisting of three single phase inverter, connected / linked in parallel is shown. For extracting three phase stable and balanced (fundamental) voltages, the gating signals of single-phase inverters are established advanced / delayed by an angle of 120 degrees with respect to each other depending upon the cycle/phase of operation. In this arrangement, the transformer primary windings have been made isolated from each other, whereas the secondary winding might be arranged in either star or delta configuration. The transformer secondary is commonly connected in wye arrangement in order to eradicate harmonics appearing at the output voltages. Input AC voltage of 15 KV is provided to this three phase inverter. Every phase consists of two capacitors of 2.5KV each with two IGBTs switch modules. In accordance with output frequency, ON time and OFF time of IGBT is established; thereby gate pulses are produced. The switch-1(IGBT-1)

is activated/triggered for first half cycle and during this time period; the switch-2(IGBT-2) is not activated. During this phenomenon, half cycle of AC square wave output voltage is accomplished and load voltage equals to $2.5KV$. Similarly in second half cycle, the switch-2(IGBT-2) is triggered and lower DC voltage source is connected with the load. On completion of this second half cycle of AC square wave output, the load voltage equals to $-2.5KV$. Such process is repeated and persistent for other two phases of the circuit.

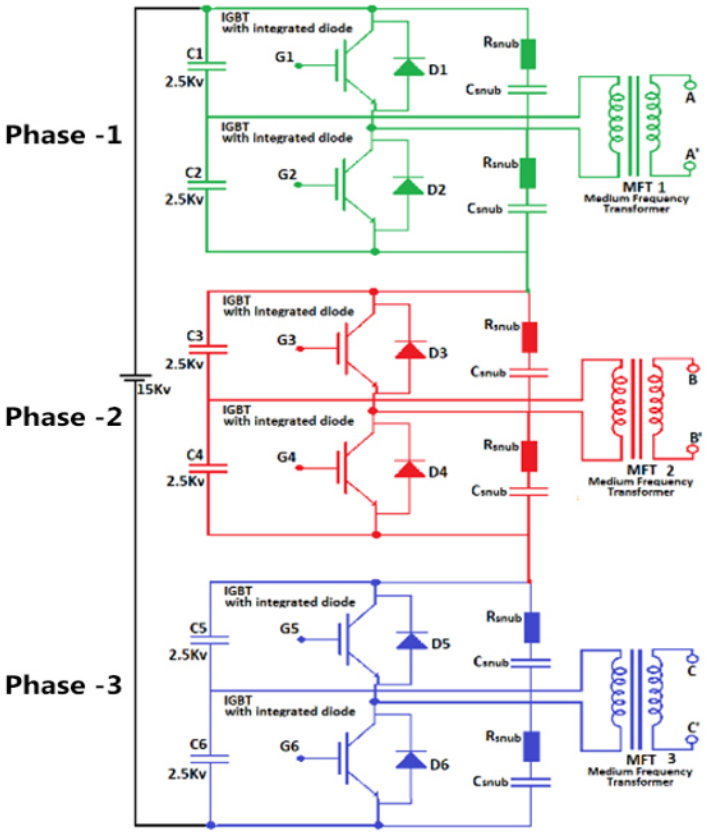


FIGURE 4.9: Propose Inverter Design

In this model an effort is made to establish a three phase high frequency DC-AC converter in SST application. This design is constructed with help of combinations of three single-phase parallel inverters connected in parallel using IGBTs switches. The advantages of this design include light weight, small size, small standby power and high efficiency. The simulation results will be carried out by MATLAB/ Simulink. However, at this stage, the mathematical evaluations of different parameters of the proposed inverter have been undertaken in the subsequent section in tabulated form.

4.6 Mathematical Evaluation of the Proposed Inverter Design

The proposed inverter have been undertaken in the subsequent section in tabulated form. In this section, the proposed design is being evaluated numerically with help of the deduced relationship of various parameters and formulae. As the design is primarily consists of three phases formed by three single phases, therefore the mathematical evaluation of one phase will also be the same and persistent for the rest of two phases.

4.6.1 Single Phase Inverter with 15kV DC Supply Voltage

Using the parameters value given in Table 4.2, Table 4.3 deliberates the mathematical evaluation of the design in a single Phase Half Bridge perspective with 15kV DC input.

TABLE 4.3: Proposed Design with 15kV DC input Single Phase Half Bridge

Parameters	**Formulae**	**Calculated Values**	**Outcome**
RMS output voltage(V_0)	$V_o = (\frac{2}{T_o}\int_o^{T_{o/2}} \frac{Vin^2}{4}dt)^{\frac{1}{2}} = \frac{V_{in}}{2}$	$\frac{15000}{2} = 7500V$	7500 Volts
RMS output voltage at the fundamental frequency (V_{0F})	$V_{0F} = \frac{2V_s}{\sqrt{2}\times\pi} = 0.45V_{in}$	$0.45x15000 = 6750V$	6750 Volts
Peak Transistor (IGBT) Current at 1000 ohms load	$I_p = I_{orms} = \frac{V_{peak}}{R_{load}}$	$I_p = \frac{7500}{1000} = 7.5A$	7.5 Amperes
Average (IGBT) Current at 1000 ohm load at 50% duty cycle.	$I_{av(Q)} = Duty\ cycle \times I_p$	$I_{av(Q)=0.5\times7.5=3.75A}$	3.75 Amperes
The peak reverse blocking voltage (VBR)	$V_{BR} = V_o$	$V_{BR} = 7500V$	7500 Volts
The output Power (P_0)	$P_o = \frac{vo^2}{R_{(Load)}} = V_o \times I_{orms}$	$P_o = \frac{7500^2}{1000} = 7500x7.5$	56250 Watts
Average Supply Current	I_s	$I_s = 3.75A$	3.75 Amperes
RMS harmonic Voltage(V_h)	$V_h = [Vo^2 - V_{0F}^2]^{1/2}$ or $V_h = 0.2176V_{in}$	$V_h = [7500^2 - 6750^2]^{1/2}$ $V_h = 3269.174208V$	3269.174208 V
Total Harmonic Distortion (THD)	$THD = \frac{V_h}{V_{0F}}$	$THD = \frac{3269.174208}{6750} = 0.4843$	0.4843 = 48.43%
Input Power of the inverter (P_{in})	$P_in = V_{in} \times I_s$	$Pin = 15000 \times 3.75 = 56250W$	56250 W
Inverter Efficiency($\%\eta_{inv}$)	$\%\eta_{inv} = \frac{P_o}{P_{in}} \times 100$	$\eta_{inv} = \frac{56250}{56250} = 1.00 \times 100$	100%

From mathematical evaluation for 15kV dc supply voltage, it is evident that the lossless inverter system delivers the output with the utmost efficiency.

4.6.2 Single Phase Inverter with 5kV DC Supply Voltage

As per section 4.6.1, using same analogy, Table 4.4 deliberates the mathematical evaluation of the design in a single Phase Half Bridge perspective with 5kV DC input.

TABLE 4.4: Proposed Design with 5kV DC input Single Phase Half Bridge

Parameters	**Formulae**	**Calculated Values**	**Outcome**
RMS output voltage(V_0)	$V_o = (\frac{2}{T_o}\int_o^{T_{o/2}} \frac{Vin^2}{4}dt)^{\frac{1}{2}} = \frac{V_{in}}{2}$	$\frac{5000}{2} = 2500V$	2500 Volts
RMS output voltage at the fundamental frequency (V_{0F})	$V_{0F} = \frac{2V_s}{\sqrt{2}\times\pi} = 0.45V_{in}$	$0.45x5000 = 2250V$	2250 Volts
Peak Transistor (IGBT) Current at 1000 ohms load	$I_p = I_{orms} = \frac{V_{peak}}{R_{load}}$	$I_p = \frac{2500}{1000} = 2.5A$	2.5 Amperes
Average (IGBT) Current at 1000 ohm load at 50% duty cycle.	$I_{av(Q)} = Duty\ cycle \times I_p$	$I_{av(Q)=0.5\times2.5=1.25A}$	1.25 Amperes
The peak reverse blocking voltage (VBR)	$V_{BR} = V_o$	$V_{BR} = 2500V$	2500 Volts
The output Power (P_0)	$P_o = \frac{vo^2}{R_{(Load)}} = V_o \times I_{orms}$	$P_o = \frac{2500^2}{1000} = 2500 \times 2.5$	6250 Watts
Average Supply Current	I_s	$I_s = 1.25A$	1.25 Amperes
RMS harmonic Voltage(V_h)	$V_h = [Vo^2 - V_{0F}^2]^{1/2}$ or $V_h = 0.2176V_{in}$	$V_h = [2500^2 - 2250^2]^{1/2}$ $V_h = 1089.724738V$	1089.73 Volts
Total Harmonic Distortion (THD)	$THD = \frac{V_h}{V_{0F}}$	$THD = \frac{1089.73}{2250} = 0.4843$	0.4843 = 48.43%
Input Power of the inverter (P_{in})	$P_in = V_{in} \times I_s$	$Pin = 5000 \times 1.25 = 6250W$	6250 W
Inverter Efficiency($\%\eta_{inv}$)	$\%\eta_{inv} = \frac{P_o}{P_{in}} \times 100$	$\eta_{inv} = \frac{6250}{6250} = 1.00 \times 100$	100%

From mathematical valuation for 5kV dc input voltage, it is apparent that the lossless inverter system in single phase half bridge perspective provides the output with the utmost efficiency.

4.6.3 Proposed Three Phase Half Bridge Inverter

Using the parameters value given in Table 4.2, Table-4.5 deliberates the mathematical evaluation of the design in a Three Phase Inverter formed of three single phase half bridge inverter.

TABLE 4.5: Mathematical Evaluation of the inverter design (5kV Three Phase Half Bridge)

Parameters	**Formulae**	**Calculated Values**	**Outcome**
	(Resistive Load = 1000 ohms)		
RMS output voltage at each Phase (V_0)	$V_o = (\frac{2}{T_o}\int_o^{T_{o/2}} \frac{Vin^2}{4}dt)^{\frac{1}{2}} = \frac{V_{in}}{2}$	$\frac{5000}{2} = 2500V$	2500 Volts
RMS output current at each Phase($I_0 = I_{ph}$)	$I_{ph} = \frac{V_{in}}{2R_L} = \frac{V_{ph}}{R_L}$	$\frac{5000}{2\times1000}$	2.5 Amperes
RMS output voltage at the fundamental frequency (V_{0F})	$V_{0F} = \frac{2V_s}{\sqrt{2}\times\pi} = 0.45V_{in}$	$0.45x5000 = 2250V$	2250 Volts
Line to Line rms Voltage (V_{L1})	$V_{LL} = 2V_p\sqrt{\frac{2}{3}}$	$V_{LL} = 2\times2.5K\times\sqrt{\frac{2}{3}}$ OR $V_{LL} = 0.8165\times5000$	4082.48 V
RMS fundamental line Voltage (V_{L1})	$V_{L1} = 4V_{in}\frac{sin60}{\sqrt{2}\pi} = 0.7797v_{in}$	$V_{L1} = 0.7797\times5000 = 3898.5V$	3898.5V
RMS fundamental Phase Voltage (V_{Ph1})	$V_{ph1} = \frac{V_{L1}}{\sqrt{3}} = \frac{3898.5}{\sqrt{3}}$	$V_{ph} = \frac{3898.5}{\sqrt{3}} = 2250.80V = V_o$	2250.80 V
RMS harmonic Voltage(V_h)	$V_h = [V_L^2 - V_{L1}^2]^{1/2}$ or $V_h = 0.24236V_{in}$	$V_h = [4082.48^2 - 3898.5^2]^{1/2}$ $V_h = 1211.751088V$	1211.75 Volts
THD	$THD = \frac{V_h}{V_{L1}}$	$THD = \frac{1211.75}{3898.5} = 0.4843$	$0.3108 = 31.08\%$
The load Power (P_o)	$P_o = 3V_{ph}I_{ph}$	$P_o = 3\times500\times2.5$	18750 Watts
Avg Supply Current (I_s)	$I_s = I_{ph}$	2.5 A	2.5 Amperes
RMS Load Current (I_0)	$I_0 = I_{ph}$	2.5 A	2.5 Amperes
Average (IGBT) Current	$I_{av(Q)=\frac{I_{ph}}{2}}$	1.25	1.25 Amperes
Input Power (P_{in})	$P_{in} = 3\times V_{in}/2\times I_{ph}$	$3\times\frac{5000}{2}.5$	18750 Watts
Inverter Efficiency	$\%\eta_{inv} = \frac{P_0}{P_{in}}\times100$	$\eta_{inv} = \frac{18750}{18750} = 1.00*100$	100%
RMS (IGBT) Current	$I_{Qrms} = I_{ph}$	$I_{Qrms} = 2.5A$	2.5 Amperes

In mathematical evaluation of proposed inverter system design in single phase as well as three phase perspective, the output is delivered with the utmost efficiency, without any dissipation.

4.7 Performance Evaluation Of Inverters

Normally, an inverter is analyzed operationally based on the aspects such as: (1) Efficiency and (2) Total Harmonic Distortion (THD). Based on the standard formulae and practical considerations, the calculation of the performance parameter related to efficiency and Total harmonic distortion (THD) is shown in Table-4.6. For efficiency calculation, Figure 4.8 is used for efficiency measurement with a resistive load of 500 ohms.

TABLE 4.6: Mathematical Calculation of Performance Parameters of Inverter

Parameter	**Value**	**Calculation**
Inverter Efficiency	100%	Efficiency, $\eta = \frac{P_0}{P_{in}}$ • $P_{in} = 15000 \times 7.5 = 112500W$ • $P_0 = 7500 \times \frac{7500}{500} = 112500W$ • $Efficiency, \eta = \frac{P_0}{P_{in}} = \frac{112500}{112500} = 1 = 100\%$
THD	48.4%	$THD = \frac{1}{V_{0F}}(\sum_{n=3,5,7}^{\infty} V_o^2 n^2)$ $V_{0F} = V_{1rms} = \frac{2V_s}{\sqrt{2}\pi}$ • **For $\mathbf{V}_s$ = 15kV** $V_{0F} = \frac{2(1500)}{\sqrt{2}\pi}$ $V_{0F} = \frac{30000}{4.443} = 6752.195$ $V_h = \sqrt{V_o^2 + V_{1rms}^2} = \sqrt{7500^2 - 675.195^2}$ $V_h = \sqrt{10657862.68} = 3264.638$ $THD = \sqrt{\frac{3264.638}{6752.195}} = 0.4843 = 48.43\%$ Similarly, • **For $\mathbf{V}_s$ = 5kV** $V_{0F} = 0.45Vs = 2250V, V_0 = 2500V$ $V_h = [V_0^2 - V_{OF}^2]^{1/2} = 1089.724736V$ $THD = \frac{V_h}{V_{0F}} = 0.4843 = 48.43\%$

4.8 Optimization of the Proposed Design

Power converters have a major influence on the efficiency, reliability, cost, and dynamic performance of the overall system. Efficiency and development/design charges are the two most promising aspects considered in any system; therefore in fabrication scenario, it is very pertinent to be cautious in augmenting the efficiency. Efficiency and development/design charges are the two the most promising aspects considered in any system. In contrast to the reported design methodologies, the design and optimization methodology utilized in this dissertation stands for augmenting the converter efficiency. In the optimization perspective, following constraints are given due deliberations:

- Efficiency Augmentation
- Reduction of cost, volume

- Voltage System Stability under static load
- Delivery of stable output Square wave
- Snubber Circuit Arrangement
- Output Frequency and Voltage Control
- Controlling/Modulation Technique

4.8.1 Efficiency Augmentation

High power density of the inverter infers a very constrained design with reduced/negligible losses. Unless these losses are minimized, the conversion efficiency may not be improved. Therefore, to address this issue, the RC snubber circuit and PWM techniques are being adopted. However, the cost calculation of the system must be kept in mind in order to be maintained at a reasonable level. Efficiency augmentation is one of the foremost anticipated features of the DC-AC converter. It must be noted that the efficiency of high frequency inverter of an isolated DC-DC converter in solid state transformer applications is a prime importance in wake of the escalating energy cost and its continuous and uninterrupted operation.

4.8.2 Reduction in Expenditure and volume of the Design

One of the key constraints of this design is cost effectiveness. The occurring expenditure of this design topology is lesser as compared to the rest of topologies in particular to Full Bridge configuration. As a comparison, Table 4.7 illustrates the comparison of the half bridge and full bridge topology inverter.

4.8.3 Voltage System Stability

Electric loads play a momentous part in the analysis of the voltage stability of interconnected power systems. In the normal working circumstances, the power system is supposed to be operative and functional, where the acceptable steady voltages in a requisite square wave AC form are maintained at the output of the

TABLE 4.7: Comparison of inverter topology [59]

Parameter	**Half Bridge Topology (p.u.)**	**Full Bridge Topology (p.u.)**
Cost	0.86	1.00
Size	0.91	1.00
No. of Switching Devices	2	4
No. of Driving Signals	2	2
Complexity Factor/Control complexity	0.85	1.00
Switching Power Loss	0.50	1.00
RMS Current through inverter switch for same output	1.414	0.707

system. Nevertheless, during instabilities, system voltage may deviate from the rated values; therefore it is very essential that a stable structure must re-establish and restore its voltages to a steady balance value. Conversely, in case of unstable system, the output voltage may not be restored to an acceptable and conventional steady value, thereby resulting in the gradual decrease of the system voltage. Moreover, this action forces the system into a cascading outage and ultimately leading to voltage failure. Voltage stability mechanism is incorporated with help of static phenomenon. In static load analysis, all the dynamics of connected expedients are snubbed and the system is presumed to be in perfect and flawless stability. In this state, the voltage delivery is correctly meeting the demand and the output voltage is conserved at a steady and stable value.

4.8.4 Snubber Circuit

To discourse the constraints, the foremost parameter is the selection and implementation of the requisite inverter design topology in the arrangement of snubber circuit. There exist a variety of snubbers, but the most practicable and appropriate ones include (1) RC snubber (2) RCD turn-off snubber. Out of these types, the preference is being given to the RC snubber circuit with requisite component values for execution, because this arrangement and their placements across the switches contribute for efficiency improvement. Figure 4.10 and Figure 4.11 illustrate the basic circuit design symbol of RC snubber and RCD turn off snubber respectively.

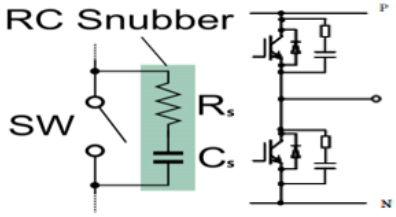


FIGURE 4.10: RC snubber

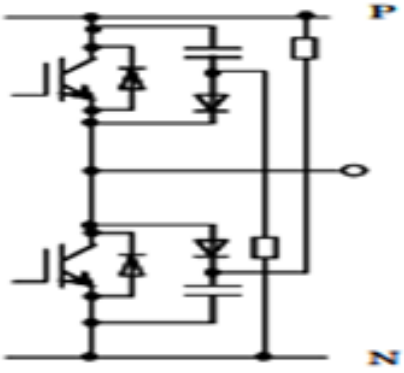


FIGURE 4.11: RCD turn-off snubber

The capacitance value of a snubber capacitor is estimated by following relationship:

$$Cs = \frac{I_L t_f}{V_s} \tag{4.22}$$

Where I_L is the load current,t_f is fall time and V_s is the source voltage or dc supply voltage. The film capacitor as a high frequency capacitor in this operation is highly commended.

By nature the role of snubber resistance is to release the electric charge stored in the snubber capacitor before the next switch turn off event. In order to choose a value of snubber resistor, the discharge time (i.e.$R - sC_s = \tau_s$) in snubber perspective may also be reflected. As per the adequacy of discharge timing, one third of the switching period is preferred (i.e.3R_s C_s=T_s=$\frac{1}{f_s}$)

Therefore the value of snubber resistance is given as:

$$R_s = \frac{1}{3 f_s C_s} \tag{4.23}$$

For selection of snubber diode a number of considerations are kept in mind such like (1) low transient forward voltage (2) short reverse recovery time and (3) soft recovery (4) design of circuit with low inductance wiring etc. These snubber circuits are primarily meant for protection as well as to augment the performance related to the semiconductor devices. Prevention of arcing process is also accomplished by these loss circuits. When a switch is opened unexpectedly, the voltage spikes are generated, which can be suppressed with help of snubber circuit frequently

used in switching power supply. Following are some of the functions, facilitated by snubber circuit in switching mode include [179]:

- Shaping of bipolar switching transistor load line for keeping it in its safe operational region.
- Reduction of voltages and currents during turn-on and turn-off transient situations.
- Elimination of the energy from a switching device as well as dissipating the energy in a resistor in order to reduce the junction temperature.
- Reduction of the ringing for limiting the peak voltage on a switching transistor and thereby lowering their frequency.

As the snubber power loss is the loss that occurs while the IGBT is ON but is independent of the load can be measured/calculated with help of input DC voltage and the input DC current by the relationship, provided the resistive load is taken at infinite ohms value and load current is taken as zero ampere:

$$Snubber\ Loss = I^2 R_(IGBT(ON)) = V_{dc} \times I_{dc}, W \tag{4.24}$$

Experimentally, it is observed that the snubber loss is same (constant) for both light and heavy load. At lighter load, the processed power is lesser whereas the snubber loss is same; hence accordingly at light load the efficiency is lower. Similarly, at heavier load, the processed power is greater and the snubber loss is same, therefore at heavier load the efficiency is greater [180]. The use of snubbers is a very vigorous and robust technique, however, optimum values of the passive components for snubber circuits have to be selected for maintaining balance between the switching losses of the devices and snubber losses to ensure minimum total losses [181].

4.8.5 Output Frequency and Voltage Control

In various power applications, there is a dire need to control the inverter's output (load) voltage and its output frequency. For accomplishment of such requirements,

some mechanism has to be charted out in the inverter conduction perspective. The inverter output frequency can be easily controlled with help of controlling/adjusting the triggering instants of the power switch electronically. The control of the voltage is usually required for provision of stable inverter output voltage and therefore, among the reported and practiced means, the adoption of pulse width modulation (PWM) is the only technique option for regulating and controlling of the voltage within the inverter. By virtue of using such practice, output voltage is controlled and regulated through altering the output voltage pulses duration.

4.8.6 Controlling/Modulation Technique

The adoption of modulation technique for a device depends on the type and nature of device to be controlled, the type of semiconductors, the power to be applied and the modulation algorithm to be executed. The Pulse Width Modulation (PWM) technique merits such as: (1) easy in implementation and control,(2) no environmental disparity/ drifting/degradation in linearity, (3) compatibility with state of art microprocessors,(4) lesser dissipation of power, (5) alloying the linearly regulating of output voltage/current,(6) without any assistance of additional circuitry/components, the output voltage can be controlled and adjusted easily, (7) the adjustment of the output voltage definitely results in obliteration/elimination of lower order harmonics, and (8) the filtering elements are min used for the reason that the higher order harmonics can be filtered calmly.

4.9 Inverter Power Loss

In power systems, the half-bridge structures with two semiconductor switches and anti-parallel diodes are extensively used. The power loss produced by the ideal semiconductor switch is basically the multiplication of voltage and current measured during the function/operation of the semiconductor switch. Once a semiconductor switch is taken to OFF (i.e. nonconductive), then there will be no flow of current through it, in-spite of the presence of the supply voltage. Consequently, there will be no dissipation of power. On contrary, once the switch is ON (i.e. conductive), there is a flow of current through the switch by an amount of supply/input voltage divided by load resistance (V_s/R_L), nevertheless there will be no

voltage drop across it, hence again this will result in no power loss. Here, it is also appraised that in the ideality perspective, the current rise and fall time is zero. During switching the power loss is assumed to be zero. Contrasting to a switch (with ideal parameters), in a real and tangible switch, the complete losses may be enumerated by the conduction loss, the switching loss and the off-state loss. The power loss in off-state can be neglected /mistreated, owing to the situation that the leakage current in off-state is to be negligible as well as insignificant. In case of an inverter using IGBT, the losses are largely generated by IGBTs and the diodes. For resistive loads, the diodes across the transistors have no function/role.

4.9.1 Switching Loss

The switching loss occurs when there is transition takes place in a semiconductor device from the blocking (off) state to the conducting (on) state and vice-versa. The prevailing transition pause/interval is described and considered by a momentous voltage across its terminals and a substantial current flow through it. To gauge the loss due to switching operation, the dissipated energy recorded in each transition has to be multiplied by the frequency. In case of IGBTs, the switching loss fundamentally comprises of the turn-on loss and turn-off loss. In case of diodes, such loss is comprised of the turn-on loss as well as the reverse-recovery loss. The diode turn-on loss is often ignored in operation, for the reason that such loss is considerably lesser as compared to the reverse-recovery loss. Figure 4.12 depicts the losses of a single IGBT switch. It is visualized that whenever a change in a state of the switch occurs, a time delay will take place after the command signal till the time the change is completed. Switching losses are generated during these delay periods. These switching losses are the main source of device loss, which are momentously and significantly dependent on the switching frequency. For the duration of the transition interval, both the quantities (i.e. the current through and the voltage across the device) are substantively larger than zero, which ultimately leads to excessive instantaneous power loss [178].

In case of inverters which generate the output voltage in rectangular waveform, there is a direct relationship between the switching and the frequency of output

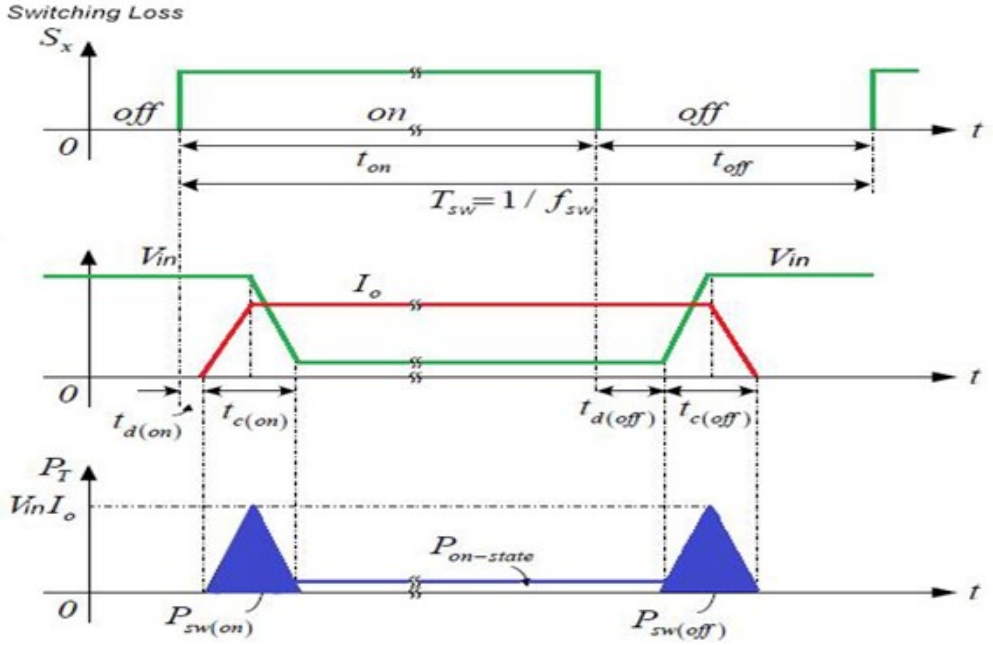


FIGURE 4.12: Losses of an IGBT [178]

voltage. In the prevailing situation, the output voltage frequency is taken to be same as the IGBTs switching frequency. In PWM technique, the inverter aggregate switching losses do not virtually depend on the output voltage frequency but rather depend directly on the switching frequency. This switching frequency ought to be much higher than the output voltage frequency [**?**]. To estimate the switching loss for an IGBT, ensuing equation is followed:

$$P_{SW(IGBT)=(E_{ON}+E_{OFF})\times f_{sw}} \tag{4.25}$$

4.9.2 Conduction Loss

Conduction loss is the one that takes place when the IGBT is in conduction state, where flow of current takes place. During the state of conduction, the cumulative power dissipation can be figured out by taking the product of the on-state voltage and the on-state current. In order to obtain average power dissipation during PWM applications, the conduction loss is required to be multiplied by the duty factor [190]. Therefore, the average conduction loss dissipated by IGBT is given by the following equation.

$$P_{cond(IGBT)} = \frac{1}{T}\int_0^T [V_{CE}(t) * I_{CE}(t)]dt \tag{4.26}$$

In order to substitute the values of the parameters taking from the concerned datasheet in the above equation; there is a requirement to linearize the equation to a more common on-state loss equation applicable for other numerous semiconductor devices.

$$P_{cond(IGBT)} = V_{CEO} * i + R_0 * i^2 \tag{4.27}$$

Where V_{CEO} is On-state voltage threshold voltage, temperature dependent and R0 is the On-state resistance, temperature dependent. R_0 can be calculated as:

$$R_0 = \frac{V_{CEO} - V_{CE1}}{I_{C2} - I_{C1}} \tag{4.28}$$

4.9.3 Total Loss

By determining the switching, conduction and snubber losses, it is possible to obtain reasonable characterizations of the system's efficiency, thermal load and most importantly the junction temperature of the devices. As freewheeling diode does not conduct for resistive load, therefore diode losses are not taken into considerations. The total power loss model of an IGBT semiconductor can be accumulated by the following relationship.

$$P_{loss(IGBT)} = P_{cond(IGBT)+P_{sw(IGBT)}+P_{snubber}} \tag{4.29}$$

4.9.4 Analytical Loss Calculation

In this subsection, an effort is made to evaluate analytically the switching and conduction losses of IGBT. For this purpose the data, parameters and rating appear with data sheet of IGBT type 5SNA 1200E330100 of ABB HiPak-family have been used. Since IGBTs have similar data sheets, therefore this data is applicable to all IGBTs. Table-4.8 highlights the requisite parameters values retrieved from data sheet as well as from design loss calculation and Table-4.9 deliberates tabulated loss calculations relating to switching losses as well as conduction losses.

TABLE 4.8: Loss Calculation Parameters

Parameter	**Symbol**	**Condition**	**Value**	**Unit**
Collector Emitter Voltages	V_{CES}	$V_{GE} = 0V, T_{vj} \geq 25^oC$	3300	V
DC Collector Current	I_C	$T_c = 80C^0$	1200	A

Parameter	**Symbol**	**Condition**	**Value**	**Unit**
Collector cut-off current	I_{CES}	$V_{CE} = 3300V, V_{GE} = 0$	$12(T_{vj} = 25^0C)$ $120(T_{vj} = 125^0C)$	mA mA
Collector-emitter saturation voltage	V_{CEsat}	$I_c = 1200A, V_{GE} = 15V$	$3.1(T_{vj} = 25^0C)$ $3.8(T_{vj} = 25^0C)$	V V
Rise Time	t_r	$T_{vj} = 25^0C$ $T_{vj} = 125^0C$	0.175 0.2	μs μss
Fall Time	t_f	$T_{vj} = 25^0C$ $T_{vj} = 125^0C$	0.35 0.44	μss μss
Resistance, terminal-chip	R_{CC+EE}	$T_{vj} = 25^0C$ $T_{vj} = 125^0C$	0.06 0.085	mΩ mΩ
Output Voltage Peak Value	V_{0p}	-	2500	V
Output Current Peak Value	I_{0p}	-	12.5	A
Operating Frequency	f_{op}	-	25	kHz
Switching Frequency	f_{sw}	-	50	kHz

TABLE 4.9: Analytic Loss Calculations

(1) Switching Losses			
Loss Estimation Equation	**Calculation**	**Result**	**Unit**
Switching Loss = $\frac{V_{op}}{2} \times \frac{I_{op}}{2} \times (t_r + t_f) f_{sw}$	$\frac{2500}{2} \times \frac{12.5}{2} \times (0.2\mu + 0.4\mu) * 50000$	234.375	W
(2) Conduction Losses			
Conduction losses On time = $(I_{op} \times R_{CC} + V_{CEsat})I_{op} = (I_{op} \times 0.08m + 3.8)I_{op}$	(12.5*0.00008) + 3.8 12.5 = 3.501 * 12.5	47.5125	W
Conduction losses Off time $I_{CES} * V_{op}$	0.120*2500	300	W
Average Conduction Losses = Losses (on time +off time)/2	$\frac{47.5125+300}{2}$	173.75	W

Table-4.9 reveals that when V_{0p}=2500V and I_{0p}=12.5A at 50000Hz switching frequency, the switching losses comes out to be 234.375W, whereas the conduction losses estimated to be 173.75W.

4.10 Summary

The second contribution of this research dissertation is highlighted in this chapter. Firstly it emphasized the model of the inverter as per the performance parameters & literature survey. In that perspective, it concentrated on the design and fabrication of high frequency inverter in half bridge topology perspective keeping in

view various aspects in desirability, constraints and optimization. Mathematical model has been discussed. Inverter losses were also deliberated in the perspective of switching losses, conduction losses and snubber losses. Mathematical evaluation of performance parameters of the proposed power inverter model, encompassing the efficiency and total harmonic distortion (THD) were also reflected concisely. At the end, loss estimation based on data sheet as well as design was also assumed and accomplished.

Chapter 5

Results and Discussion

The output results play a vital and dynamic role in the projected work. In this chapter, the proposed high frequency PWM inverter circuit is simulated by means of MATLAB/SIMULINK. Simulation has been done with and without using dynamic load condition, and the results are presented. The design is also evaluated in term of assessing inverter efficiency under various loads as well as total harmonic distortion. To appraise the anticipated performance of the dc-ac converter, numerous outcomes are simulated to visualize the steady state behavior.

5.1 Single Phase High Frequency Half Bridge Inverter

In this perspective , a single phase half bridge inverter using two switches (IGBTs) with two capacitors shown in Figure 4.8 (chapter 4) is implemented in order to transform 15 KV DC into two equal halves of 7.5 KV square waves with switching frequency of 50 KHz. Figure 5.1 illustrates the simulated outcome of a single phase DC-AC converter in half bridge configuration of design given in Figure 4.8. The measured output and the peak value of load voltage comes to 7.5KV square wave as a fixed voltage. Table 5.1 exhibits the simulation parameters of single phase PWM inverter of design Figure 4.8. Currently, IGBTs have become promising because these are easier to use, faster, and are available in higher voltage and current

ratings. IGBT carries the merits of both MOSFETs as well as BJTs. Like MOSFETs possesses high switching speed with high impedance and like transistors, it devours high gain and low saturation voltage.

TABLE 5.1: Simulation Parameters-1ϕ High Frequency PWM Inverter

Parameter	**Value**
Input DC Voltage (Vin)-Single Phase	15kV
V_{C1}, V_{C2}.	7.5kV
Operating Frequency	25kHz
Switching Frequency(f_s)	50 KHz
IGBTs Specifications	
Internal Resistance (Ron)	1e-3 Ω
Snubber Resistance (Rs)	1e5 Ω
Snubber Capacitance Cs(F)	1e-6 F
Outcomes	
Output Voltage (Simulation Output)	7.5kV AC
Peak Voltage (Simulation Output)	7.5kV

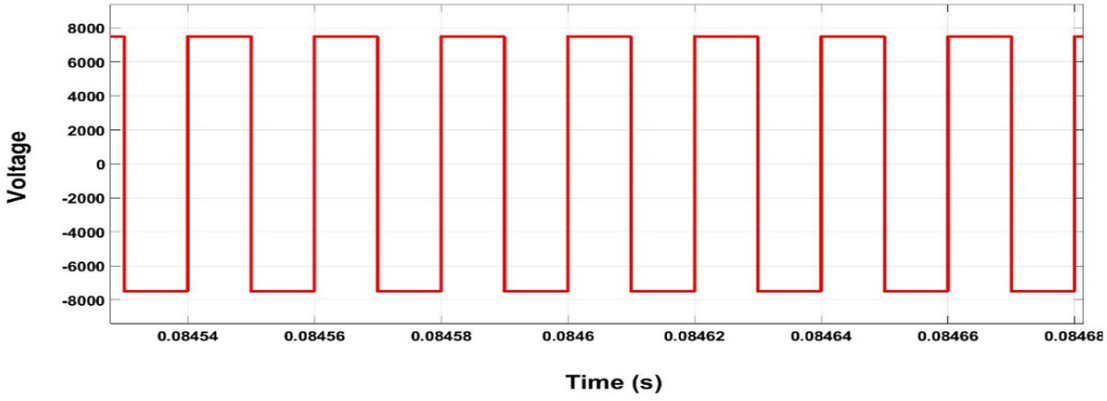


FIGURE 5.1: Single phase Inverter output (15kV DC Input)

In Figure 4.3 (Chapter-4), two switches (S^+ and S^-) are incorporated for single phase inverter. Congruently for simulation perception, IGBTs are taken as a switches replacing S^+ switch with IGBT-1 and S^- switch with a IGBT-2 as depicted in inverter design of Figure 4.8 (chapter-4). From operation perspective of this design, Vgs1 and Vgs2 are the voltages appear across gate terminals G1 and G2 of IGBT-1 and IGBT-2 respectively. Similarly, V_{T1} and V_{T2} are output voltages of switches IGBT-1 and IGBT-2 correspondingly. Figure 5.2 highlights the waveforms sequence of the switches in a single phase (1ϕ) half bridge inverter perspective for design of Figure 4.8. A source is divided into two parts and the gating signals of the two switches (IGBTs) possess a phase angle of 180 degree. When gate voltage-1(Vgs1) is applied for a period of first half cycle (i.e. 180

degrees), the switch-1 will conduct and the load is directly connected to source on the upper arm. Consequently, the output voltage equals to the source voltage(i.e.Vin/2). On removing gate voltage-1(Vgs1) at time, t=T/2(s), the switch-1 will be non-operative. During second half cycle, when gate voltage (Vgs2) is applied, the switch-2 gets turned ON. In this case load will be directly connected to the source (i.e.Vin/2) on the lower arm. The voltage source polarity on the upper & lower arm is opposite to each other. Consequently, in this second half cycle, the output voltage is –(Vin/2) as presented in the output voltage waveform. The output voltage virtually is a square wave and the use of diodes (D1 & D2) in antiparallel connection with switches allows the current to flow when the switch is turned OFF. These diodes (i.e.D1 & D2) are also termed as fly back diodes, for the reason that once these diodes conduct , the energy is fed back to the DC source .

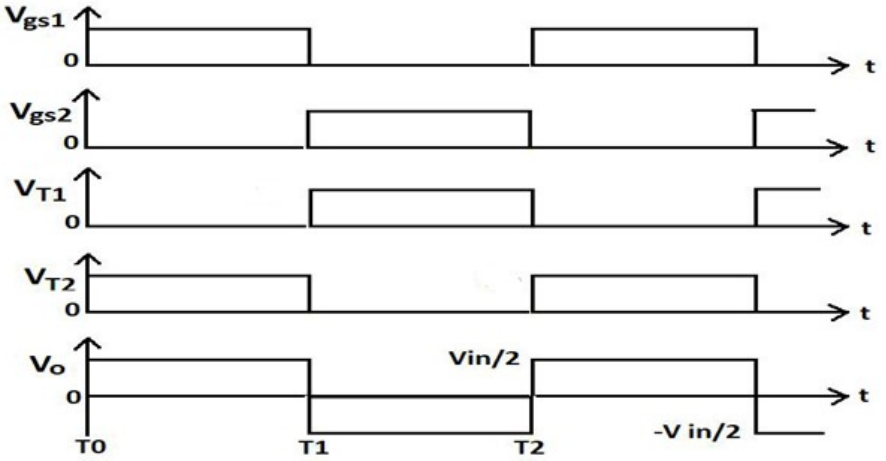


FIGURE 5.2: Sequence Waveforms of a Single Phase Half Bridge Inverter design of figure 4.8

5.2 Proposed Three Phase High Frequency PWM Inverter

Three phase high frequency inverter in half bridge topology, shown in Figure 4.9 (Chapter-4) using six IGBT switches and six capacitors, each phase attaining 5 KV DC in order to convert 15KV DC input into equivalent three phase square wave AC voltage (2.5KV), is implemented. Usually there exist two forms of control signals,which are used to operate the IGBT switches for the execution of three phase inverter. There is 120 degree conduction and 180 degree conduction.

Each one of these control signals, possesses different features in order to yield the anticipated output for a three phase AC squarewave signal. It might be obvious from their nomenclature, that in 120 degree conduction process, every switch will conduct for 120 degrees whereas, in the 180 degree conduction mode, every switch will conduct for 180 degrees. The main advantage of using the control signal in 180 degree conduction mode as compared to the 120 degree conduction mode is that the number of switches which remain ON at any instant of time. In 180 degree conduction perspective, there are three switches with setting the time period to its half value (i.e 50% of Time Period), for every switch to remain ON . Whereas for 120 degree conduction mode, there are only two switches with setting of the time to its one third value (33% of Time Period) allocated for every switch. Table 5.2 shows the parameter values in simulation,concerning input and output data.

TABLE 5.2: Simulation Parameters-3ϕ High Frequency PWM Inverter

Parameter	**Value**
Input DC Voltage (Vin)	15kV
Output Voltage (Calculated)	2.5kVAC
Peak Voltage(Calculated)	2.5kV
Power rated	100kVA
Phase-1 input voltage	5kVDC
Phase-2 input voltage	5kVDC
Phase-3 input voltage	5kVDC
C_1 ,C_2, C_3, C_4, C_5, C_6	10 μF
IGBTs Specifications	
Internal Resistance (Ron)	1e-3 Ω
Snubber Resistance (Rs)	1e3 Ω
Snubber Capacitance Cs (F)	Infinity
Switching frequency(f_s)	50KHz
IGBT voltages	2.5kV
V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C5}, V_{C6}	2.5kV
OUTCOME	
(1) Peak Voltage of each phase ,Vp(VAC)	2.5kV
(2)Line to Line Voltage,V_{LL}(VAC)	4082.43 V AC

Figure 5.3 establishes the 5kV DC input to any one of the phase of this inverter. In simulation chart perspective, the input measured and displayed is exactly of value of 5kV with respect to the timing axis.

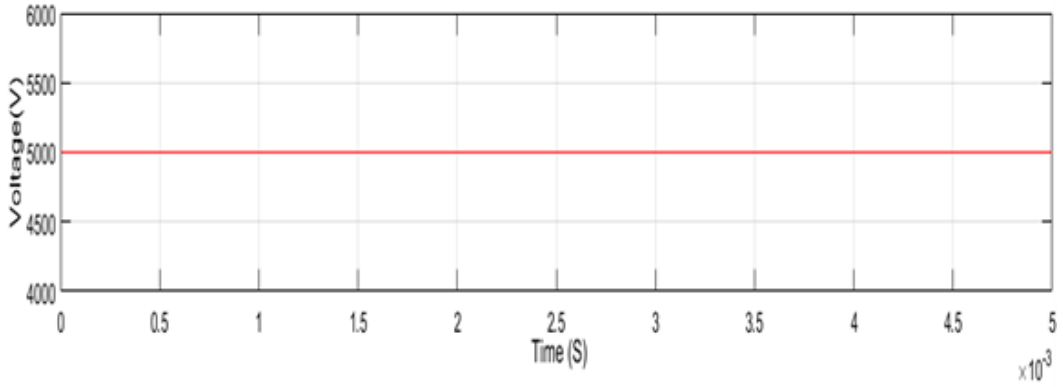


FIGURE 5.3: DC input voltage waveform to single phase half bridge Inverter of figure 4.9

Figure-5.4 depicts the simulated output of the one of the phase of inverter of Figure 4.9,which is infact the input to the next stage (i.e. medium frequency transformer) with frequency of 50 kHz. The 5kV DC is the input to one of the single phase of this anticipated inverter and at the output 2.5kV AC squarewave is received. In this conduction practice, the setting timing for the switches is half the value (i.e 50%) of its time period for every switch to remain ON.

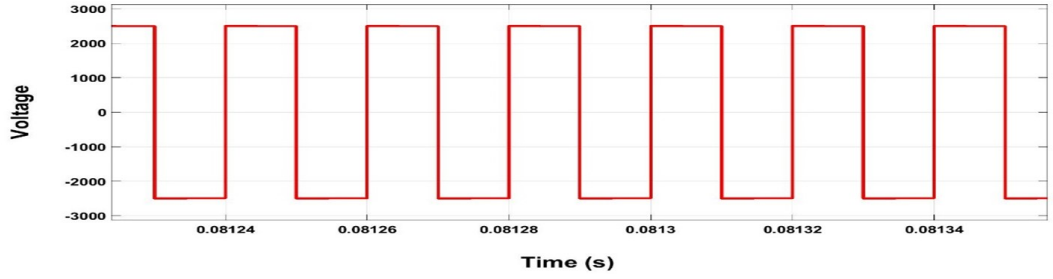


FIGURE 5.4: Simulation output voltage waveform of one of the phase of Inverter of figure 4.9

Figure 5.5 depicts the simulation output voltage waveform of the proposed three phase inverter design of Figure 4.9, each with a peak voltage of 2.5 kV in 50% time period conduction with a switching frequency of 50kHz. Each phase has been given equal DC voltage of 5kV as input and at the output of this three phase half bridge inverter ,each phase delivers an output of 2.5kV squarewave AC.

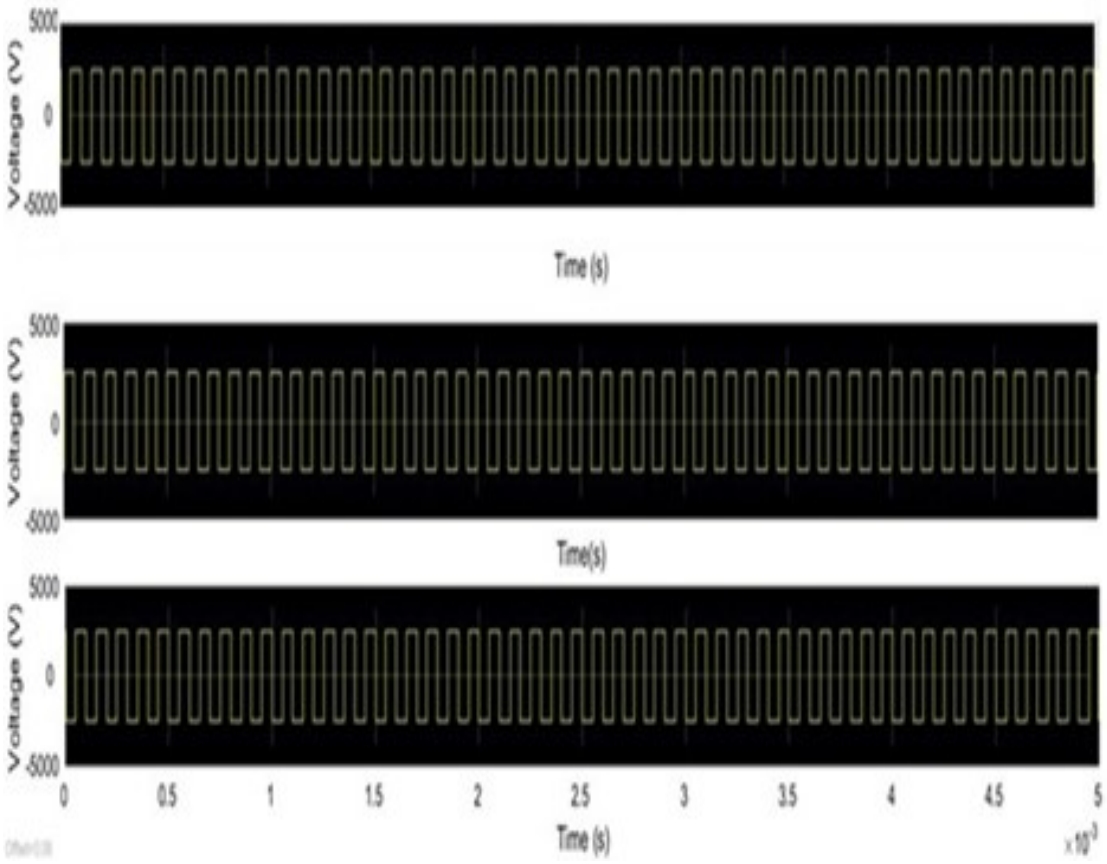


FIGURE 5.5: Simulation Output voltage of proposed three phase inverter design of figure 4.9

Figure-5.6 shows the waveform sequence for three phase inverter design of Figure 4.9 (chapter-4) in 180 degrees conduction (i.e.setting the timing of switches to 50% of its time period) perspective. During the process of switching, phase-1 comprises of pair of switches (switch-1 and switch-2) , phase-2 contains the switching pair (switch-3 and switch-4) and finally phase-3 consists of switching pair (switch-5 and switch-6). At any specified time, both the switches in the same phase, would never be operative(closed), otherwise this situation will lead to the short circuiting of the supply voltage and ultimately result in failure of the entire setup. At any specified time, both the switches in the same phase, would never be operative(closed), otherwise this situation will lead to the short circuiting of the supply voltage and ultimately result in failure of the entire setup. Therefore, such situation should be circumvented at all times.

The design of Figure 4.5 (Chapter-4) divulges that a three phase bridge inverter is equivalent to three half bridge inverters structured side by side in accordance with

a single phase inverter. This arrangement requires six switches and six diodes. In Figure 4.9 (Chapter-4), the synoptic of the driving electronics for the implementation of conversion of the dc voltage into square wave AC voltage in three phase perspective has been deliberated, where the switches have been replaced with IGBTs switches. switch-1(Sw1) is driven by G1, the switch-2(Sw2) is driven by G2, the switch-3(Sw3) is driven by G3, the switch-4(Sw4) is driven by G4, the switch-5(Sw5) is driven by G5 and the last switch-6(Sw6) is driven by G6.

In the start of the switching sequence, the switch-1(Sw1) will be closed (i.e., operative) from 0 degree to 180 degrees, as the designated/allotted time of conduction is 180 degrees. After a lapse of 120 degrees of positive cycle of the first phase, the second phase also in possession of a positive cycle (as depicted in the three-phase voltage graph), so switch-4(Sw4) of this cycle of the second phase will be closed (i.e.operative) after Switch-1(Sw1). Switch-4(Sw4) will also be kept closed for another 180 degrees. So this switch (i.e.Sw4) will be operative(closed) from 120 degree to 300 degree and it will be non-operative (opened) merely after 300 degrees. Likewise, the third phase also has a positive cycle after a lapse of 120 degrees of positive cycle of second phase , therefore the switch (Sw5) will be closed after 120 degees of switch(Sw4) closing (i.e.240 degree). This switch will remain closed for approaching 180 degrees before being opened. In this process, switch-5(Sw5) will be closed from 240 degrees to 60 degrees. Upto this stage, the conduction is completed once the top layer switches are closed (positive sequencing), thereby resulted the completion of current flow.

This switch will remain closed for approaching 180 degrees before being opened. In this process, switch-5(Sw5) will be closed from 240 degrees to 60 degrees. Thereby resulted the completion of current flow. For down layer switches, the Sw2, Sw3 and Sw6 are being closed in a prearranged order. Consequently after Sw1 being opened, the Sw-2 will be in action and closed. Similarly the Sw-3 will be operative (closed) after Sw-3 being opened at 300 degrees. Following the same procedure,the Sw-6 will be closed after the completion of conduction cycle of Sw-5. This switching cycle between switches of the same phase has been deliberated in Figure 5.6,where Sw-2 follows Sw-1, Sw-3 follows Sw-4 and finally Sw-6 follows Sw-5.

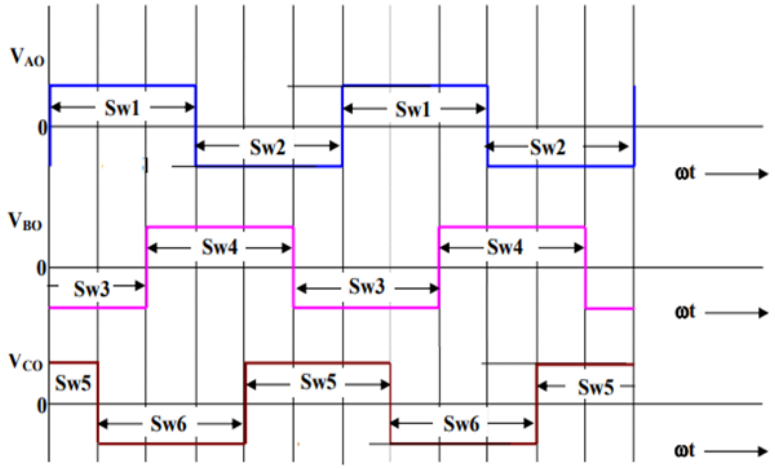


FIGURE 5.6: Waveform Sequence for Three Phase Inverter design of figure 4.9

5.3 Efficiency and Load Analysis

In this section, the proposed DC-AC Converter (Inverter) in a single phase as well as a three phase half bridge high frequency perspective have been evaluated on different resistive loads to assess the conversion efficiency from DC voltage to square wave AC voltage. This performance parameter establishes that how much DC power is converted into an equivalent AC square wave power. In this scenario, some of the power may be lost as a heat, and correspondingly some stand-by power may be exhausted in order to keep the inverter in a powered mode. According to valuation, the efficiency parameter is taken as a linear factor for the systems power yield [152]. For valuation purpose, the switching losses are not taken into considerations, whereas only snubber losses are taken into account. For the utmost system performance, a high efficiency over the entire power range is mandatory.

5.3.1 Single Phase Inverter Efficiency and Load Analysis

A single phase high frequency PWM inverter in half bridge topology perspective, using two IGBTs switches with two high power capacitors is implemented in model for efficiency measuring perspective, shown in Figure-4.8 (Chapter-4). The circuit parameter values taking part in execution of single phase high frequency half bridge inverter model for achieving the requisite data for appraisal/valuation of efficiency have been worked out and illustrated in the successive sections. It is worth noting that the default value of snubber resistor (R_s) is measured in ohms (Ω) and if

this parameter is set to infinity value it will result in elimination of the snubber from the entire model. Similarly the snubber capacitance measured is in farad (F), whose default value is infinite. By setting its value to zero, it eliminates the snubber. On contrary, setting its value to infinity, a resistive snubber is achieved.

5.3.1.1 Single Phase Inverter with Input Voltage 15kV DC

Initially, an effort is made to measure the various data for calculation of efficiency by taking an input/source voltage of 15KV DC to convert into 7.5kV AC square-wave with various loads connection. In this conduct, various measurements for attainment of the requisite parameters have been charted out. Table-5.3 illustrates the circuit parameter values taking part in execution of single phase high frequency half bridge inverter model for achieving the requisite data for appraisal/valuation of efficiency. Figure 5.8 represents a MATLAB simulation model of inverter in single phase configuration perspective. This model simulates a single phase inverter with pulse width modulation (PWM). Table 5.4 illustrates various data received from the simulation of the model on various loads and correspondingly it figure out the conversion efficiency for design of Figure-4.8 and Figure 5.8 depicts the pictorial representation of converter efficiency versus output power for this data.

TABLE 5.3: Circuit Simulation Parameters-1ϕ PWM Inverter (15kV DC Input)

Parameter	**Value**
Input DC Voltage (Vin)	15kV
V_{C1}, V_{C2}	7.5kV
C1,C2	10μF
Output Voltage (simulated output)	7.5kV AC
Peak Voltage (simulated output)	7.5kV
Operating Frequency	25kHz
Switching Frequency(f_s)	50kHz
IGBTs Specifications	
Internal Resistance (Ron)	1e-3 Ω
Snubber Resistance (Rs)	1e7 Ω
Snubber Capacitance Cs (F)	Ie-6 F
Load Resistance	(60Ω-4000Ω)

TABLE 5.4: Efficiency Valuation for Single Phase PWM Inverter (15kV) for design of figure-4.8

Load	Input Voltage	Input Current	Input Power	Losses (W)					Output Voltage	Output Current	Output Power	Efficiency
Ω	(V)	(A)	(W)	Snubber	Switching	On time Cond	Off Time Cond	Total	(V)	(A)	(W)	%
60	15000	62.29	934000	2600	7007.625	175.0328071	18.74	17002.79561	7496	122.3315374	916997.2044	98.1795722
70	15000	53.42	800900	2000	6009.75	150.0325914	18.7425	14357.05018	7497	104.9143591	786542.9498	98.20738542
80	15000	46.75	701100	1500	5259.375	131.24969	18.7425	12318.73438	7497	91.87425178	688781.2656	98.24294189
90	15000	41.57	623300	1300	4676.625	116.6724904	18.7425	10924.07998	7497	81.68279579	612375.92	98.24738008
100	15000	37.39	560900	1300	4206.375	104.9156819	18.7025	9959.986364	7481	73.64523642	550940.0136	98.22428483
200	15000	18.72	280900	400	2106	52.47207014	18.725	4754.39414	7490	36.86857221	276145.6059	98.30744246
500	15000	7.497	112500	100	843.4125	21.0005928	18.74	1866.306186	7496	14.75903066	110633.6938	98.34106117
1000	15000	3.75	562600	40	421.875	10.50225	18.745	942.2445	7498	74.90767611	561657.7555	99.83251964
2000	15000	1.876	28140	20	211.05	5.2533631	18.7475	490.1017262	7499	3.687144722	27649.89827	98.25834497
3000	15000	1.251	18770	20	140.7375	3.5030504	18.7475	345.9761008	7499	2.456864102	18424.0239	98.15676025
4000	15000	0.9389	14080	20	105.62625	2.629061045	18.75	274.0106221	7500	1.840798584	13805.98938	98.05390183

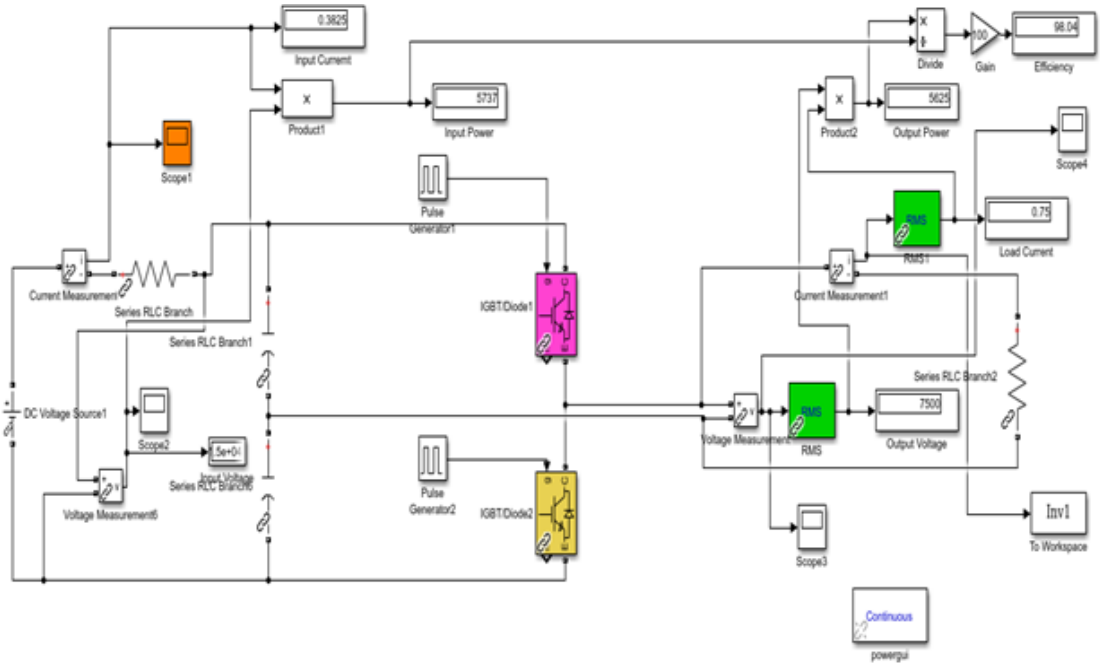


FIGURE 5.7: Single phase Inverter Simulation Model (15kV DC input) for design of figure-4.8

In single phase with 15kV input DC voltage, the conversion efficiency (as per Table 5.5) is higher than the 96% over a various output load resistances ranging from 60Ω to 4000Ω as established in the design. Correspondingly, this design model covers the efficiency range from 98.05% to 98.34% for the mentioned resistive loads. Furthermore, the analysis of the evaluated efficiencies given in Table 5.4 also reveals that the efficiency variation exists from heavier (60Ω) load to lighter (4000Ω) load. Actually, there are two kinds of losses in power electronic systems namely constant losses and variable losses. Constant losses are the losses that are independent of

load, whereas the variable losses depend on load. The constant losses in this design simulation are the snubber, whereas the variable losses are IGBT switching losses and conduction losses. Since constant losses are independent of the load, therefore these losses are same for both light and heavy loads. At lighter load, the processed power is lesser whereas the constant losses are same; hence accordingly at light load the inverter efficiency is lower. Similarly, at heavier load the processed power is greater and the constant losses are same, therefore at heavier load the efficiency is more respectively. It is worth mentioning that the input currents, input powers and snubber losses are stated/measured from the execution of simulation of Figure 5.7, whereas the output parameters/ data and the losses containing switching losses and conduction losses(on time/off time) have been derived/calculated using various formulae. Table 5.4 reveals that the snubber loss is almost constant with slight variation of its value from load to load due to the resistive load as well as simulation execution.

5.3.1.2 Single Phase Inverter with Input Voltage 05kV DC

In another test, figure 5.7 is considered for second time for the measurements of the efficiency by taking an input/ source voltage of 05kV DC as exhibited in Figure 5.8. The requisite parameter specification for appraisal of conversion efficiency is depicted in Table 5.5. Table 5.6 exhibits the various data received from the simulation of the design.

Table 5.5: Circuit Simulation Parameters-1ϕ PWM Inverter (05kV DC Input)

Parameter	**Value**
Input DC Voltage (Vin)	05kV
V_{C1}, V_{C2}	2.5kV
C1,C2	10μF
Output Voltage (simulated output)	2.5kV AC
Peak Voltage (simulated output)	2.5kV
Operating Frequency	25kHz
Switching Frequency(f_s)	50kHz
IGBTs Specifications	
Internal Resistance (Ron)	1e-3 Ω
Snubber Resistance (Rs)	1e7 Ω
Snubber Capacitance Cs (F)	Ie-6 F
Load Resistance	(65Ω-4000Ω)

TABLE 5.6: Efficiency Valuation for Single Phase Inverter (05kV) for design of figure-4.8

Load	Input Voltage	Input Current	Input Power	Losses (W)					Output Voltage	Output Current	Output Power	Efficiency
Ω	(V)	(A)	(W)	Snubber	Switching	On Time Cond	Off Time Cond	Total	(V)	(A)	(W)	%
65	5000	19.17	95820	250	718.875	53.73479822	6.2475	1807.714596	2499	37.61996215	94012.2854	98.11342664
70	5000	17.81	88990	220	667.875	49.91875138	6.2475	1668.082503	2499	34.9427441	87321.9175	98.12553938
80	5000	15.58	77900	170	584.25	43.66283782	6.2475	1438.320676	2499	30.59691049	76461.67932	98.153632
90	5000	13.86	69260	140	519.75	38.83873594	6.2475	1269.672472	2499	27.20701382	67990.32753	98.16680267
100	5000	12.47	62350	110	467.625	34.94088014	6.2475	1127.62676	2499	24.4987488	61222.37324	98.19145668
200	5000	6.242	31210	40	234.075	17.48383401	6.25	525.617668	2500	12.27375293	30684.38233	98.31586777
500	5000	2.499	12500	10	93.7125	6.9981992	6.25	217.9213984	2500	4.912831441	12282.0786	98.25662881
1000	5000	1.25	6251	4	46.875	3.50025	6.2475	116.2455	2499	2.454883754	6134.7545	98.14036954
2000	5000	0.6254	3127	3	23.4525	1.75118258	6.25	65.90736516	2500	1.224437054	3061.092635	97.89231323
3000	5000	0.4171	2086	3	15.64125	1.167907836	6.25	49.11831567	2500	0.814752674	2036.881684	97.64533482
4000	5000	0.313	1585	3	11.7375	0.876415675	6.25	40.72783135	2500	0.617708867	1544.272169	97.43042074

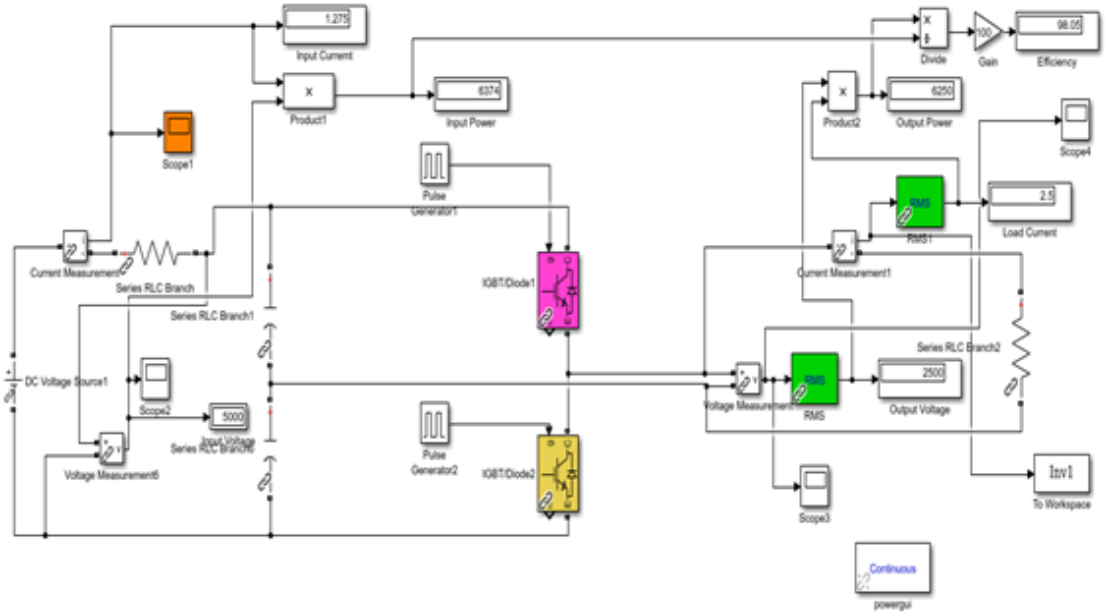


FIGURE 5.8: Single phase Inverter Simulation Model (5kV DC input) for design of figure-4.8.

In a single phase inverter with 05kV input DC voltage, the conversion efficiency (Table 5.6) is also higher than the 96% over a various output load resistances ranging from 65Ω to 4000Ω as established in the design. Correspondingly, this design covers the efficiency, ranging from 97.43% 98.11% to the mentioned load resistances. The variation of inverter efficiencies observed at various loads reveals that at lighter load, the processed power is lesser whereas the constant losses (i.e. snubber losses) are same; hence accordingly, at lighter load the efficiency is lower to an extent. Similarly, at heavier load, the processed power is better and

the snubber losses are same, therefore at heavier load the efficiency is greater. It is also mentioned that the input currents, input powers and snubber losses are stated/measured from the execution of simulation of figure 5.8, whereas the output parameters/ data and the losses containing switching losses and conduction losses(on time/off time) have been derived/calculated using their various formulae. Table 5.6 also reveals that the snubber loss is almost constant with slight variation of its value due to the resistive load as well as simulation execution.

5.3.2 Three Phase Inverter Efficiency and Load Analysis

The proposed three phase high frequency PWM inverter in half bridge topology perspective, using six IGBTs switches with six capacitors is simulated in three single phase perspective. Table-5.7 illustrates various simulation parameter values taking part in execution of this model for achieving various data required in measurements of efficiency. In this case,the efficiency is measured incorporating various but equal balanced resistive loads (i.e.190Ω-10000Ω) in each phase. Figure 5.9 represents the MATLAB simulation model of inverter. Various measurements for requisite parameters in execution of simulation have been charted out. In this context, table 5.8 illustrates the various data received from the simulation model in a three single phase perspective. In this context, table 5.8 illustrates the various data received from the simulation model in a three single phase perspective.

Table 5.7: Circuit Simulation Parameters- Three Phase PWM Inverter

Parameter	**Value**
Input DC Voltage (Vin)	15kV
Power rates	100kVA
C1,C2,C3,C4,C5,C6	10μF
Operating Frequency	25kHz
Switching Frequency(f_s)	50kHz
IGBT voltages	2.5kV
V_{C1}, V_{C2}, V_{C3},V_{C4},V_{C5},V_{C6}	2.5kV
Source Resistance	0.1Ω
IGBTs Specifications	
Internal Resistance (Ron)	1e-3 Ω
Snubber Resistance (Rs)	1e7 Ω
Snubber Capacitance Cs (F)	Ie-6 F
Load Resistance	Static Load

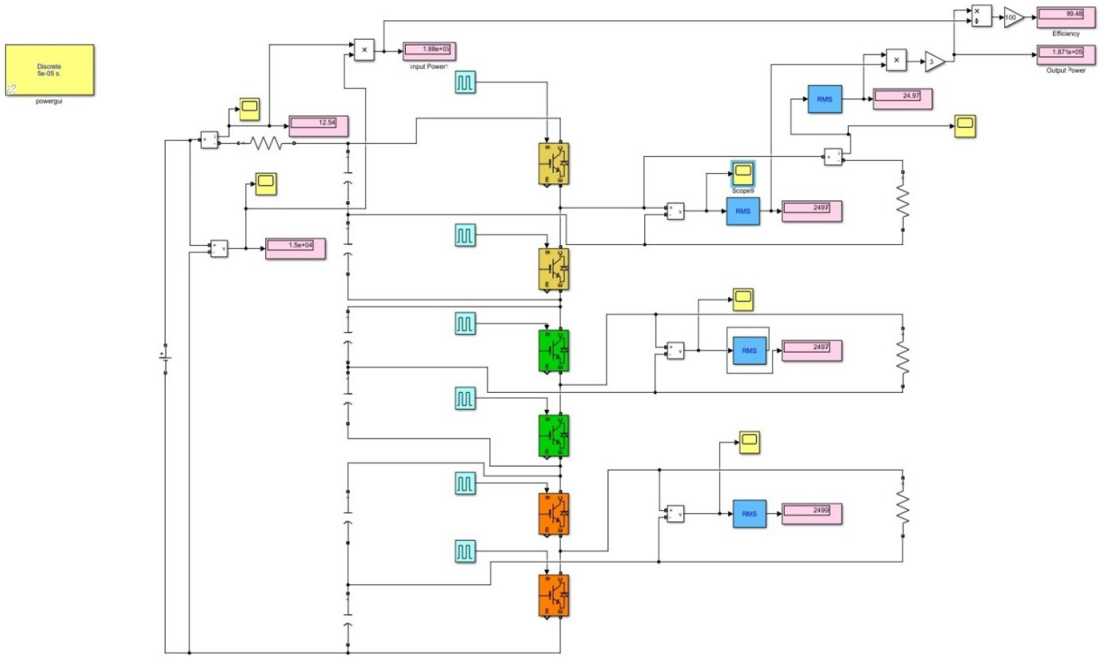


FIGURE 5.9: MATLAB simulation model for three phase PWM Inverter design of figure-4.9

TABLE 5.8: Efficiency Valuation- Three Phase PWM Inverter design of figure-4.9

Load	Input Voltage	Input Current	Input Power	Losses (W)					Output Voltage	Load Current	Output Power	Efficiency
Ω	(V)	(A)	(W)	Snubber	Switching	On Time Cond	Off Time Cond	Total	(V)	(A)	(W)	%
190	15000	6.579	98680	20	740.1375	18.42812532	6.25	1549.631251	2500	38.8521475	97130.36875	98.42964
195	15000	6.41	96150	20	721.125	17.9545741	6.25	1510.659148	2500	37.85573634	94639.34085	98.42885164
197	15000	6.313	94700	20	710.2125	17.68277664	6.25	1488.290553	2500	37.28468378	93211.70945	98.42841547
200	15000	6.25	93750	20	703.125	17.50625	6.2425	1463.7475	2497	36.95885162	92286.2525	98.43866933
500	15000	2.5	37510	10	281.25	7.001	6.2475	598.997	2499	14.77030932	36911.003	98.40310051
1000	15000	1.25	18760	10	140.625	3.50025	6.2475	307.7455	2499	7.383855342	18452.2545	98.35956557
2000	15000	0.6255	9382	7	70.36875	1.7514626	6.25	163.7404252	2500	3.68730383	9218.259575	98.25473859
3000	15000	0.4172	6257	7	46.935	1.168187849	6.25	115.7063757	2500	2.45651745	6141.293624	98.15076913
4000	15000	0.313	4695	7	35.2125	0.876415675	6.25	91.67783135	2500	1.841328867	4603.322169	98.04733054
5000	15000	0.2505	3757	7	28.18125	0.70141004	6.25	77.26532008	2500	1.471893872	3679.73468	97.94343039
10000	15000	0.1255	1882	7	14.11875	0.35140252	6.25	41.44030504	2500	0.736223878	1840.559695	97.79807093

In three phase inverter containing three single phases (with 15kV input DC voltage), the conversion efficiency (Table 5.8) ranging from 97.79% to 98.42% is higher than 96% over a various output load resistance ranging from 190Ω to 10000Ω for each phase ,as established in the design . Correspondingly, this design covers the efficiency range from 97.79% to 98.42% to the resistive loads already mentioned. Further, from the exploration of the evaluated efficiencies for various resistive loads (190Ω to 10000Ω) given in Table-5.8, it is apparent that the higher efficiency (98.42%) exists at heavier (190Ω) load and lower efficiency (97.79%) at lighter

(10000Ω) load. The reason for this variation is that at lighter load, the processed power is lesser whereas the snubber losses are same; hence accordingly at lighter load, the efficiency is lower. Correspondingly, at heavier load, the processed power is larger and the snubber losses are same, therefore at heavier load the efficiency is greater. It is well noticed that the input currents, input powers and snubber losses are stated/measured from the execution of simulation of Figure 5.9, whereas the output parameters/ data and the losses containing switching losses and conduction losses(on time/off time) have been derived/calculated using various formulae. Table 5.8 also divulges that the snubber loss is virtually persistent with slight variation of its value due to the resistive load as well as simulation execution.

5.4 Inverter Losses

Inverter system is primarily comprised of the Insulated Gate Bipolar Transistors (IGBTs) and its antiparallel diode. Both these components work in the on-off state and sporadically experience a diversity of dynamic and static process. Each of these processes yields the portion of the loss and (by summing these losses) the total loss of the switching device. The total loss is comprised of primarily by conduction losses and switching losses. With resistive loads, the diodes across the transistors have no function. An IGBT is taken as a voltage-controlled device which combines the merits/advantages of a MOSFET and a BJT. Power losses in IGBTs are mostly comprised of steady–state conduction losses and switching losses. Conduction losses on power electronics switching devices occurs due to the reason that during conduction period the switching devices do not perform/act as an ideal switch (zero on-state resistance and zero voltage drops). Undeniably, these devices possess an on-state resistance and an amount of forward voltage drop on the device. IGBT necessitates for only a small voltage in order to maintain conduction in the device unlike in BJT. The IGBT is a unidirectional device which can only switch ON and conduct in the forward direction. This means that the flow of current takes place from the collector to the emitter unlike in MOSFETs, which are bi-directional. In simulation perspective, the snubber losses are fixed (i.e. constant) only; whereas the conduction losses and switching losses both are

variable losses and depend upon load. The deliberation of both the variable losses is as under:-

- The switching losses in semiconductor device occur when there is transitioning takes place from the blocking state to the conducting state and vice-versa. This interval is evaluated by a momentous voltage across its terminals and a substantial current through it. The energy dissipated in each transition has to be multiplied by the frequency in order to obtain the switching losses. For single phase half bridge inverter with 15KV DC input, the switching losses are calculated which are ranging from 7007.625W to 105.6263W for the resistive load ranging from 60 Ω to 4000 Ω. In case of single phase half bridge inverter with 05KV DC input, the calculated switching losses are extending from 718.875W to 11.7375W for the resistive load (65 Ω to 4000 Ω). Similarly for the proposed three phase inverter the calculated switching losses are experienced to be ranging from 740.138W to 14.1188W for the resistive load (190Ω to 10000 Ω). The reverse recovery time aspect does not relate to the IGBT. It is related to power diodes in reverse recovery characteristics. The use of anti-parallel diode across a switch is in practice to provide path for reverse current in case of inductive load. It is related to power diodes in reverse recovery characteristics. The use of anti-parallel diode across a switch is in practice to provide path for reverse current in case of inductive load.

- PWM high frequency inverter is a part of transformer isolated DC-DC converter and output voltage of this inverter is ought to be a square-wave due to high frequency switching at 50 kHz. PWM high frequency inverter is a part of transformer isolated DC-DC converter and output voltage of this inverter is ought to be a square-wave due to high frequency switching at 50 kHz. The input voltage to the ensuing stage (i.e. MFT) is of square-wave pulse. SPWM technique involves Frequency Modulation Ratio (fm). At 50 kHz frequency, if the fm becomes 10, the required switching frequency will be 500 kHz, which is not practicable. The last stage of SST is Low Frequency Inverter (LFI), which will definitely produce the output in a sine-wave form in order to feed the end consumer as a 381VAC.

- The conduction losses occur when the device is in a full conduction state. In this scenario, the amount of current in the device exists which is required by the circuit and the amount of voltage at its terminals is the voltage drop takes place due to the device itself. These losses are taken to be in direct relationship with the duty cycle. For single phase half bridge inverter with 15KV DC input, the conduction losses (on time+off time) are calculated which are ranging from 193.77W to 21.37W for the resistive load (60 Ω to 4000 Ω). In case of single phase half bridge inverter with 05KV DC input, the calculated switching losses are ranging from 59.97W to 7.12W for the resistive load ranging from 65 Ω to 4000 Ω. Correspondingly for the proposed three phase inverter the calculated switching losses are extending from 24.67W to 6.40W for the resistive load (190Ω to 10000 Ω).

- In all three tables (i.e. Table-5.4, Table-5.6 and Table-5.8) the snubber power loss is the simulated loss which is in fact the difference between the input power and output power. Table 5.9 illustrates various circuit parameter values taking part in execution of single phase high frequency half bridge inverter model for achieving/appraisal of snubber power losses. Illustrates various circuit parameter values taking part in execution of single phase high frequency half bridge inverter model for achieving/appraisal of snubber power losses.

TABLE 5.9: Simulation Parameters for appraisal of Snubber losses

Parameter	**Value**
Input DC Voltage (Vin)	15kV
V_{C1}, V_{C2}	7.5kV
Switching Frequency(f_s)	50kHz
Load Resistance	Infinite Ω
IGBTs Specifications	
Internal Resistance (Ron)	10e-3 Ω
Snubber Capacitance Cs (F)	1e-6 F
Snubber Resistance (Rs)	(1e3 Ω - 1e10 Ω)

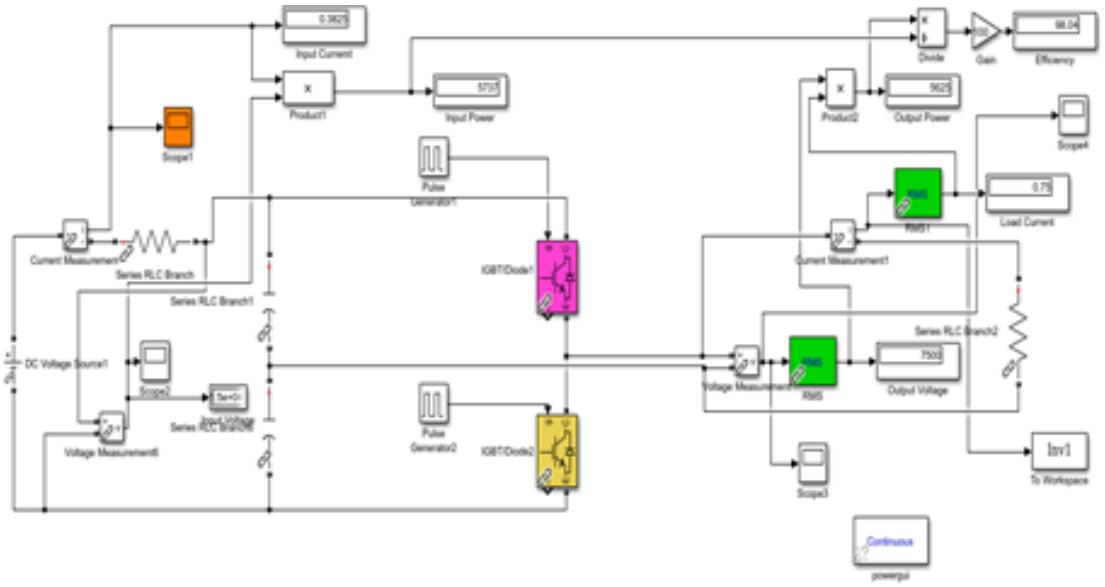


FIGURE 5.10: MATLAB simulation model for effect of snubber resistor on snubber loss for fig-4.8

Figure 5.10 is used in simulation for observing the effect of snubber resistor on snubber loss, whereas the Table 5.10 shows the effect of snubber resistor on snubber loss in single phase inverter.

TABLE 5.10: Effect of snubber resistor on snubber loss in single phase inverter

$\mathbf{R}_{(IGBT)ON}$ Ω **Snubber Resistance**	**Current (V)**	**Snubber Loss ($\mathbf{P}_s$=$\mathbf{P}_{in}$)(W)**	**Output Voltage (V)**	**Load Current (A)**	**Output Power (W)**
1e3	14.98	224800	7492	0	0
1e4	1.5	022500	7499	0	0
1e5	0.15	002250	7500	0	0
1e6	0.015	000225	7500	0	0
1e7	0.0015	00022.5	7500	0	0
1e8	0.00015	0002.25	7500	0	0
1e9	0.000015	00.225	7500	0	0
1e10	0.0000015	00.0225	7500	0	0

The analysis of simulation for observing the effect of snubber resistor on snubber loss (Table 5.10) divulges that with increase in snubber resistance, the input current is reduced , thereby resulting into the reduction of snubber power losses correspondingly while maintaining the output voltage persistent. For reduction of the switching losses, it is essential that the voltage and current waveforms of IGBT during the turn-on or turn off transition periods may be manipulated in order to eliminate or to lessen the overlap. Moreover these switching losses in inverters (generating output voltage in the form of the rectangular wave) depend

directly on the output voltage frequency, which is the same (i.e. output voltage frequency equals the switching frequency of IGBTs). When the inverter operates with the pulse width modulation (PWM) technique, the switching losses do not practically depend on the frequency of the output voltage; rather depend directly on the switching frequency. PWM strategy is considered to be one of the standard methods for power conversion.

5.5 Total Harmonic Distortion Measurement

It is clear and apparent from the analysis of simulation outcome that the inverter that the output voltage waveform is virtually a square wave, which is quite rich of harmonics. These harmonic components are considered to be harmful for the load as well as for the system, for the reason that these harmonics increase the I2R losses; thereby generating the heat. Nevertheless, among the various performance parameters incorporated to evaluate the amount of distortion in the output voltage waveform of the inverter is the total harmonic distortion (THD), which is the most viable and significant one. There are mainly two frequencies in inverters: (1) The output voltage frequency and (2) the frequency of the switching signal. Although, the inverter tries to make the output voltage with a fixed, programmed and predetermined frequency, but even then excessive harmonic signals are added to the output voltage because of the switching actions. The harmonic signals are types of noise whose frequencies are multiples of the switching frequencies. The foremost reason of harmonic signals is that the switches open and close with a fixed switching frequency. The output voltage total harmonic distortion (THD %) factor can be abridged by using a low pass LC filter between the inverter output and the load. This well-designed output filter can filter out these harmonics, but even then one or two harmonics near the cut-off frequency can still persist /survive and distort the output waveform.

From Table 5.4 and Figure 5.7, it is clear that in all the case of varied resistive loads, the input dc voltage is fixed (i.e. 15000V) and output voltage is also constant to an amount of 7500V. So the Total Harmonic Distortion (THDs) comes analytically to an estimation of 48.43%. On the same analogy, the figure 5.8 and table 5.6 also

show that in all the case of varied resistive loads, the input dc voltage is fixed (i.e. 5000V) and output voltage is also constant to an amount of 2500V. Therefor the Total Harmonic Distortion (THDs) comes to a valuation of 48.43%. For three phase PWM inverter in half bridge perspective, referring, the analytical valuation of THD comes to an estimation of 31.083%.

Furthermore, an attempt is made to simulate the proposed model in MATLAB / Simulink using powergui Fast Fourier Transform (FFT) analysis tool to measure total harmonic distortion at the output voltage through Workspace block. In the waveform design, the harmonics/ harmonic frequencies of periodic voltages are deliberated to be the frequency components, which are taken/computed at integer multiples of the frequency of the main signal. Fast Fourier Transform (FFT) of the periodic waveform reveals these results. Harmonic distortion is the consequence of the distortion of the signal due to these harmonics. Total Harmonic Distortion measurement for three phase proposed design is undertaken using modulation technique. In this arrangement with 15KV dc input, the simulated THD comes out to be 47.73% for all the three phases. FFT analysis is shown in figure 5.21.

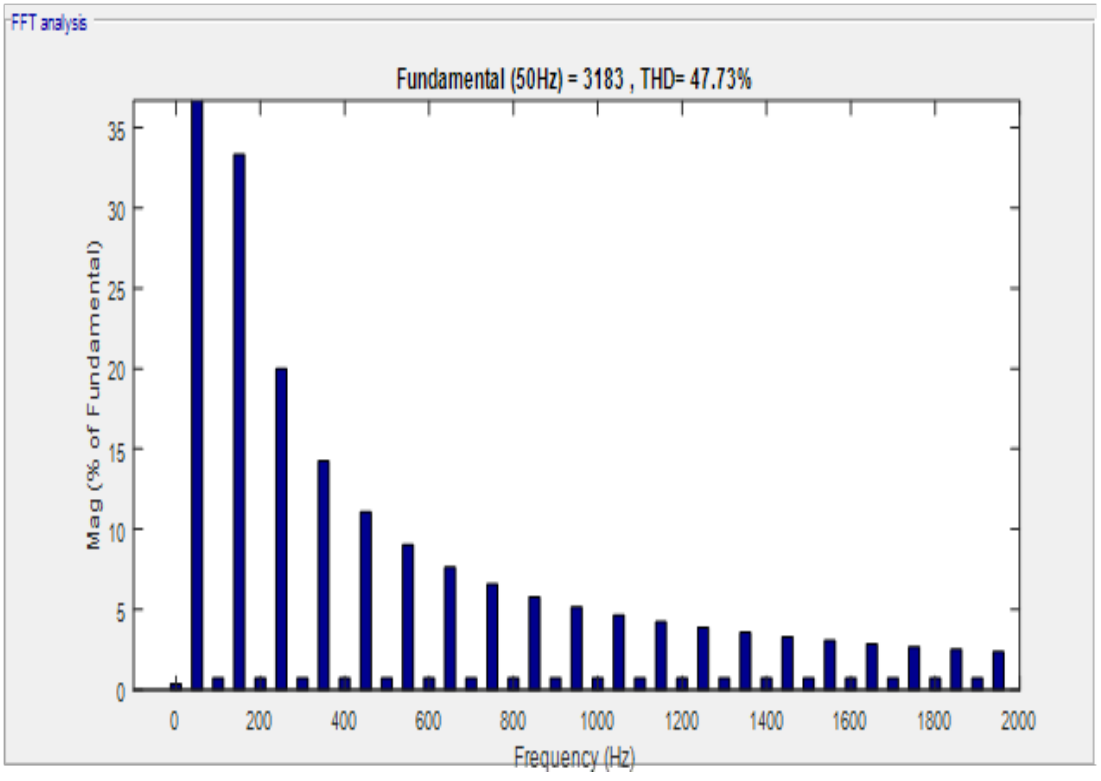


FIGURE 5.11: FFT Analysis for design of figure-4.9

5.6 Analysis of Results and Discussion

After the assortment of the requisite inverter topology and its arrangement in single phase as well as three phase perspective, it was simulated and worked out with the calculated values. In appraisal of the proposed inverter design with the rest of the existed configurations/ topologies of inverters deliberated during literature survey, following have been deduced from the simulation test / trials as well mathematical evaluation:

- The significance of the half bridge configuration is emphasized in terms of its output voltage, the number of bridges, the driving switches and the design complexity. These are the few parameters which merit for the low cost and circuit simplification. The half bridge arrangement is adopted for the reasons as: (1) output voltage is half as compared to full bridge voltage requirement (i.e. step down) (2) number of bridges requirement is half as compared to full bridge topology (3) simplification of a power scheme layout (4) the reduction in complexity of control and protection circuit (5) significant saving/reduction in inverter price/cost and (5) the attainment of substantial and significant converter efficiency.

- IGBTs semiconductor switches are adopted in the inverter system for the reason that these are easier to use, faster, and are available in higher voltage/current ratings. These devices carry the merits of both MOSFETs and BJTs. Like MOSFETs, possess high switching speed with high impedance and like BJTs, produce high gain and low saturation voltage. IGBT is a unidirectional device which can only switch ON and conduct in the forward direction and flow of current takes place from the collector to the emitter unlike in MOSFETs, which are bi-directional.

- Being a high frequency PWM inverter [3*(5kVDC/2.5KV wave AC)] in 100KVA solid state transformer applications, this design found to be producing virtually a square wave shaped voltage output with peak voltage of 2.5 kV in each phase which is a required input AC voltage to the ensuing stage (i.e. MFT).

- In inverter optimization perspective, the various constraints/limitations which are given for due deliberations/achievement includes: (1) efficiency augmentation (2) reduction of cost/volume and (3) the delivery of stable output square wave AC. These restrictions were dealt / addressed in a befitting manner and ultimately came up with the impeccable design. These implementations proved to be valuable ones and led for acquiring the essential and indispensable results.

- At 15kV DC input to the designed inverter (in a single phase perception), the calculated output power comes to the valuation of 27649.89827W using resistive load of 2000Ω. At this ouput the total loss (including snubber,conduction and switching loss) is estimated to be 490.1017 W as is evident from Table 5.4. Similarly, again at the 15KV input dc, the simulator input power comes to an estimation of 28140 W using resistive load of 2000 Ω with the input supply current of 1.867amperes.

- For the data given above in the preceding step, resorting for appraisal of the inverter efficiency, the efficiency calculated as 98.25834497%. The deterioration / degradation of the simulator measured efficiency is due to the system losses occured in simulation execution. These losses include IGBT semiconductor snubber,conduction and switchng losses.

- From the study of Table-5.4 and Table-5.6, the appraised inverter efficiency is appreciable and substantial. In a single phase arrangement (with 15kV DC input), the inverter efficiency is ranging from 98.05% to 98.34% with the resistive output load (60Ω - 40000Ω); whereas with 05kV DC input, the simulated inverter efficiency is ranging from 98.05% to 99.96% with the resistive output load (65Ω - 4000Ω). In case of three phase inverter formed by three single phase inverter, the inverter efficiency found to be ranging from 97.7980% to 98.42964% at resistive output load (190Ω - 10000Ω).

- Analysis of the evaluated efficiencies revealed that the efficiency variation in simulation is due to the losses which occurred during simulation execution. Basically, there are two types of losses dynamically take place in power electronic systems namely as constant losses and variable losses. Constant

losses in simulation of this design include snubber losses, whereas the variable losses are the switching losses and conduction losses. Constant losses also affect the efficiency parameter thereby the snubber losses deteriorate the efficiency performance.

- The snubber losses are almost constant/fixed one ,which are appraised in the execution of inverter models as per following detail:
  - For single Phase half bridge inverter with 15kV dc input : 110W-112W
  - For single Phase half bridge inverter with 5kV dc input : 120W to 124W
  - For three Phase half bridge inverter with 15kV dc input : 370W to 380W

- As the snubber losses are practically constant, at higher load (i.e.100Ω), the output power (P_{out}) is increased/high, the efficiency (i.e. $\frac{P_{out}}{P_{out}+Losses}$ ot $\frac{P_{input}-Losses}{P_{input}}$) also increased/high. Whereas on contrary at the lower load (i.e.10000 Ω), the efficiency is reduced/lower.

- Analysis of simulation fallouts for snubber losses (i.e. Table 5.10) reveals that with increase in snubber resistance; the input current is reduced; thereby resulting into reduction/decline of snubber power losses correspondingly, while maintaining the output voltage constant. When the inverter is subjected to operate with the pulse width modulation (PWM) technique, then switching losses do not practically depend on the frequency of the output voltage; rather depend directly on the switching frequency. Therefore the PWM strategy is considered to be one of the standard techniques for power conversion.

- Total Harmonic Distortion (THD) is considered to be a measure of harmonic pollution in the inverter system and it is experienced that variations in the input DC voltages and switching frequency of inverter both affect the THD aspect of inverter output voltage. Mathematically, the THD for single phase inverter with input DC of 5000 V is given as 48.43%. On the same analogy ,the THD valued for three phase inverter comprised of three single phases is also 48.43% ,which exhibits that the output voltage waveform of the inverter

being a square wave is quite rich of harmonics. Moreover, from the calculation it is also evident that THD is not dependent on the load connected at the inverter output as it is already established in the design chapter. With the application of requisite filter arrangement (i.e. Low Pass Filter etc.), such performance parameter can be minimized to bare minimum level and be improved to certain level. In the simulation perspective in modulation technique, such THD can be measured. Fast Fourier Transform (FFT) analysis of the proposed design divulges the simulated THD as 47.73% (for every phase).

- As per IEEE-519, Voltage distortion (THD) limit for BUS voltage V, (69V$\leq$ V <1kV) is 5.0% at the point of common coupling (PCC), which is subjected to the output voltage of complete power supply system (i.e. SST). This THD limit will be attained at the 50 Hz, output of LF Inverter, being the last stage of SST. 48.8% THD pertains to the square-wave output voltage waveform of HF inverter, which is in order.

- The high frequency inverter (being part of 2nd and 3rd SST topology) is the most significant and exciting part of solid state transformer (SST), therefore the anticipated inverter design is furnished in such a manner that it must offer a stable and desired output voltage level at 50 kHz switching frequency with minimum number of driving switches with emphasis on enhanced efficiency, less cost and better voltage regulation incorporating PWM technique. This regulated output voltage is the input voltage to the ensuing stage i.e. Medium Frequency Transformer (MFT) of SST.

- Solid State Transformer (SST) cost is higher than Line Frequency Transformer (LFT) cost. Nevertheless, with advances and progresses in power electronics, it is anticipated that the cost of SST decreases. However, on contrary, it is expected that the escalation in the price of copper and electrical steel sheets causes an increase in the cost/price of Line Frequency Transformer [191].

- The higher the switching frequency, the greater the numbers of times the switch changes state per second. Switching losses are proportional to the

switching frequency. In nutshell, the switching losses are increased with increase in switching frequency. Therefore, in this design as a tradeoff 50 kHz switching frequency is used.

- In research perspective, the ferrite medium, operating at 50% duty cycle within dual half bridge (DHB), is preferred for practice not only to provide galvanic isolation but also to step down the voltage levels. It provides high resistance to high current and low eddy current losses over several frequencies. Its extraordinary permeability augments its ideal and model combination for use in high frequency transformers.

- Neutral Point concept exists in transformer, where the secondary winding of it may be loaded as Y (wye) connected. However the provision of neutral point is out of question in this anticipated design, being an entity of DC-DC converter. The provision of neutral point at the end of last stage of SST (i.e. Low Frequency Inverter) will be taken place in Y connected load in order to connect the end consumer with 381 VAC. The provision of neutral point at the end of last stage of SST.

- The reverse recovery time aspect does not relate to the IGBT. It is related to power diodes in reverse recovery characteristics. The use of anti-parallel diode across a switch is in practice to provide path for reverse current in case of inductive load. It is related to power diodes in reverse recovery characteristics. The use of anti-parallel diode across a switch is in practice to provide path for reverse current in case of inductive load.

- In case of conventional transformer (LFT), the total loss is the combination of core loss and copper Loss, whereas in case of Solid State Transformer (SST), the total loss is comprised of core loss, copper loss and converter loss. With increase in loss, the system efficiency is affected and deteriorated. Comparing LFT and SST efficiencies is somewhat multifarious and ambiguous. The LFT efficiency is very high, about 98.5% to 99.5%, while the SST efficiency has been indicated in various articles to be around 90% to 98.1%. At a glance, the SST efficiency may be lower/inferior than LFT, however if the complete system set is deliberated, it may lead to a diverse result [220].

5.7 Comparison of Proposed Design with the Existed Design

The most important power-electronic circuits in practical applications are the Pulse Width Modulation (PWM) based inverters. These inverters have attained a remarkable place in the fabrication/design of two or three stage solid state transformer. These inverters generate the desired AC square wave output voltage from DC voltage levels at its input, giving an output voltage changing between two voltage levels only for the ensuing stage (i.e. Medium Frequency Transformer). The proposed design has been accomplishes as per the problem statement and laid out objective. An appraisal has been carried out as per literature existed inverter in the subsequent Table-5.11, which proves that the conferred inverter is an appropriate choice.

TABLE 5.11: Proposed inverter design outcome vs. the existed design

Serial #	Parameter	Proposed Design	Existed Design	Reference
1.	Output Voltage	Half of the supply voltage.(*As a requirement of step down voltage for subsequent stages of three stage inverter)*	Supply Voltage	[47, 57, 58]
2.	Output Waveform	Square wave	Square *except that output goes to zero volts for a time before switching positive or negative wave*	[57, 82]
3.	No of semiconductor devices conducting simultaneously	One	Two*(even more)*	[94]
4.	Number of Switching Devices	Two Per Phase	Four Per Phase*(even more in MLI)*	[57, 58]
5.	Size of the inverter system(per unit)	0.86 p.u.	1.00 p.u.	[58]
6.	Switching Power Loss*(per unit)*	0.5 p.u.*(For same power if voltage is half then current is double)*	1.00 p.u.	[58]
7.	Design Complexity*(per unit)*	Simpler	Complex	[82, 89]
8.	Complexity Factor*(per unit)*	0.85 p.u.	1.00 p.u.	[47, 57, 58]
9.	Cost*(per unit)*	0.86 p.u.	1.00 p.u.	[57, 58]
10.	Suitability	Medium and high power applications	Medium and high power applications	[44–46]
11.	Inverter Efficiency*(single phase)*	99.94%	96.00%	[82, 96]

Serial #	Parameter	Proposed Design	Existed Design	Reference
12.	Inverter Efficiency *(Three phase)*	99.98%	96.00%	[82, 96]
13	Total Harmonic Distortion(THD)	48.43%	47.73%	[82, 96]

As per comparison, to estimation, the half bridge inverter provides a benefit of over 40% as compared to the two extra transistors used in other design [94].

5.8 Summary

Simulation and analysis outcomes (with static load) of the proposed inverter are presented in this chapter elaborately. In simulation perspective, half bridge configuration in the design (180 degree conduction) is quite favoring to our requirement as compared to the rest of techniques and practices. Simulation results are depicted under various loads for single phase as well as three phase utilization and verified the ability of the proposed inverter to generate square wave output with higher efficiency. These analyzed results found consistent, showed good agreement and covenant with the theoretical estimation coupled with ratification of the reliability of the anticipated inverter. These outcomes also substantiate that the proposed three phase high frequency inverter circuit has the ability to generate square wave output using fewer components (power switches and capacitors).This chapter also evaluates the predicted performance of this design in terms of efficiency under various loads in the light of losses (i.e. snubber losses, switching losses and conduction losses) as well total harmonic distortion (THD). In a nutshell, the results from the simulation as well as theoretical (mathematical) estimations are consistent. Moreover the comprehensive simulations have been anticipated to deliberate the effectiveness of the proposed inverter in solid state transformer applications.

Chapter 6

Conclusion and Recommendations

A brief conclusion of thesis is outlined in this chapter. Some future research recommendations are suggested for researchers interested to work in the area of Solid State Transformer and in particular PWM inverter. The first section is devoted to the summary of the thesis along with the concluding remarks. Possible direction for the future research is presented in the later part.

6.1 Thesis Summary and Conclusion

The accessibility of functionalities such as power flow control, voltage regulation, harmonic suppression, voltage sag ride through capability and weight reductions make the SST an enabling technology for energy systems and applications characterized by space limitations. Nevertheless, the design of the high frequency PWM inverter is taken the most challenging and demanding portion from the electronics point of view and also considered to be one of the significant components of isolated DC-DC converter in a SST application.

Numerous topologies and configurations to realize a SST were presented in Chapter 1 and Chapter 2 and it was concluded that the key anticipated characteristics of a SST topology must include: the availability of a LV DC link, input power factor correction, control functionality, reduced number of components, input and

output voltage regulation, reactive power compensation, ride through capability, weight reduction and power quality improvement, etc. Therefore, topologies consisting of two or three stages with a LV DC link are the most suitable for the SST implementation since two stages and three stages SST can provide the main features required in energy systems. Two stages SST with high DC (i.e. HVDC) link is less appropriate topology as it is devoid of isolation arrangement from the grid, thus not complying with smart grid requirements. In addition, this DC link is not appropriate for distributed energy store (DES) and distributed energy resources (DER). The inverter (DC-AC converter) part of this topology is common for high order SST topologies. Three-stage SST configuration (segregated five parts/blocks) (i.e. topology with high voltage (HV) as well as with low voltage (LV) DC links) is the most feasible and appealing topology of SST. HVDC and LVDC links are meant to enhance the ride through proficiency of SST; thereby allowing the improvement of power quality at input as well as output ends.

Power conversion using high frequency inverters are achieving improved consideration in scheming high frequency power distribution arrangements. In bridge arrangement, the vivacious and significant structures proposed are Full Bridge (FB) and Half Bridge (HB) Inverter in step down and step up mode; where performance parameters concerning efficiency and total harmonic distortion (THD) were deliberated through simulation and experimental results. In case of dual half bridge (DHB) arrangement, the transformer flux swing was merely half of that of the dual active bridge (DAB) arrangement using the same transformer effective cross sectional area and switching frequency. In addition, the number of switching devices and correspondingly, the equivalent drivers were also half in number in DHB arrangement comparatively. Hence such uniqueness and distinctiveness contribute towards more cheap and inexpensive solution.

The dynamic mathematical model of Solid State Transformer was investigated in chapter 3. Consequently, three design considerations were investigated, with particular emphasis on PWM inverter in full bridge and half bridge configuration perception. From analysis of these prospects, it concluded that half bridge topology favored the need as it required lesser number of components, low cost and high efficiency etc. Modeling of inverter with transformer system was also undertaken

and further highlighted prominent differences between full bridge and half bridge configurations in parameter perspective. Difference between fixed load inverter and variable load inverter was also deliberated. The variable load PWM inverter being the most suitable and substantial for distribution applications is adopted and implemented.

The design of 15KV PWM inverter in three phase perspective adopting half bridge topology for SST applications has been proposed in chapter-4 after analyzing mathematically. This structure has the reduced number of power switches as well as DC voltage sources as compared to the rest of configurations. This design is evaluated mathematically as a single phase as well as three phase inverter from all the parameter perspective. Mathematical calculations of total harmonic distortion (THD) and efficiency have been considered concisely.

The design contemplations integrated into the proposed PWM inverter was implemented in MATLAB® as an interactive tool for designing high frequency PWM inverter in Chapter 5. The design methodology accounts for the phase difference of 120 degrees in each phase. Simulation results while switching at 50 kHz show the performance and suitability of the projected topology in SST fabrication with effective improvements in order to validate and authenticate the theoretical analysis. It was concluded that these simulation results are consistent and show virtuous agreement and covenant with the theoretical fallouts with conformity to the reliability of the projected inverter.

To conclude, in this dissertation, the design of 15KV PWM inverter at 100KVA rated power using half bridge topology in three phases for SST applications is anticipated and simulated. The incorporated design methodology accounts for the phase difference of 120 degrees in each phase. Simulation results (switching at 50 kHz) show the suitability of this inverter with effective improvements to validate the theoretical analysis as well as depicting/verifying it's to generate square wave AC output. In static load modeling, the stability of this prototype inverter (DC-AC converter) under various load perspective is strongly established. To gauge the conversion efficiency, the design (as a single phase as well as three phase) has been evaluated on different resistive loads. As a single phase inverter with 15kV

input DC voltage, its conversion efficiency estimated from 98.05% to 98.34% at the resistive load ranging from 60Ω to 4000 Ω and as a three phase, this efficiency is estimated from 97.79% to 98.42% at a resistive load ranging from 190Ω to 10000Ω. Total Harmonic Distortion measurement for three phase proposed design is measured using modulation technique. In this arrangement with 15KV dc input, the FFT analysis in simulation shows the THD to be 47.73% for each phase of the proposed inverter. These examine found consistent, unswerving, showed virtuous agreement and covenant with the theoretical estimation. These are the performance parameters of the proposed inverter which clearly dictates the efficacy and significance of the research and also substantiate that the proposed three phase high frequency inverter design has the ability to generate square wave output with less harmonics distortion with commendable efficiency using fewer components (power switches and capacitors).

6.2 Recommendations for Future Work

The research work presented in this thesis focuses on the high frequency PWM inverter as a part of Solid State Transformer in distribution system applications. Following are some recommendations for researchers who want to work in this area:

- Development of hardware and execution of high frequency PWM inverter for Solid State Transformer may be carried out.
- With the objective of diminishing the harmonic content in the output voltage regulation, appropriate filter network may be worked out and introduced.
- Comparison of the total harmonic distortion (THD) of the proposed design with the rest of techniques, incorporating varying types of carrier wave may be undertaken.
- Implementation and execution of three phase inverter for other industrial applications may be evaluated.

- An accurate cost analysis of the proposed inverter system at manufacturing stage can be carried out.

- Integration of an innovative and appropriate controller which could lead to very low THD for the output current, even in the presence of nonlinear/unbalanced load.

- An automatic voltage regulator (AVR) maintains a constant voltage level on the same load and regulates voltage variations to deliver constant voltage. Implementation and execution of an appropriate AVR for the realized inverter may be appraised.

- Extending the work/operation of the proposed three phase inverter in dynamic load scenario.

- Other than the three stages SST evaluate and appraise other possible SST topologies, and their impact on high frequency inverter (DC-AC converter) design in order to establish the most suitable, significant and momentous configuration in terms of efficiency, functionalities, cost, total harmonic distortion (THD) and power density for a particular application.

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Appendix A

TABLE A1: Summary of solid state transformer.

Year	Development	Result/Observation	Ref.
1980	Single Stage, AC-AC (Step Down converter)	Low output voltage level. Lack of an isolation transformer and DC bus.	[192]
1995	Single Stage, AC-AC (Step Down Converter)	Low output voltage level. Lack of an isolation transformer and DC bus.	[193]
1996	Single Stage, (High Frequency AC link)	Reduction in transformer size/weight. No arrange-ment for instantaneous voltage regulation and voltage sags compensation. Lower stress factors. Low output voltage level.	[194]
1999	Three Stage (High Frequency AC link)	Reduction in size and losses. Improved voltage regulation. No arrangement for control as well as Power factor improvement. Lack of DC bus. Efficiency - 80%.	[195]
2000	Three stage cascaded H-bridge (HF AC link)	Critical loads and energy storage system protection.	[196]
2006	5kVA, 220V / 380V, 2-stage (Direct AC/AC HF link)	Unbalanced linear load and input voltage, Lower Total Harmonic Distortion (THD).	[199]
2000	10kVA, 7.2kV / 240V, 3-stage	Enhancement in Control and power factor. The output efficiency - 90%.	[197]

2005	Three stage (HF AC link)	Provision of power quality functions, galvanic isolation and isolation of a disturbance from either source or load. Rising cost with appreciable efficiency.	[198]
2006	50kVA, 2.4kV / 240V / 120V 3-stage (3 level NPC in MV side)	Voltage sag compensation. Fault isolation. Load variation, Unbalanced load.	[200]
2006	High Frequency DC link	PF improvement. Protection of critical loads and energy storage system. Usage of numerous power converter and DC link electrolytic capacitors.	[201]
2008	Single phase, three stage, (cascaded H-bridge)	PF improvement. Protection of critical loads and energy storage system. Low efficiency and reliability.	[202]
2009	High Frequency DC link	Maintaining of source voltage balance among different modules. Lower efficiency due to a number of components.	[203]
2010	2kW, 110V / 20V, Single-stage (AC-AC)	Steady state response, Bidirectional power flow, Maximum power point tracking.	[204]
2010	20kVA, 7.2kV / 240V, 3-stage, (cascaded H-bridge)	Steady state response, Bidirectional power flow, Maximum power point tracking.	[205]
2011	High Frequency DC link	Reduction in voltage stress, rating of components and lower efficiency.	[206]
2011	1.2MVA, 15kV/16.7Hz 2-stage, cascaded H bridge	Steady state response Bidirectional power flow.	[207]
2012	1kW, 208V / 120V Three-stage (two level)	Steady state response Bidirectional power flow.	[208]

2012	Three stage AC/AC (Matrix converter based SST HF DC link)	Reduction in number of components, escalating efficiency, while reduction in power quality with the voltage stress factor.	[209]
2012	Three phase, single-stage (Matrix converter)	Voltage regulation is 0.5-1. Higher Total Harmonic Distortion (THD).	[210]
2013	100KW, 10kV AC-750V DC 2-stage (AC / DC / DC, MMC)	Steady state response and bidirectional power flow.	[211]
2014	3.6kV-120V / 10kVA, Three stage (FB HF AC link)	Accessibility for both AC and DC outputs. Efficiency of system ranges from 84% to 88%.	[63]
2015	600kVA, 3.3kV DC / 3.3kV DC, 3-stage (cascaded H-bridge in MV side)	Steady state response and Bidirectional power flow.	[212]
2015	5kW, 300V AC / 380V DC 2-stage (cascaded H-bridge)	Steady state response and Bidirectional power flow.	[213]
2015	2kW, 300V / 60V, 3-stage (two level)	Steady state response, load variation and bi-directional power flow.	[214]
2015	2 kVA, 380V / 120V Three stage, (cascaded)	Steady state, power flow reversal, startup and bi-directional power.	[215]
2015	5.8 kVA, 5kV DC / 800V DC, 3-stage (NPC with SiC)	Steady state response and bidirectional power flow.	[216]
2016	Three stage (HF AC link)	Ability to substitute the ancient version CT in near future.	[65]
2016	50 kVA, 480V / 480V, Single stage, Dyna-C (AC / AC topology)	Steady state response and bidirectional power flow.	[217]

2016	3kVA, 2.4kV / 127V, 3-stage (two level)	Steady state response, nonlinear load and unidirectional power flow.	[218]
2016	10kVA, 208V, Single stage AC-AC (two level, soft switching)	Steady state response and bidirectional power flow.	[219]
2017	2kW, 400V / 208V Single stage, AC-AC, matrix based	Steady state, load variation, unbalanced voltage & current and bidirectional power flow.	[220]
2018	High Frequency AC link (Three phase modular)	Possibility of SST implementation in marine electrical power systems and offer various advantages in the marine power system for enhancing the efficiency and environmental sustainability of future ships.	[69]
2019	Three Phase SST Design	Generation of single phase, three phases or DC voltage.	[116]

TABLE A2: Summary of isolated DC-DC converter.

Year	**Converter Type**	**Result/Observation**	**Ref.**
2013	DHB DC-DC converter [1KW(385V–48V)]	Use of 50% duty cycle by each switch to function, attaining ZVS over an extensively varying load. Efficiency = 96% (light and heavy weight both).	[72]
2014	DAB DC-DC converter (Full Bridge)	3-level DC-DC converters in FB possess the capability for enhancing light load efficiency as compared to 2-level DC-DC converters.	[73]
2015	DAB DC-DC converter (Full Bridge)	Two equivalent resistances are being added in primary of HF transformer to increase the accuracy of power and efficiency.	[74]

2016	DHB DC-DC converters (Half Bridge)	Better anti-imbalance capability in transformer. Can function in step up (29V-380V) as well as in step down (380V-29V). In step down mode, it attained the efficiency in excess of 90%, while in step up mode; it achieved an efficiency of 82%.	[76]
2017	Three level DC-DC converter	Maintaining galvanic isolation and high voltage conversion ratio using medium frequency transformer (400Hz-20kHz). THD reduction for primary voltage (HF inverter) from 48% to 37%, where-as this performance reduction in primary current (HF inverter) is from 32% to 28%. The efficiency is increased from 81% to 92%.	[77]
2017	1.7kW isolated DC-DC converter bidirectional)	Very compact in size, possesses reduced power loss and reduced heat sink requirement. In step down mode operation (for DC input) the peak efficiency recorded was 80%,whereas in step up mode operation, the peak efficiency was also 80%	[78]
2017	3kW experimental and trial DC-DC converter prototype	Possesses high efficiency, reduced voltage stress and operate at a varied ZVS range in lowered switching losses.	[79]
2018	20kW quadruple active bridge (QAB) converter	Possesses an efficiency of 97.5%, where-as the converter's loss is around 57%, in contrast to IGBTs. This reduction is noticed because of the usage of SiC-MOSFETs.	[93]

2017	DC-DC Converter (isolated / non isolated)	In an analysis of isolated and non-isolated DC-DC converters, the only isolated DC-DC converters encounter the parameters such as: (1) Standards of utility grid, (2) Simple in accomplishment of multiple output voltages and (3) Suitability for high power levels.	[80]

TABLE A3: Summary of high frequency inverters.

Year	**Converter Type**	**Result/Observation**	**Ref.**
2011	DC-DC converter (Dual Half Bridge) (1KW)	DHB is more economical with less number of switches as compared to DAB ; achieving an efficiency of 97.2% at 50kHz operation	[82]
2012	Half-Bridge PV Inverter System	The quantity of active switches is reduced to half in comparison to FB topology, thereby resulting in system simplification and reduction in cost.	[94]
2015	ML PWM inverter (Cascaded H Bridge)	Better performance in MLIs than conventional ones.	[83]
2016	Three phase inverter	With change in duty cycle of inverter, load impedance can be adjusted while matching source impedance. Efficiency may be improved in real time.	[84]
2016	DC-DC Converter (with H6 Bridge)	Six level solutions for single phase grid connected converters is presented. 5 levels inverter attained efficiency up to 95%, more than the conventional DC-AC inverters.	[85]
2017	Multilevel inverters	H-Bridge possesses some advantages due to its easy extensibility to high number of level and implementation.	[90]

2016	Dual Active Bridge Converter	With help of effective soft start algorithm, the inrush current through the switches is suppressed significantly at the startup state of the DAB. Improved efficiency	[86]
2016	Multilevel inverters	MLI possesses 3 major topologies such as, capacitor clamped, diode camped and cascaded. Improved performance in MLIs than conventional ones noticed.	[87]
2016	Multilevel inverters	Eleven (11) levels inverter offers more efficient performance in terms of the PF, THD and its efficiency as compared to 7-9 level MLI.	[88]
2017	3 Phase PWM Inverter	Three phase ac power of 0.8V, displaced by 120 phase shift provided to the inverter resulted into an almost sinusoidal current wave. The amplitude MI was ≤ 1	[89]
2017	Three phase DAB (with 3L-NPC half bridge)	Three level topologies are promising solution for LVC. HB solution is preferred at MV side of DC-DC converter.	[91]
2017	Single phase 7 level inverter	Enhanced efficiency and lesser THD than conventional inverter.	[92]
2017	40V / 120V, 5KW Three level DC-DC converter (isolated)	Reduction of THD of primary voltage (HF inverter) is from 48% to 37%. Reduction of THD of primary current (HF inverter) is from 32% to 28% with 3 level. Efficiency enhanced from 81% to 92%.	[98]
2018	Multiple-Active-Bridge DC-DC Converter (20kW prototype)	Efficiency up-to 97.5%. Usage of SiC-MOSFETs reduces the converter's losses to approx. 57%, as compared to the IGBT.	[93]

2018	Half-Bridge Inverter (Transformer Isolated)	Operation/functionality noticed at ideal point. Satisfactory settings operation for ZVS turn-on of all devices through the power range of the converter. Constant and adequate vibrant response of the converter. Offer significant efficiency gains over conventional square-wave control.	[99]